

FLORIAN BRANDNER

DONNÉES PERSONNELLES

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EXPÉRIENCE PROFESSIONNELLE

Télécom ParisTech *actuellement* Maître de conférences , Paris, France
Maître de conférences dans le équipe S3 du laboratoire LTCI de Télécom ParisTech (Université Paris-Saclay).

ENSTA ParisTech 10/2013
08/2015 Enseignant-chercheur, Palaiseau, France
Enseignant-chercheur dans l'Unité d'Informatique et d'Ingénierie des Systèmes de l'ENSTA ParisTech (École Nationale Supérieure de Techniques Avancées).

DTU Compute 11/2011
09/2013 Post-doc, Copenhague, Danemark
Chercheur en post-doc à la section des systèmes embarqués de DTU Compute (Denmarks Tekniske Universitet). Financé par le projet européen T-CREST.

INRIA Grenoble 10/2009
10/2011 Post-doc, Lyon, France
Chercheur en post-doc au Laboratoire de l'Informatique du Parallélisme (LIP) à l'École Normale Supérieure de Lyon (ENS de Lyon). Financé par l'INRIA et le projet Mediacom.

MSR Redmond 04/2009
07/2009 Microsoft Research, Redmond, WA, USA
Stage de recherche à Microsoft Research sur la génération de code just-in-time pour le langage JavaScript dans le projet SPUR.

CD Laboratoire Doctorat 10/2005
02/2009 Assistant de Recherche, Vienne, Autriche
Travail sur la compilation portable, les optimisations de la compilation, et les langages pour la description des processeurs dans le Christian Doppler Laboratory – Compilation Techniques for Embedded Processors. Financé par ONDEMAND Microelectronics et la Christian Doppler Forschungsgesellschaft.

StarCore LLC. 03/2004
10/2004 Ingénieur Compilation, Vienne, Autriche
En 2004 *StarCore* (aujourd'hui *LSI LOGIC*) a ouvert une branche à Vienne. J'ai participé au développement des optimisations d'un nouveau compilateur pour les processeurs StarCore SC1200 et SC1400.

01/2004
02/2004 Ingénieur, Vienne, Autriche

Atair GmbH. Développement d'un langage pour la description des processeurs pour le compilateur Open Compiler Environment (OCE) de *Atair.D*

2002
2005 Assistant d'Enseignement, Vienne, Autriche

Vienna University of Technology Assistant d'enseignement dans l'équipe Languages Group de l'Institute of Computer Languages ; dans le laboratoire Distributed Systems Laboratory de l'Institute of Information Systems ; et dans l'équipe Database and Artificial Intelligence Group de l'Institute of Information Systems.

ÉDUCATION

10/2005
12/2009 Vienna University of Technology, Autriche

Doctorat Doctorant en informatique à Vienna University of Technology. La soutenance (Rigorosum) a eu lieu à Vienne le 18 decembre, 2009.

Thèse : Compiler Backend Generation from Structural Processor Models
Jury : Jens Knoop, Andreas Krall, Tomáš Hruška
Directeur : Andreas Krall

09/1999
10/2004 Vienna University of Technology, Autriche

*Dipl. Ing.
Master* Étudiant en informatique à Vienna University of Technology.
Diplômé avec distinction en 2004.

Thèse : Instruction set simulation
Directeur : Andreas Krall

06/2003
01/2004 Technical University of Denmark, Lyngby

Exchange Étudiant en informatique à la Technical University of Denmark (DTU) à Lyngby à-côté de Copenhague, Danemark.

09/1991
06/1999 BG/BRG Bruck an der Mur, Autriche

Lycée Étudiant dans la lycée BG/BRG Bruck an der Mur, Autriche.

INFORMATION SUPPLÉMENTAIRE

Languages ANGLAIS · Couramment
FRANÇAIS · Conversation
ALLEMAND · Langue maternelle
DANOIS · Lecture

CHAPITRES DE LIVRE

DSP Instruction Set Simulation

Florian Brandner, Nigel Horspool, and Andreas Krall
Handbook of Signal Processing Systems (2nd Edition)
S.S. Bhattacharyya, E.F. Deprettere, R. Leupers, and J. Takala (Éditeur)
2013, Springer

Propagating Information using SSA

Florian Brandner and Diego Novillo
SSA-based Compiler Design
F. Rastello (Éditeur)
à paraître, Springer

DSP Instruction Set Simulation

Florian Brandner, Nigel Horspool, and Andreas Krall
Handbook of Signal Processing Systems
S.S. Bhattacharyya, E.F. Deprettere, R. Leupers, and J. Takala (Éditeurs)
2010, Springer

ACTES DE CONFÉRENCE

Proceedings of the 11th Workshop on Optimizations for DSP and Embedded Systems

Florian Brandner and Tom Vander Aa (éditeurs)
Orlando, FL, USA, 2014
ACM ICPS

Proceedings of the 10th Workshop on Optimizations for DSP and Embedded Systems

Florian Brandner and Tom Vander Aa (éditeurs)
Shenzhen, China, 2013
ACM ICPS

JOURNAUX

Studying Optimal Spilling in the Light of SSA

Florian Brandner, **Florian Brandner**, and Alain Darté
ACM Transactions on Architecture and Code Optimization (TACO)
Volume 11(4) : (2015), ACM

Refinement of Worst-Case Execution Time Bounds by Graph Pruning

Florian Brandner and Alexander Jordan
Computer Languages, Systems & Structures (COMLAN)
Volume 40(3-4) : 155-170 (2014), Elsevier

Criticality : Static Profiling for Real-Time Programs

Florian Brandner, Stefan Hepp, and Alexander Jordan
Real-Time Systems (RTS)
2014, Volume 50(3) : 377-410, Springer

Elimination of Parallel Copies using Code Motion on Data Dependence Graphs

Florian Brandner and Quentin Colombet
Computer Languages, Systems & Structures (COMLAN)
2013, Volume 39(1) : 25-47, Elsevier

Automatic Generation of Compiler Backends

Florian Brandner, Viktor Pavlu, and Andreas Krall
Software : Practice and Experience (SPE)
2013, Volume 43(2) : 207-240, Wiley

CONFÉRENCES

Efficient Context Switching for the Stack Cache : Implementation and Analysis

Sahar Abbaspour, **Florian Brandner**, Amine Naji, and Mathieu Jan
23th International Conference on Real-Time and Network Systems (RTNS)
Lille, France, 2015, ACM ICPS

Splitting Functions into Single-Entry Regions

Stefan Hepp and **Florian Brandner**
International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)
New Delhi, India, 2014, ACM

A Loosely Synchronizing Asynchronous Router for TDM-Scheduled NOCs

Ioannis Kotleas, Dean Humphreys, Rasmus Bo Sørensen, Evangelia Kasapaki, **Florian Brandner**, and Jens Sparsø
International Symposium on Networks-on-Chip (NOCS)
Ferrara, Italy, 2014, IEEE

Static Analysis of Worst-Case Stack Cache Behavior

Alexander Jordan, **Florian Brandner**, and Martin Schoeberl
International Conference on Real-Time and Network Systems (RTNS)
2013, Sophia-Antipolis, France, ACM ICPS

Static Profiling of the Worst-Case in Real-Time Programs

Florian Brandner, Stefan Hepp, and Alexander Jordan
International Conference on Real-Time and Network Systems (RTNS)
2012, Pont à Mousson, France, ACM ICPS

Static Routing in Symmetric Real-Time Network-on-Chips

Florian Brandner and Martin Schoeberl
International Conference on Real-Time and Network Systems (RTNS)
2012, Pont à Mousson, France, ACM ICPS

A Statically-Scheduled Time-Division-Multiplexed Network-on-Chip for Real-Time Systems

Martin Schoeberl, **Florian Brandner**, Evangelia Kasapaki, and Jens Sparsø
Symposium on Networks-on-Chip (NOCS)
2012, Kongens Lyngby, Danemark, ACM/IEEE

Copy Elimination on Data Dependence Graphs

Florian Brandner and Quentin Colombet
Symposium On Applied Computing (SAC-PL)
2012, Riva del Garda, Italie, ACM

A Non-Iterative Data-Flow Algorithm for Computing Liveness Sets in Strict SSA Programs

Benoit Boissinot, **Florian Brandner**, Alain Darte, Benoît Dupont de Dinechin, and Fabrice Rastello
Symposium on Programming Languages and Systems (APLAS)
2011, Kenting, Taiwan, Springer

Studying Optimal Spilling in the Light of SSA

Quentin Colombet, **Florian Brandner**, and Alain Darte
Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)
2011, Taipai, Taiwan, ACM

Execution Models for Processors and Instructions

Florian Brandner, Viktor Pavlu, and Andreas Krall
28th Norchip Conference
2010, Tampere, Finlande, IEEE

SPUR : A Trace-Based JIT Compiler for CIL
Michael Bebenita, **Florian Brandner**, Manuel Fahndrich, Francesco Logozzo,
Wolfram Schulte, Nikolai Tillmann, and Herman Venter
International Conference on Object Oriented Programming Systems Languages and
Applications (OOPSLA)
2010, Reno, USA, ACM

Completeness of Automatically Generated Instruction Selectors
Florian Brandner
21st International Conference on Application-specific Systems, Architectures and
Processors (ASAP)
2010, Rennes, France, IEEE

RTTM : Real-Time Transactional Memory
Martin Schoeberl, **Florian Brandner**, and Jan Vitek
25th Symposium On Applied Computing, Real Time Systems Track, (SAC)
2010, Sierre, Suisse, ACM

Generalized Instruction Selection using SSA-Graphs
Dietmar Ebner, **Florian Brandner**, Bernhard Scholz, Andreas Krall, Peter
Wiedermann, and Albrecht Kadlec
ACM Conference on Languages, Compilers, and Tools for Embedded Systems
(LCTES)
2008, Tucson, USA, ACM

Stack Allocation of Objects in the Cacao Virtual Machine
Peter Molnar, Andreas Krall, and **Florian Brandner**
7th International Conference on the Principles and Practice of Programming in Java
(PPPJ)
2009, Calgary, Canada, ACM

Embedded JIT Compilation with CACAO on YARI
Florian Brandner, Martin Schoeberl, and Tommy Thorn
12th IEEE International Symposium on Object/component/service-oriented
Real-time distributed Computing (ISORC)
2009, Tokyo, Japon, IEEE

Compiler Generation from Structural Architecture Descriptions
Florian Brandner, Dietmar Ebner, and Andreas Krall
International Conference on Compilers, Architecture, and Synthesis for Embedded
Systems (CASES)
2007, Salzburg, Autriche, ACM

Effective Compiler Generation by Architecture Description
Stefan Farfeleder, Andreas Krall, Edwin Steiner, and **Florian Brandner**
ACM Conference on Languages, Compilers, and Tools for Embedded Systems
(LCTES)
2006, Ottawa, Canada, ACM

WORKSHOPS

A Comparative Study of the Precision of Stack Cache Occupancy
Analyses
Amine Naji and **Florian Brandner**
Junior Researcher Workshop on Real-Time Computing (JRWRTC)
Lille, France, 2015

Alignment of Memory Transfers of a Time-Predictable Stack Cache
Sahar Abbaspour and **Florian Brandner**
Junior Researcher Workshop on Real-Time Computing (JRWRTC)
Versailles, France, 2014

Lazy Spilling for a Time-Predictable Stack Cache : Implementation and Analysis

Sahar Abbaspour, Alexander Jordan, and **Florian Brandner**
Workshop on Worst-Case Execution Time Analysis (WCET)
Madrid, Spain, 2014, OASICS Dagstuhl

A Time-predictable Stack Cache

Sahar Abbaspour, **Florian Brandner**, and Martin Schoeberl
Workshop on Software Technologies for Embedded and Ubiquitous Systems (SEUS)
2013, Paderborn, Allemagne

Studying Spilling in the Light of SSA

Quentin Colombet, **Florian Brandner**, and Alain Darté
Workshop on Compilers for Parallel Computing (CPC)
2012, Padoue, Italie

Modeling Application-Specific Processors for Cyber-Physical Systems

Florian Brandner, Viktor Pavlu, and Andreas Krall
Workshop on Software Language Engineering for Cyber-physical Systems (WS4C)
2011, Berlin, Allemagne (LNI)

Compiler-driven Optimization of the Worst-Case Execution Time

Florian Brandner and Alain Darté
Workshop Analyse to Compile, Compile to Analyse (ACCA)
2011, Chamonix, France

Towards a Time-predictable Dual-Issue Microprocessor : The Patmos Approach

Martin Schoeberl, Pascal Schleuniger, Wolfgang Puffitsch, **Florian Brandner**,
Christian W. Probst, Sven Karlsson, and Tommy Thorn
Workshop on Practice, Predictability and Performance in Embedded Systems (PPES)
2011, Grenoble, France

Automatic Tool Generation from Structural Processor Descriptions

Florian Brandner
15th Biennial Workshop on Programmiersprachen und Grundlagen der
Programmierung (KPS)
2009, Maria Taferl, Autriche

Precise Simulation of Interrupts using a Rollback Mechanism

Florian Brandner
12th International Workshop on Software and Compilers for Embedded Systems
(SCOPES)
2009, Nice, France

Completeness of Instruction Selector Specifications with Dynamic Checks

Florian Brandner
8th International Workshop on Compiler Optimization Meets Compiler Verification
(COCV)
2009, York, Angleterre

Fast and Accurate Simulation using the LLVM Compiler Framework

Florian Brandner, Andreas Fellnhöfer, Andreas Krall, and David Riegler
1st Workshop on Rapid Simulation and Performance Evaluation : Methods and Tools
(RAPIDO)
2009, Paphos, Chypre

Leveraging Predicated Execution for Multimedia Processing

Dietmar Ebner, **Florian Brandner**, and Andreas Krall
Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia)
2007, Salzburg, Autriche

Static Verification of Global Heap References in Java Native Libraries
Andreas Krall, Christian Thalinger, Dietmar Ebner, and **Florian Brandner**
Workshop on Semantics, Program Analysis, and Computing Environments for
Memory Management (SPACE)
2006, Charleston, USA

RAPPORTS DE RECHERCHE

Subgraph-Based Refinement of Worst-Case Execution Time Bounds
Florian Brandner and Alexander Jordan
ENSTA Technical Report, hal-00978015
Palaiseau, France, Avril 2014

Parallel Copy Elimination on Data Dependence Graphs
Florian Brandner and Quentin Colombet
INRIA Technical Report RR-7535
Lyon, France, Septembre 2011

Computing Liveness Sets for SSA-Form Programs
Florian Brandner, Benoit Boissinot, Alain Darté, Benoît Dupont de Dinechin, Fabrice Rastello
INRIA Technical Report RR-7503
Lyon, France, Janvier 2011

SPUR : A Trace-Based JIT Compiler for CIL
Michael Bebenita, **Florian Brandner**, Manuel Fahndrich, Francesco Logozzo,
Wolfram Schulte, Nikolai Tillmann, and Herman Venter
Technical Report MSR-TR-2010-27
Microsoft Research
Redmond, USA, Mars 2010

Embedded JIT Compilation with CACAO on YARI
Florian Brandner, Tommy Thorn, and Martin Schoeberl
Technical Report RR 35/2008
Institute of Computer Engineering
Vienna University of Technology
Vienne, Autriche, Juin 2008

RAPPORTS DE PROJET

D2.1 Software Simulator of Patmos
Florian Brandner
rapport du projet T-CREST
Kongens Lyngby, Danemark, Mars, 2012

D5.2 Initial Compiler Version
Florian Brandner, Stefan Hepp, and Daniel Prokesch
rapport du projet T-CREST
Vienne, Autriche, Septembre, 2012

THÈSES

Compiler Backend Generation from Structural Processor Models
Florian Brandner
Thèse
2009, Vienna University of Technology, Vienne, Autriche

Instruction Set Simulation
Florian Brandner
Diplôme (Master)
2004, Vienna University of Technology, Vienne, Autriche

RÉFÉRENCES

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