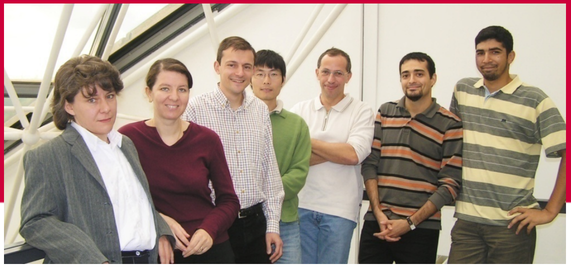
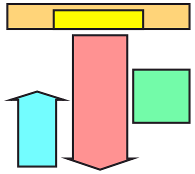
IT/TPT/COMELEC/LabSoC



- A research group of Communications and Electrical Engineering department, Telecom ParisTech, Institut Telecom
- Based in Sophia-Antipolis (French Riviera)
- 11 researchers:
  - 4 full-time researchers
  - 2 research engineers
  - 5 PhDs
- More information at:
  - http://www.comelec.telecom-paristech.fr/recherche/labsoc.en
  - renaud.pacalet@telecom-paristech.fr

LabSoC's Research topics

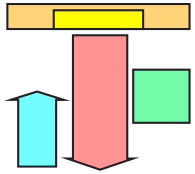


- **SoC design methodologies**
  - Design Space Exploration
  - Refinement, abstraction
  - Ultra-fast simulation, formal verification

- **Security of embedded systems**
  - Fault and side channel attacks
  - Bus probing
  - HW/SW formal verification

- **Architectures for the software defined radio**
  - Baseband Digital Signal Processing

LabSoC's Research topics



- **SoC design methodologies**
  - Design Space Exploration
  - Refinement, abstraction
  - Ultra-fast simulation, formal verification

- **Security of embedded systems**
  - Fault and side channel attacks
  - Bus probing
  - HW/SW formal verification

- **Architectures for the software defined radio**
  - Baseband Digital Signal Processing

Agenda

- Context
- EMBB architecture
  - Selection of DSP units
  - Memory architecture
  - Interconnect
  - Control and standardized DSP unit architecture
- Examples of DSP units
- Target technologies
- Software architecture and tools

Agenda

- **Context**
- **EMBB architecture**
  - Selection of DSP units
  - Memory architecture
  - Interconnect
  - Control and standardized DSP unit architecture
- **Examples of DSP units**
- **Target technologies**
- **Software architecture and tools**

Related collaborative projects - partnerships

- **Projects**
  - IDROMel (ANR)
  - PFMM (pôle SCS / DGE)
  - SYMPA (pôle SCS / DGCIS / PACA)
  - SACRA (FP7)
  - SPECTRA (Celtic)

INABENSA

ST ERICSSON

indra

TeamCast

Wellness Telecom

Monaco telecom

TELLEMENT MONACO

intel

DMCE

DANUBE MOBILE COMMUNICATIONS ENGINEERING

Agence Nationale des Fréquences

CISCO

Supélec

Fraunhofer IIS

NXP founded by Philips

3Roam

EURECOM Sophia Antipolis

VTT

ΕΘΝΙΚΟΝ & ΚΑΠΟΔΙΣΤΡΙΑΚΟΝ ΠΑΝΕΠΙΣΤΗΜΙΟΝ ΑΘΗΝΩΝ

NATIONAL & KAPODISTRIAN UNIVERSITY OF ATHENS

freescale semiconductor

cea

SIRADEL

france telecom

NEC

NEC Technologies

Infineon

TELECOM ParisTech

Why a flexible baseband processing

- **The number of air interfaces increases**
  - Today's embedded systems commonly operate on 3 or more interfaces (2G, 2.5G, 3G, WiFi, Bluetooth, GPS,…)
  - These interfaces share a lot of basic processing
- **Many side band new services**
  - Sensing, cognitive / opportunistic / cooperative radio
  - Spectrum aggregation, relaying
  - RF / BB co-design (optimization, "dirty" RF)
  - Femto – pico cells, relaying
- **All these share a lot of basic processing**

How a flexible baseband processing

- **There are many candidate architectures addressing this application field**
  - ASIC / ASIP / DSP / GP-CPU
  - Non-Uniform v.s. uniform memory access
  - Networks on chip, crossbars, busses
  - Synchronous / asynchronous design
  - Dynamic configuration / parameterization / programmability
  - …

Key criteria of a flexible baseband processing

- **Power efficiency**
  - ASIC: 1x, DSP: 10x, GP-CPU: 100x
  - P_{UE} < 3W (thermal dissipation)
  - P_{BB} < 1W (PA, LNA, UI, application processor)
  - 100 Gop/s => 1 Top/s (1 to 10 pJ / op)
  - ARM Cortex A9 dual core, 40nm, power optimized: 4 DGIPS, 0.5 W
- **Flexibility**
- **Usability**

Agenda

- Context
- EMBB architecture
  - Selection of DSP units
  - Memory architecture
  - Interconnect
  - Control and standardized DSP unit architecture
- Examples of DSP units
- Target technologies
- Software architecture and tools

Our proposal for a flexible baseband processing

- **A set of flexible DSP units**
  - Parameters (Look Up Tables, etc.)
  - Software (local and global)
  - Interconnect (partial crossbar)
- **A standardized IP-to-interconnect interface**
- **A well specified, multi-layers, API**
  - Basic DSP commands (FFT, Viterbi decoding, etc.)
  - Macros (channel estimation, etc.)
  - Synchronization primitives

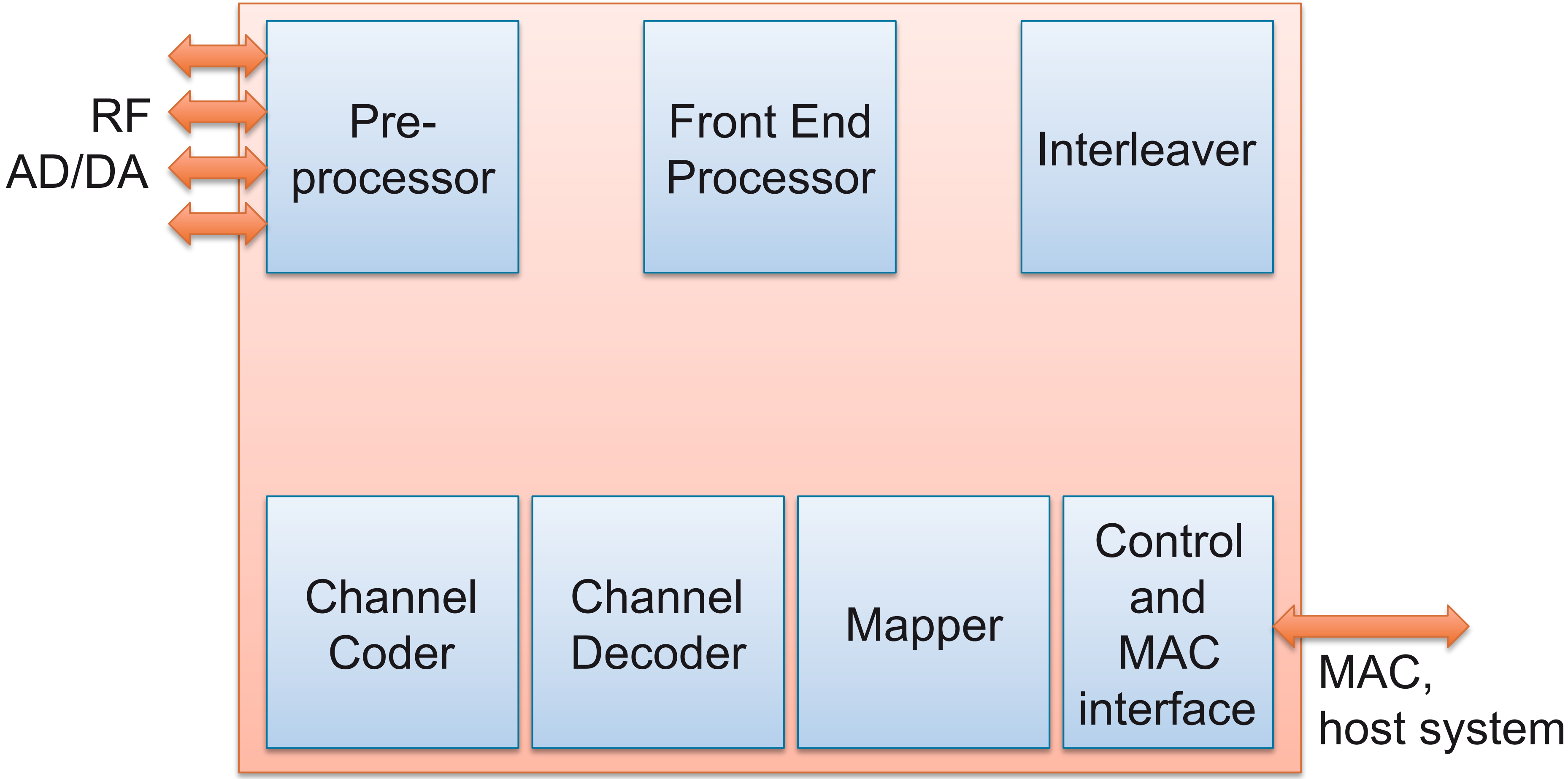
Selection / specification of DSP units

- **Multiple air interfaces**
  - GSM, WCDMA, DVB, WLAN, LTE, …
- **Plus sensing, etc.**
- **TX almost straightforward**
- **RX can be done in many ways**
  - Intra and inter-interfaces local/global optimization
  - Data types (complex, fixed point, vectors, …)
  - Similarities between processing
  - Data flows, DSP unit to DSP unit channels
  - Tradeoffs monolithic integration / flexibility

Selection / specification of DSP units

- **Interface with RF, A/D-D/A (pre-processing)**
  - Re-timing filters, NCO, I/Q imbalance, packets
- **Vector/matrix processing (front end processing)**
  - DFT/IFT, vector component-wise operations, energy, max, argmax, min, argmin,...
- **Mapping**
  - BPSK, QPSK, 8PSK, 16QAM, 32QAM, 64QAM, 256QAM,…, 65536QAM
- **Interleaving, rate matching, frame equalization**
- **Channel coding / decoding (Viterbi, turbo)**
- **Interface with MAC layer, control**

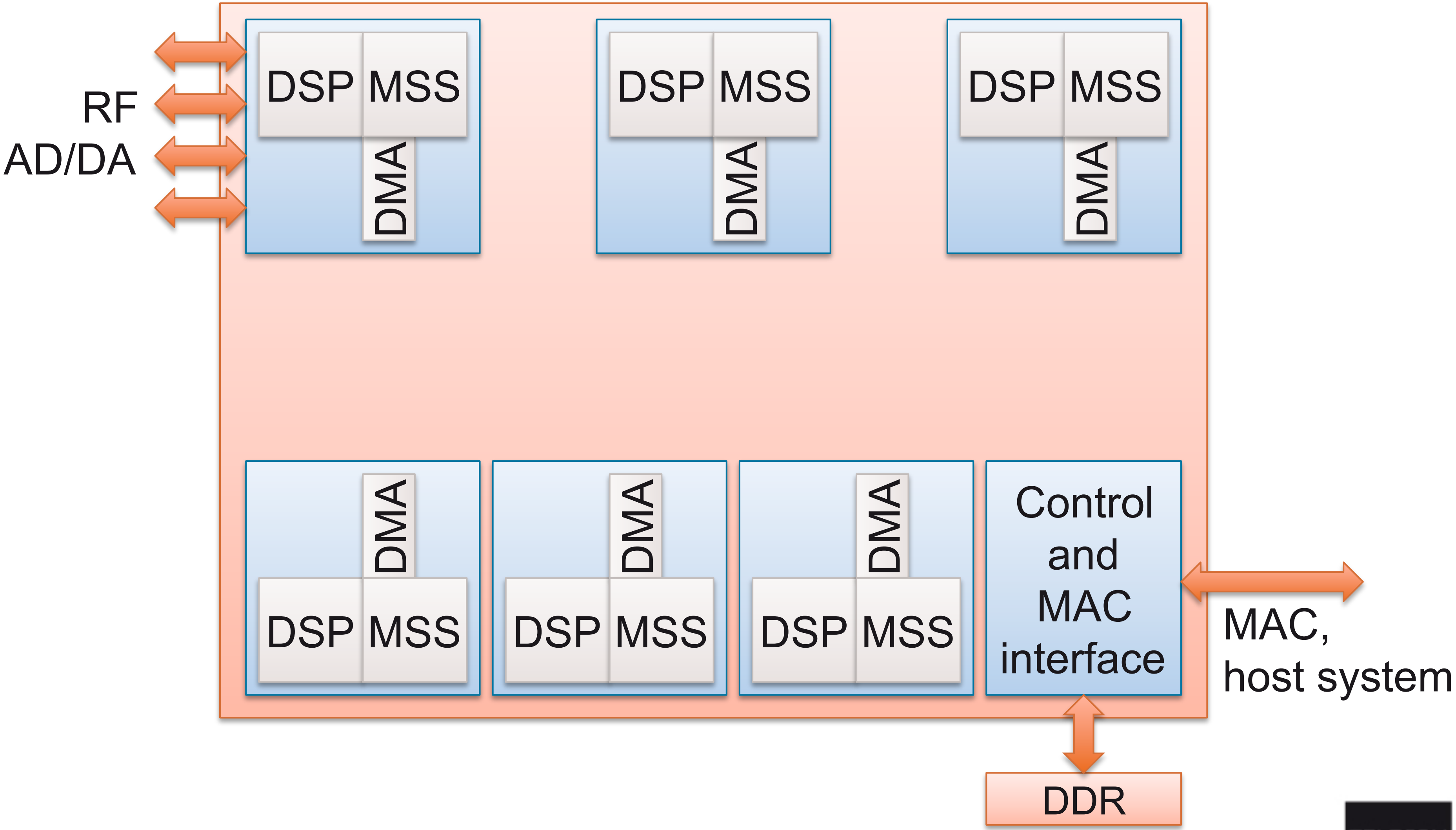
Our proposal for a flexible baseband processing



The memory architecture

- **Monolithic memory => bottleneck**
- **Non-uniform, distributed memory architecture**
  - Distributed local working memories
  - Mapped in the global memory map
- **Two exported views**
  - Local (high bandwidth, fancy organization),
  - Global (medium bandwidth, regular organization)
- **Parallelization of I/Os and processing**
- **Embedded DMA engines**
- **External DDR for mass storage**

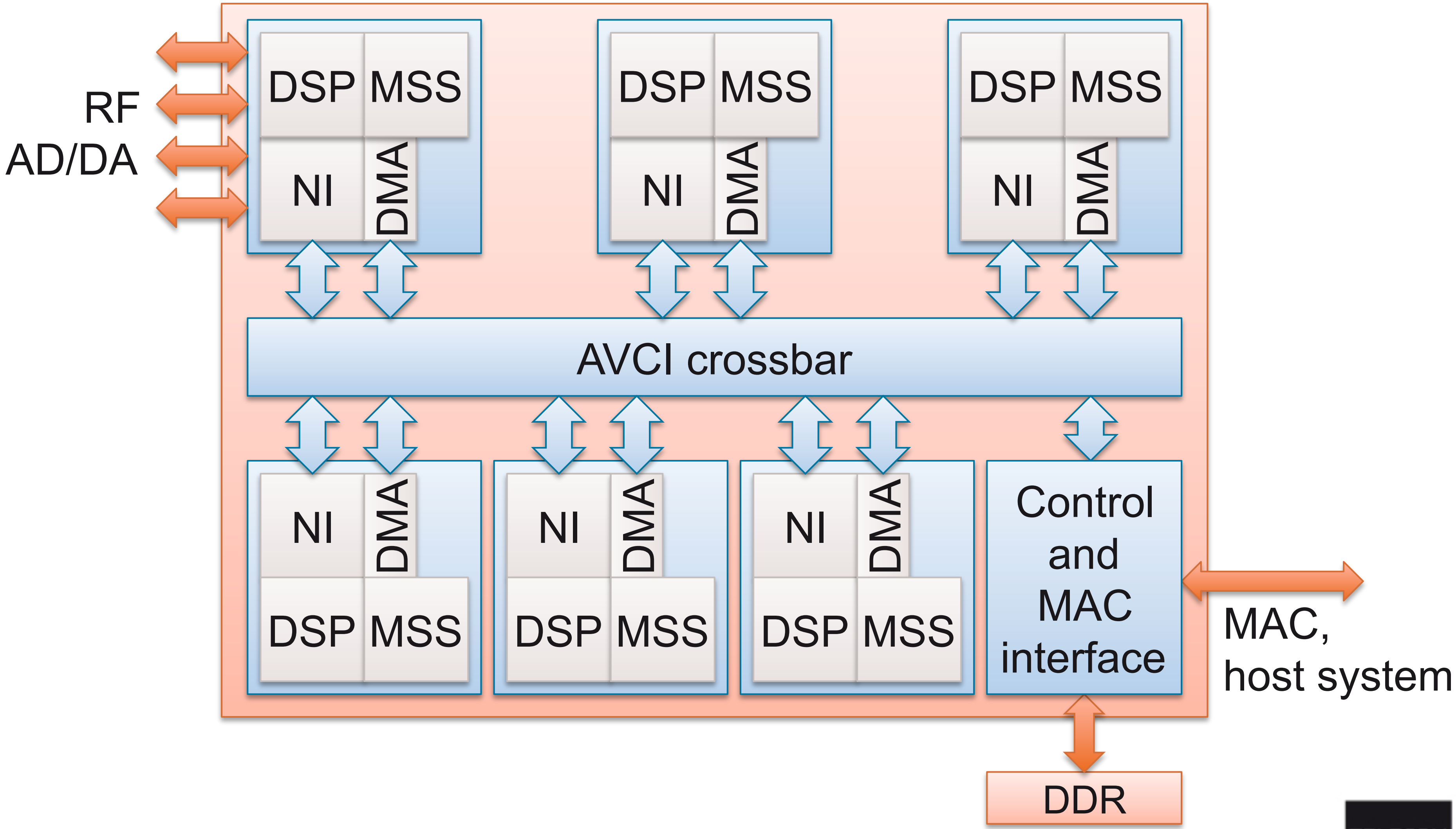
Our proposal for a flexible baseband processing



The interconnect

- **Medium to small number of processing units**
- **High bandwidth, low latency**
- **Simple, deterministic, powerful switch fabric**
- **Memory-mapped communications**
  - Command registers
  - Data blocks through DMA transfers
  - Interrupts, synchronization, signals
- **A generic partial crossbar**
  - 64 bits, natively compliant with Advanced VCI
- **Standardized network interface**

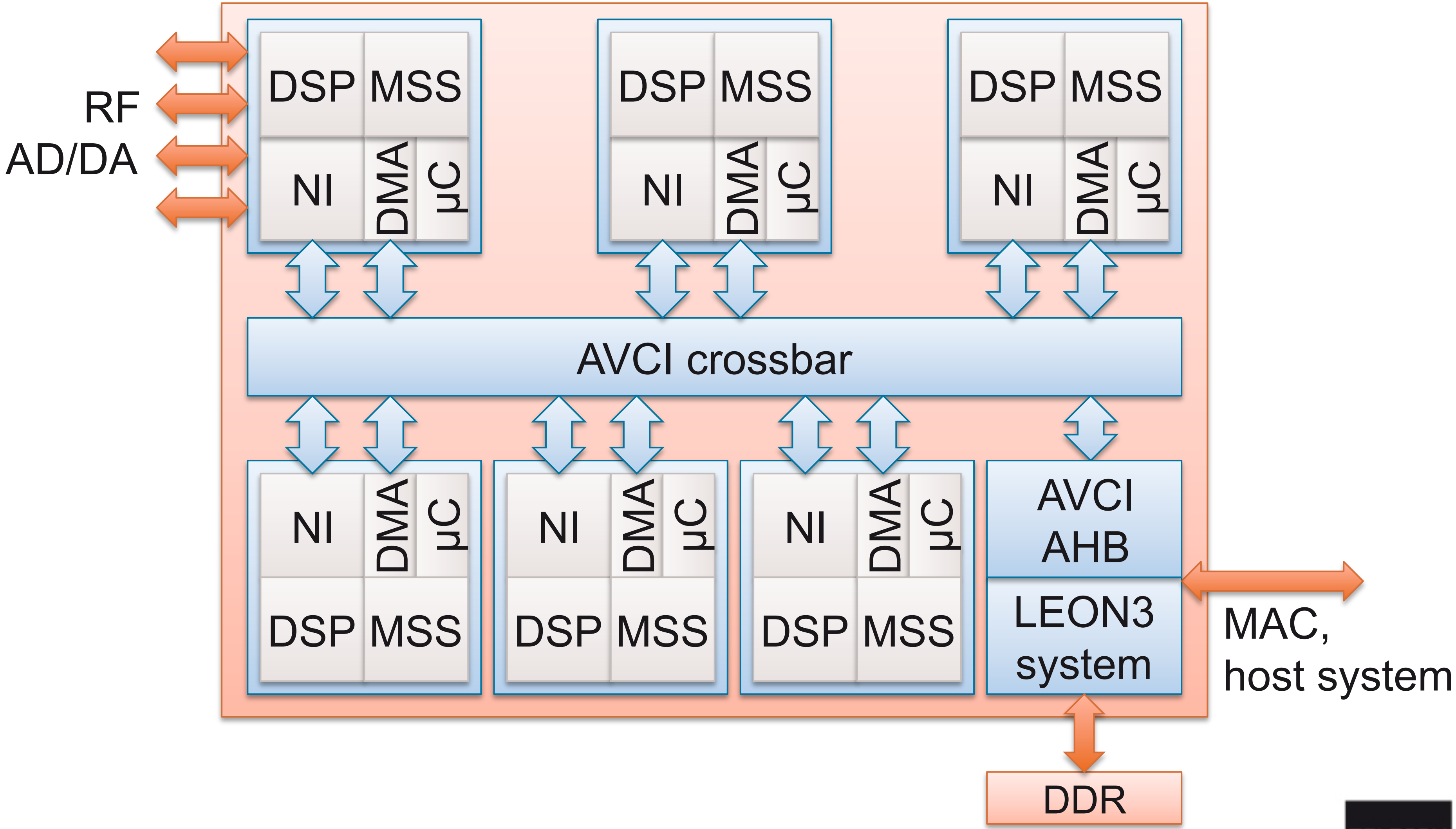
Our proposal for a flexible baseband processing



Global / local control

- **A 32 bits CPU to control and interface with host**
  - Open source LEON3 Sparc by Aeroflex-Gaisler
  - Plus GRlib IPs
  - AMBA AHB system bus (=> AHB/AVCI bridge)
- **A local small controller in each DSP unit**
  - 8 bits µC
  - Control DMA engine and DSP core
  - Address space in Memory Sub-System
  - Chain / control local processing and data transfers
  - Reduce interrupts rate to main CPU

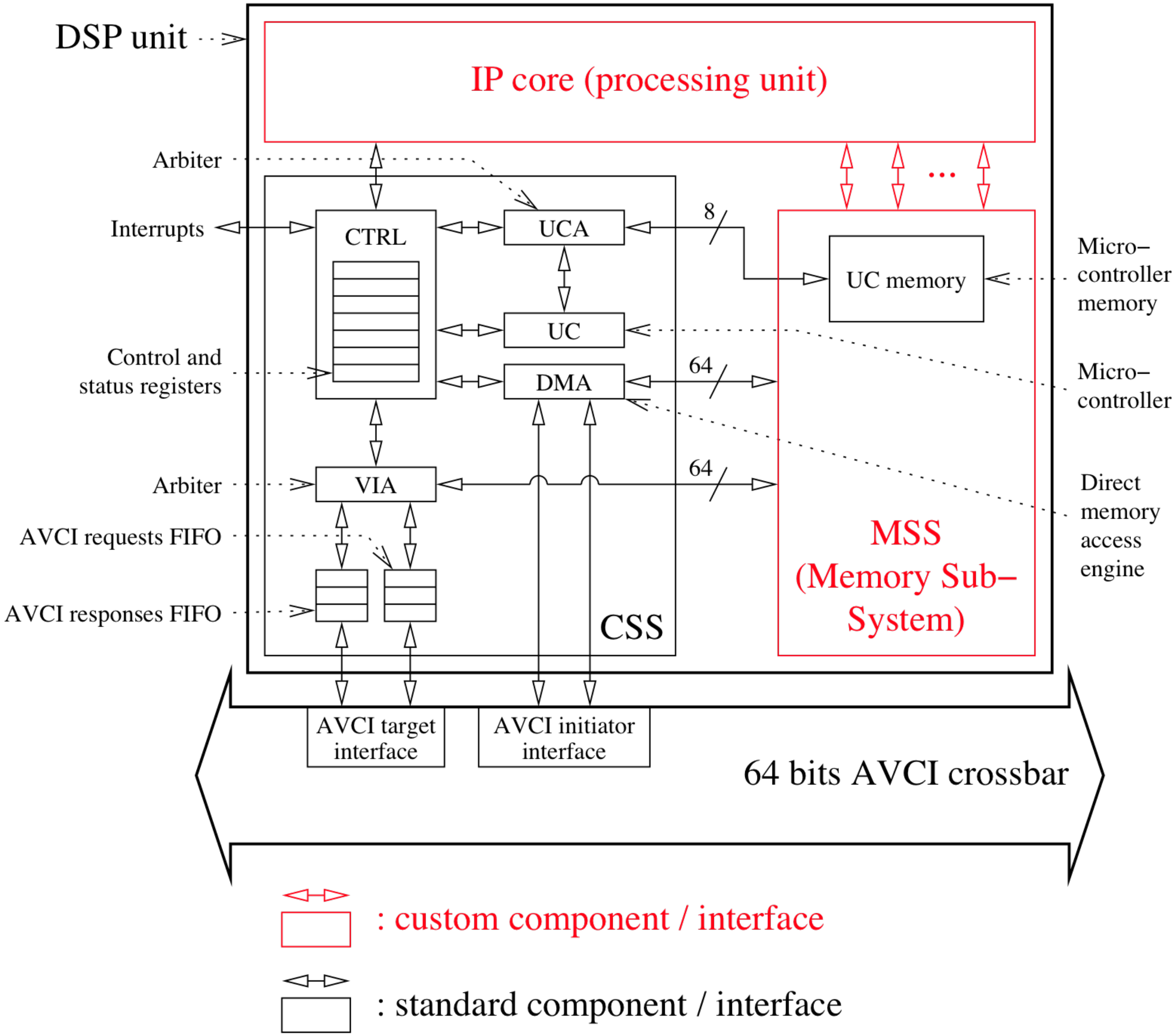
Our proposal for a flexible baseband processing



Standardized DSP unit architecture

- The designer of a DSP core concentrates on his specific problem
- Reuse of most of the system integration “glue”
- Increases the reusability of DSP units
- DSP units easily upgraded or replaced
- A generic interface with the interconnect
- A generic DMA engine
- A local micro-controller
- A mixture of standardized and custom interfaces

Standardized DSP unit architecture



Software-controlled DSP cores

- **Processing units can be driven by main CPU**
  - Memory-mapped control registers
  - Memory-mapped local memories
  - Data transfers through internal DMA (push or pull)
- **Local 8-bits µC can run sequences of processing / data transfers**
  - Channel estimation
  - Synchronization,…
- **Challenge: software design**

Agenda

- Context
- EMBB architecture
  - Selection of DSP units
  - Memory architecture
  - Interconnect
  - Control and standardized DSP unit architecture
- Examples of DSP units
- Target technologies
- Software architecture and tools

DSP units, example #1: the Front End Processor

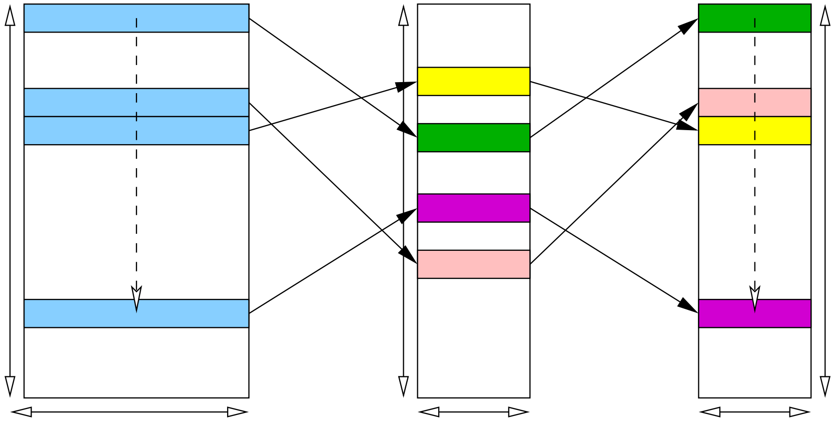
- **Operates on vectors**
  - 8 or 16 bits integers
  - 2x8 or 2x16 bits complex
- **Fancy programmable addressing schemes**
  - Repeat, skip, periodic addressing
- **Pre-post processing**
  - Type conversions, zeroing, negate, absolute value, rescaling
- **Eight (FT) or two (vector operations) components per cycle**
- **On-the-fly sum, max, min, argmax, argmin**

DSP units, example #1: the Front End Processor

- **Five instructions (192 bits VLIW)**
  - Component-wise addition
  - Component-wise product
  - Component-wise square of modulus
  - Component-wise filter by lookup table
  - Component-wise move (copy)
  - Direct and inverse Fast Fourier Transform
- **64 kBytes local MSS**
  - Four independent banks
  - 4x4096 components vectors of 2x16 bits complex

DSP units, example #2: the general purpose interleaver

- One to eight bits per symbol
- Tabulated permutation (up to 64k-entries)
- Force values
- Skip positions (multi-steps large permutations)
- Repeated values averaging



Agenda

- **Context**
- **EMBB architecture**
  - Selection of DSP units
  - Memory architecture
  - Interconnect
  - Control and standardized DSP unit architecture
- **Examples of DSP units**
- **Target technologies**
- **Software architecture and tools**

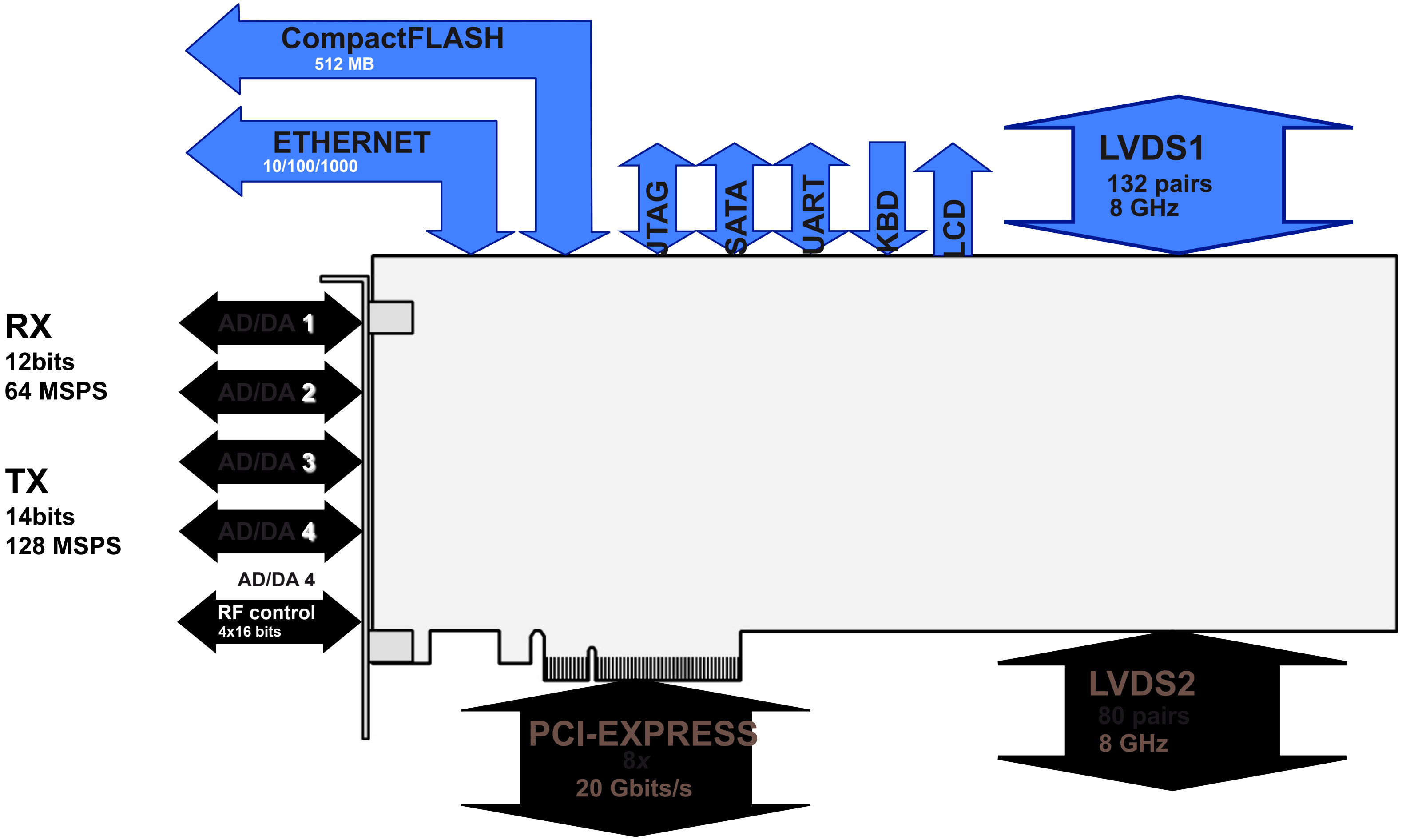
Target technologies: ExpressMIMO 1

- **FPGA-based baseband platform**
  - Virtex 5 LX330, Virtex 5 LX110T (PCIexpress)
  - 4xAD9832 (2x14-bit 128 Ms/s D/A, 2x12-bit 64Ms/s A/D)
    - Up to 8x8 MIMO capacity with low-IF, 4x4 I/Q Baseband
  - Low-jitter clock generation for converters
  - 128 Mbytes/133 MHz DDR (LX110T), 1-2 Gbytes DDR2 (LX330)
  - CompactFlash (SystemACE), JTAG Configuration
  - PCIexpress 8-way interconnect
  - LVDS expansion interface (daughter boards)
  - RF interface (micro-coax and parallel I/O for Microwire busses)

Target technologies: ExpressMIMO 1

- **LX110T**
  - Host for Gaisler Research Leon 3 Sparc Processor (maybe two), MutekH, EMBB drivers, control application
  - PCIexpress bridge to PC (8-way)/Laptop (1-way)
  - AMBA / AVCI DSP bridge to LX330
- **LX330**
  - AVCI Interconnect
  - DSP units
  - Interface to high-speed data converters

Target technologies: ExpressMIMO 1

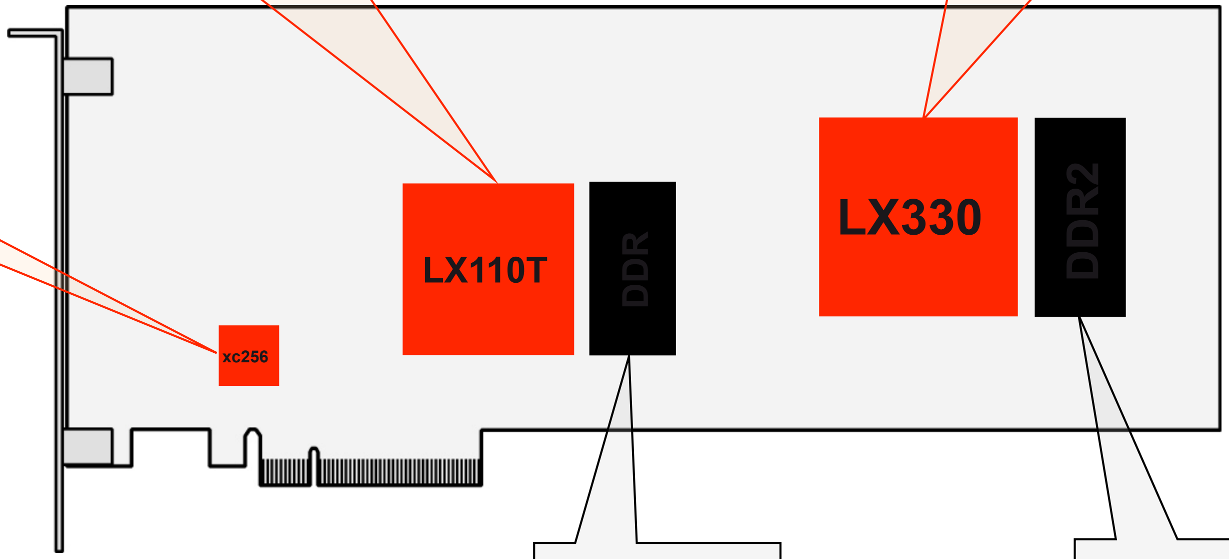


Target technologies: ExpressMIMO 1

69120	LUT
69120	Flip-Flops
64	MACs 25x18
5	Mbits SRAM
6	DCMs/PLLs
640	User IOs
+ 1	PCI-Express Endpoint
+ 1	Ethernet MAC block
+16	RocketIOs 3.2 Gbits/s

207 360	LUT
207 360	Flip-Flops
192	MACs 25x18
10	Mbits SRAM
6	DCMs/PLLs
1200	User IOs

CPLD
CoolRunner-II
xc2c256

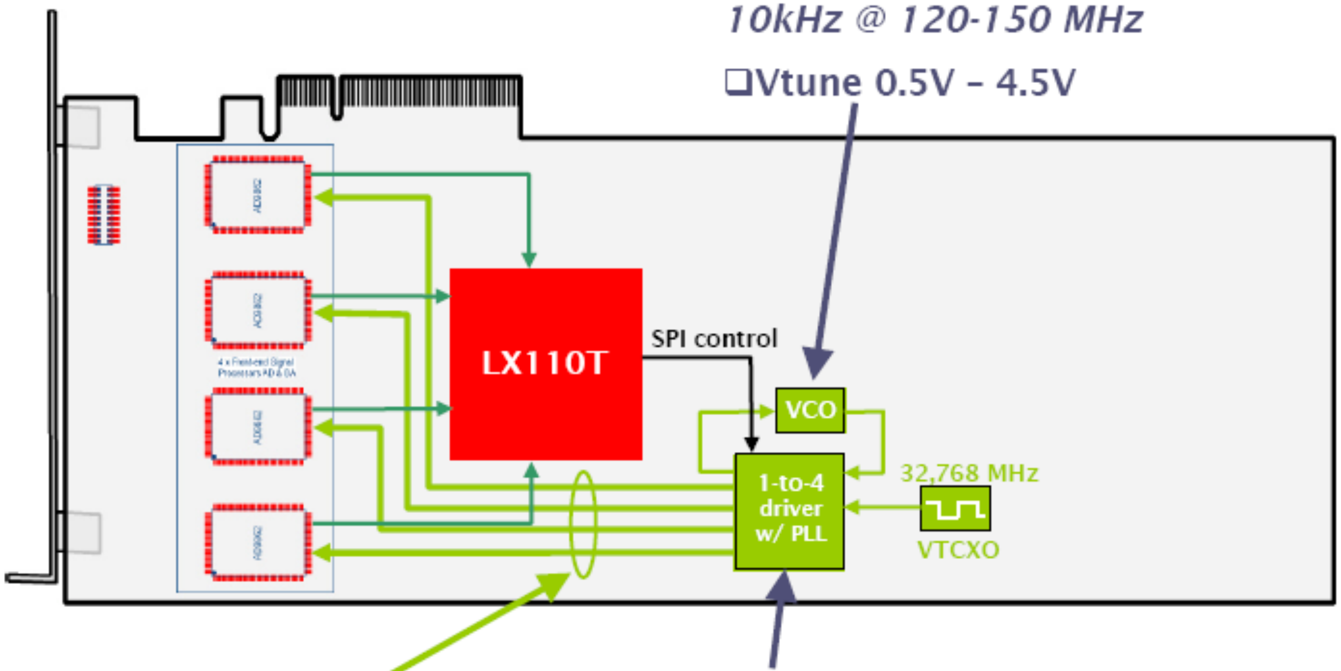


128 Mbytes
133 Mhz

1-2 Gbytes
400 Mhz

Target technologies: ExpressMIMO 1

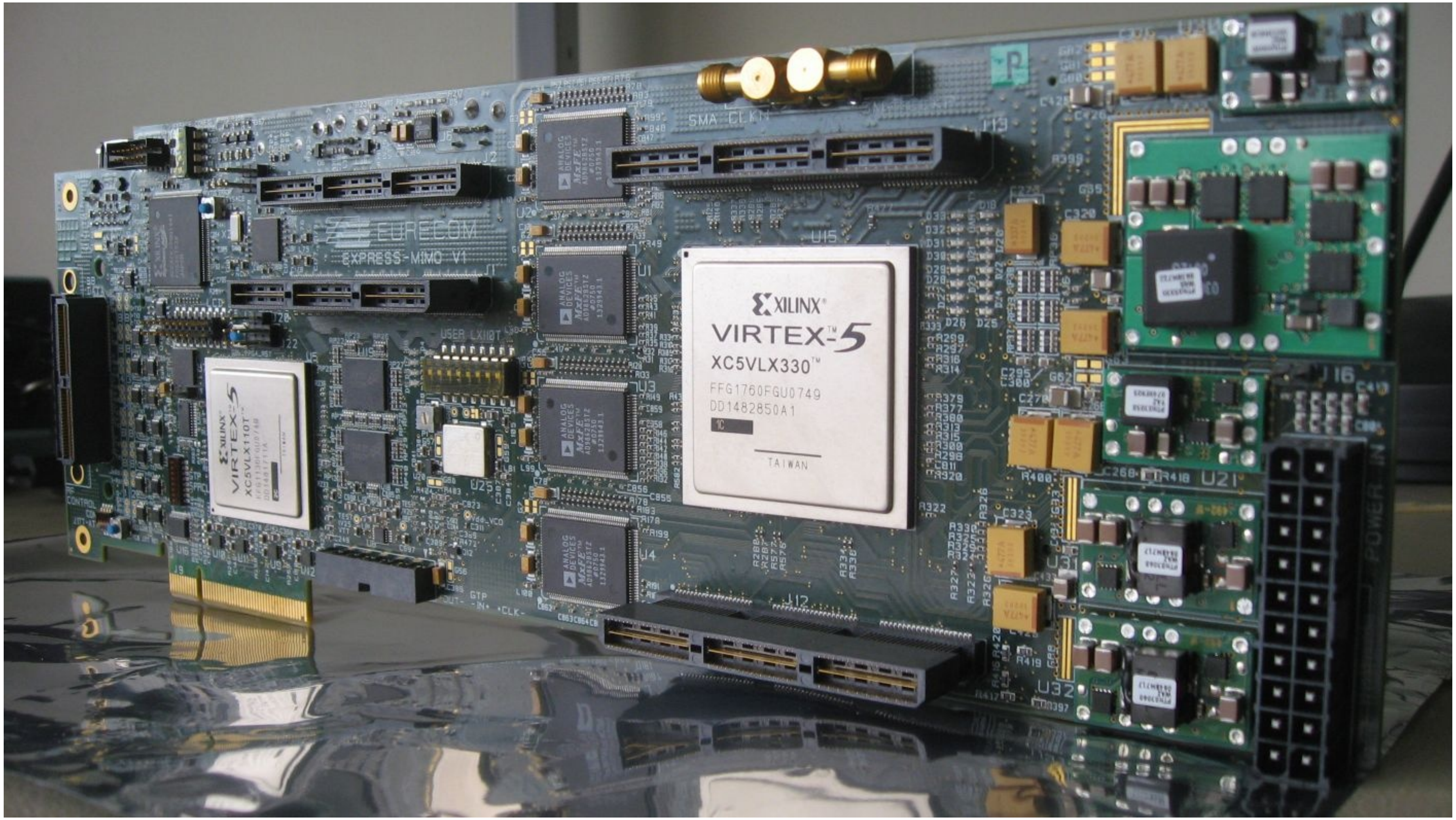
- ❑VCO with *very low phase noise, 100 dBc/Hz @ 10kHz @ 120-150 MHz*
- ❑Vtune 0.5V – 4.5V



Adjustable *from 1 MHz to 60 MHz with very low phase noise*

- ❑1-to-8 clock driver with internal PLL & *very low output phase noise contribution (-138dBc/Hz @10Hz offset @ 61.44 MHz)*
- ❑ *Programmable divider from 1 to 32*

Target technologies: ExpressMIMO 1

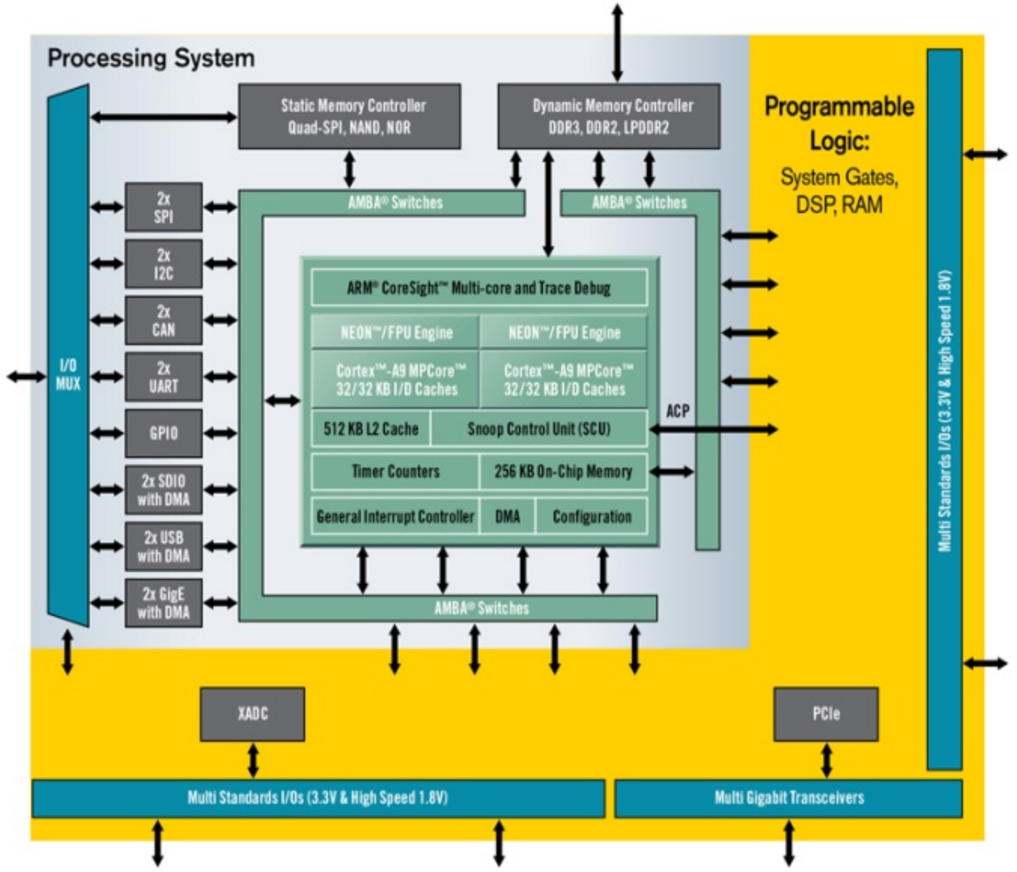


Target technologies: 40 nm SoC

- **Main outcome of SYMPA project (SCS cluster)**
- **Cancelled**
  - No support from STMicroelectronics
  - No true dual port embedded SRAMs
  - No LPDDR controller
  - No clock generator / manager
- **Replaced by yet another FPGA-based target…**

Target technologies: ExpressMIMO 3?

- Zynq70x0 (Q4 2012 / Q1 2013)



- Dual ARM Cortex™-A9 MPCore
  - Up to 800MHz
  - Enhanced with NEON Extension and Single & Double Precision Floating point unit
  - 32kB Instruction & 32kB Data L1 Cache
- Unified 512kB L2 Cache
- 256kB on-chip Memory
- DDR3, DDR2 and LPDDR2 Dynamic Memory Controller
- 2x QSPI, NAND Flash and NOR Flash Memory Controller
- 2x USB2.0 (OTG), 2x GbE, 2x CAN2,0B 2x SD/SDIO, 2x UART, 2x SPI, 2x I2C, 4x 32b GPIO
- AES & SHA 256b encryption engine for secure boot and secure configuration
- Dual 12bit 1Msps Analog-to-Digital converter
  - Up to 17 Differential Inputs
- Advanced Low Power 28nm Programmable Logic:
  - 28k to 235k Logic Cells (approximately 430k to 3.5M of equivalent ASIC Gates)
  - 240kB to 1.86MB of Extensible Block RAM
  - 80 to 760 18x25 DSP Slices (58 to 912 GMACS peak DSP performance)
- PCI Express® Gen2x8 (in largest devices)
- 154 to 404 User IOs (Multiplexed + SelectIO™)
- 4 to 12 12.5Gbps Transceivers (in largest devices)

Agenda

- **Context**
- **EMBB architecture**
    - Selection of DSP units
    - Memory architecture
    - Interconnect
    - Control and standardized DSP unit architecture
- **Examples of DSP units**
- **Target technologies**
- **Software architecture and tools**

Software architecture

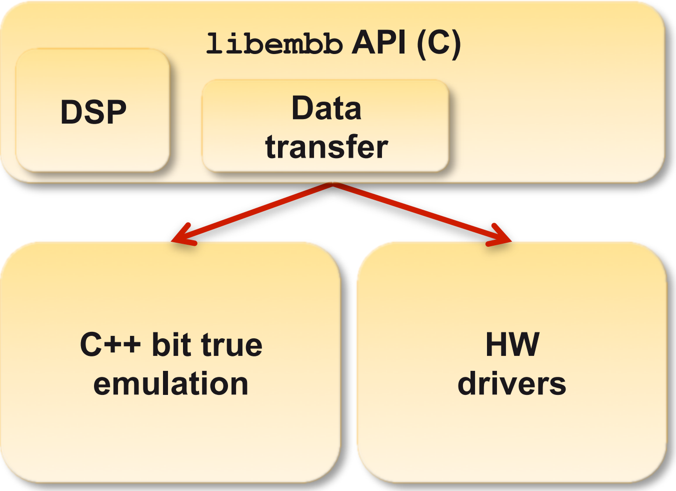
- **The most powerful processor is useless without software design tools**
- **API:** `libembb`
  - Basic commands for both main and local μCs
  - Macros
  - Synchronization and signalling
  - Data transfers
- **UML-based tools**
  - Simulation
  - Formal verification
  - Generation of software skeleton
- **SystemC bus cycle accurate simulation models**

Software architecture

- **Four baseband processing layers**
  - Basic commands (DFT, Viterbi, I/Os, …)
  - Macros (channel estimation, …)
  - Full control of a single interface
  - Interleaving of several interfaces
- **Three kinds of execution nodes**
  - Hardware DSP cores run basic commands
  - Embedded μC in DSP units run macros
  - Main CPU controls the whole processing and interfaces with MAC and upper layers
    - MutekH-based RTOS

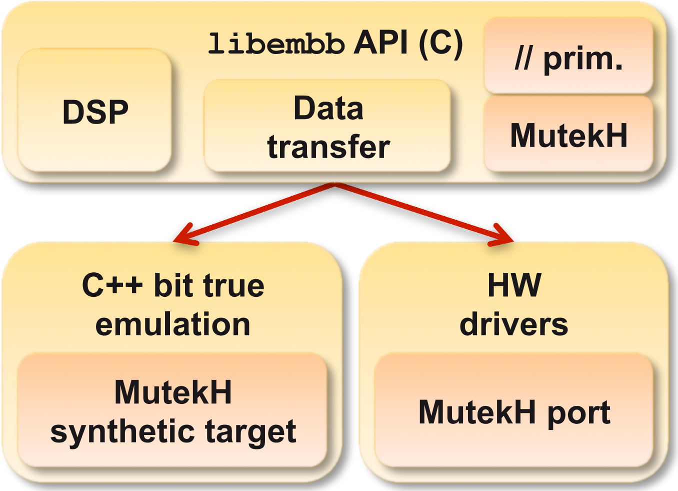
`libembb` (1/2)

- An open-source software library (CeCILL license)
- C-language API for DSP processing
  - DSP functions
    - `DFT(hndl1, dest, src, length, ...);`
    - `CWP(hndl2, dest, src1, src2, length, ...);`
  - Data transfer
    - `MEM2IP(hndl3, dest, src, length, ...);`
  - Two implementations
    - C++ emulation layer
    - C-language HW-dependent drivers



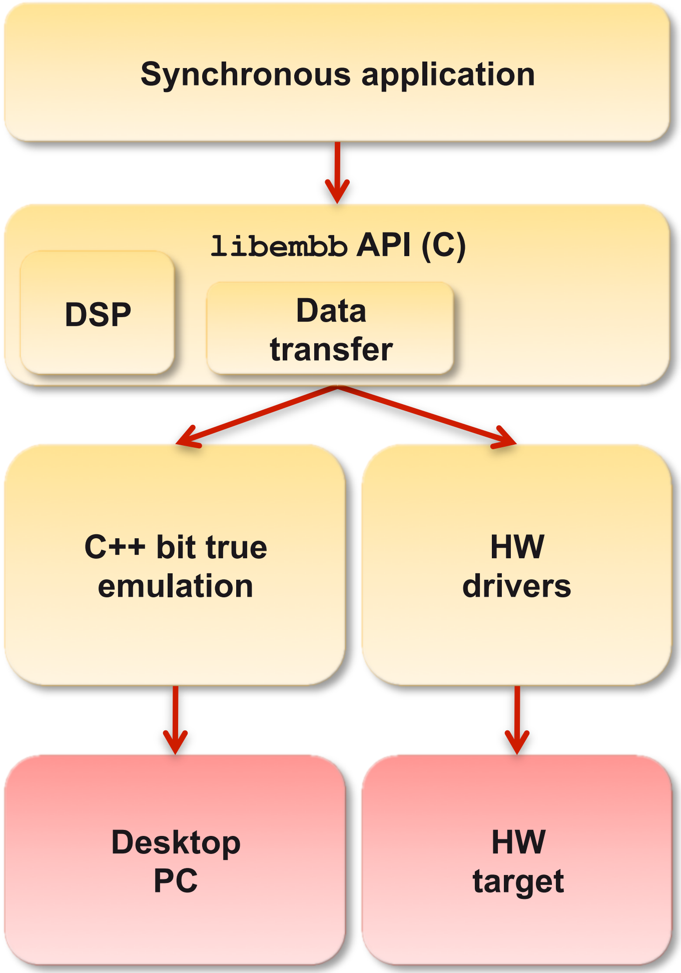
`libembb` (2/2)

- A set of primitives (on top of MutekH exo-kernel) for parallel programming
  - Timers, interrupts, schedulers,...
  - Synchronization
    - **`wait`**`(hndl1);`
    - **`wait_or`**`(hndl1, hndl2);`
    - **`wait_and`**`(hndl1, hndl2);`
- Documentation
- Examples
- Tests



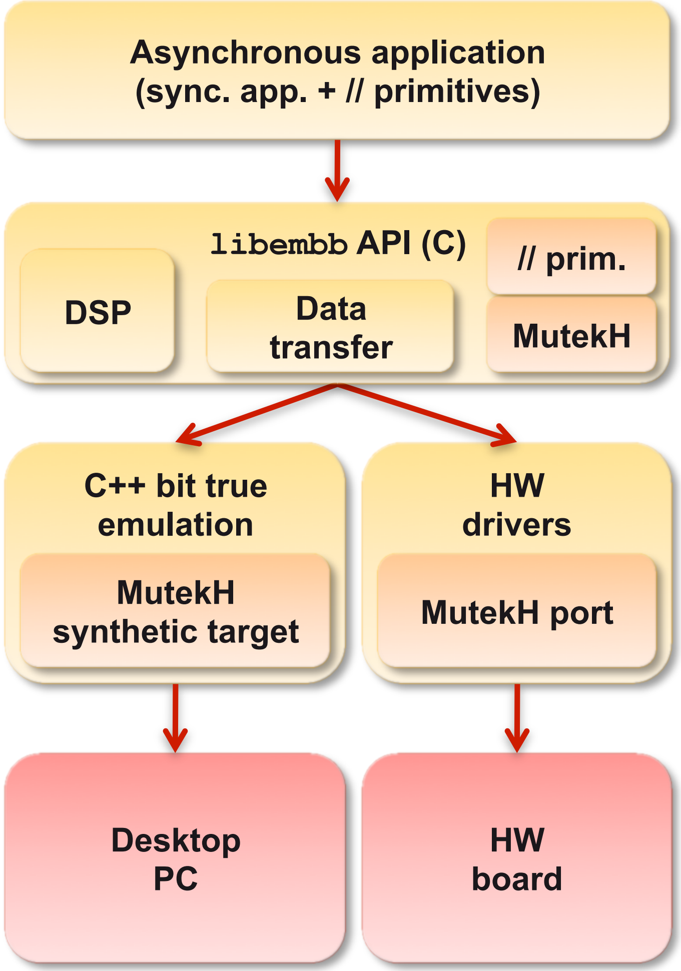
libembb usages (1/2)

- **Algorithms designs and programmer's view debugging**
  - No parallelism ("synchronous" mode), memory managed
  - Application design with C-API
  - Bit-true emulation on desktop PC (C++ emulation layer)
  - Run unmodified on HW hardware target (drivers layer)
  - Already used for hardware / software debugging, test generation, ...



libembb usages (2/2)

- **Parallel application debugging**
  - Parallelism added (C-API, parallel primitives), scheduled application
  - Multi-threaded, bit-true emulation on desktop PC (C++ emulation layer, MutekH synthetic target)
    - Possibly parallelized on multi-CPU, multi-core targets
  - Cannot explore all possible interleaving
  - Behaviour on actual HW target can be different
- **Final application**
  - Run unmodified on HW hardware target (drivers layer)

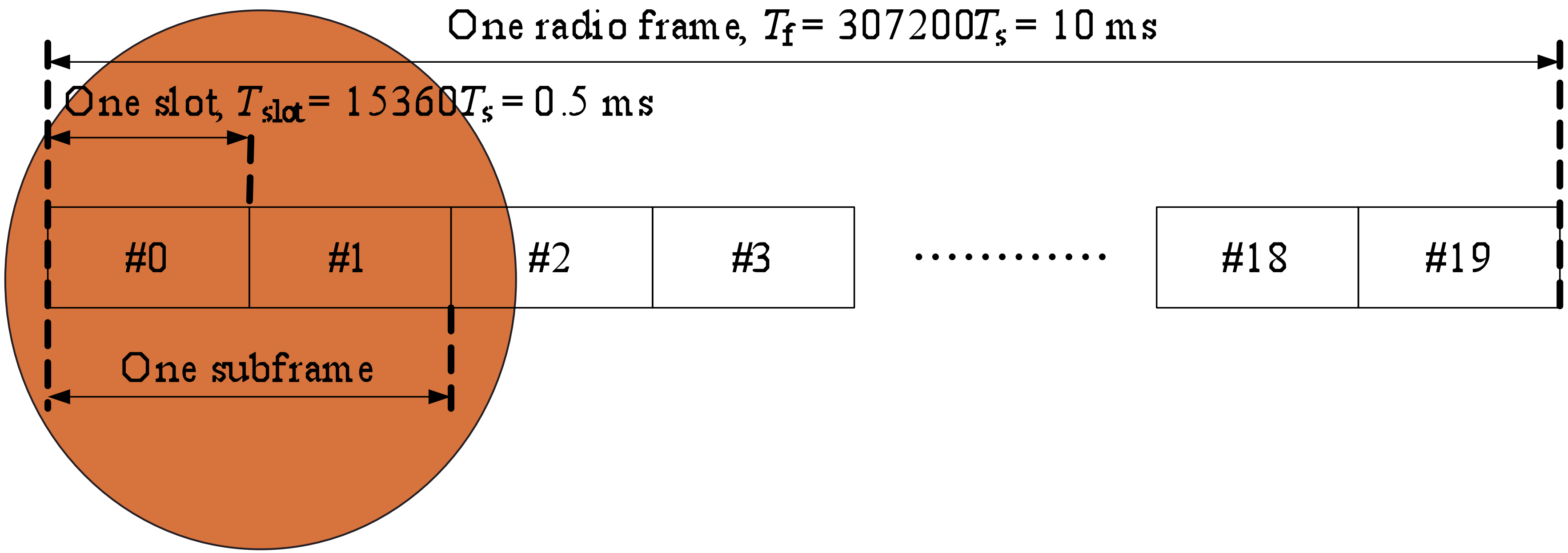


Thanks for your attention

LTE test case

- LTE is the evolving 4G standard (WCDMA -> OFDMA)
- Worst case: Up to 20 MHz baseband bandwidth and 4x4 MIMO (critical throughputs)
- Here 2 antenna UE RX
  - RX Sample throughput at preprocessor input (2 antenna terminal, 2x10-bits A/D (I/Q) @ 61.44 Ms/s => 2457.6 Mbits/s!!!!!
  - Preprocessor output 16-bits @ 30.72 Ms/s (full-bandwidth) => 1966.1 Mbits/s
  - Preprocessor output 16-bits @ 1.08 Ms/s (BCH only in unconnected mode, 99% of the time) => 61.44 Mbits/s
  - => FFT engine running at minimum 69.20 Mbits/s, maximum 1966.1 Mbits/s
- Turbo Decoder running at peak 150 Mbits/s
  - Current single-instance openair0 turbo decoder: 50 Mbits/s/iteration in 2% of LX330 => 24 % of LX330 for 6 iterations!

LTE Frame structure



One radio frame, $T_f = 307200T_s = 10$ ms

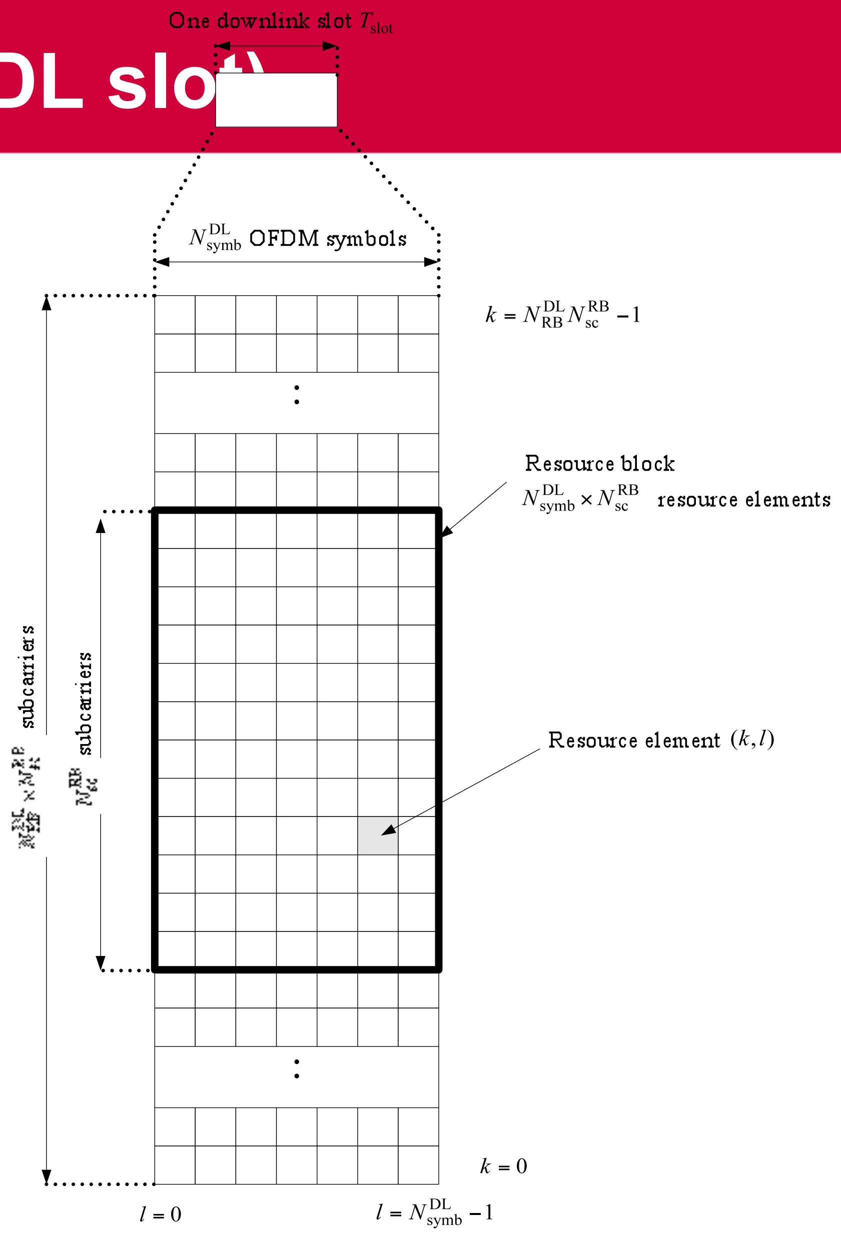
One slot, $T_{slot} = 15360T_s = 0.5$ ms

#0 #1 #2 #3 .... #18 #19

One subframe

Granularity window of PHY control (1ms) => complete demodulation
Sequence can be changed on this timescale -> tight RT constraints on OS and Inter-IP communication (10ms in UMTS, 5 ms in WIMAX)

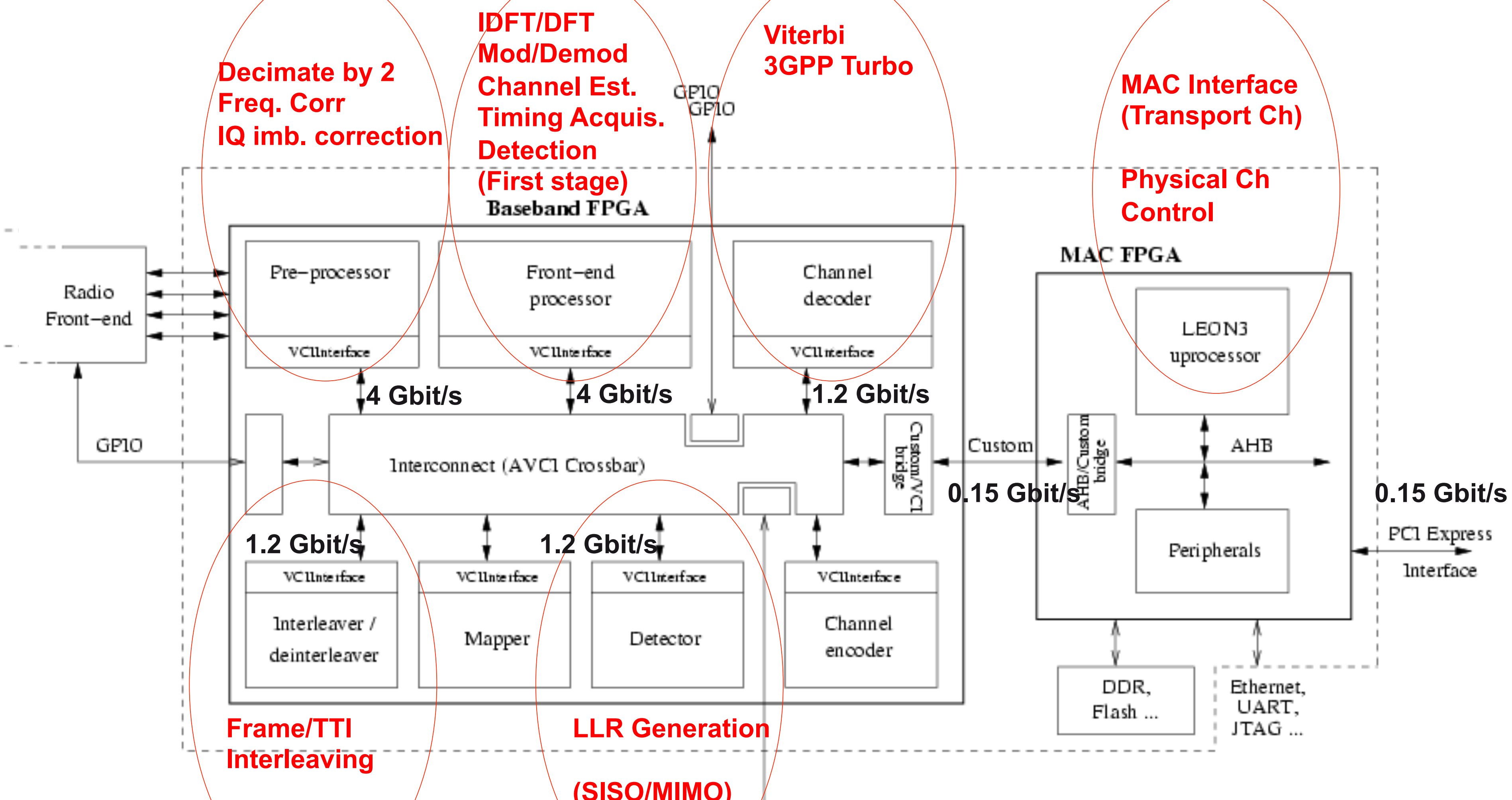
LTE Frame (DL slot)


One downlink slot T_{slot}
$N_{\text{symb}}^{\text{DL}}$ OFDM symbols
$k = N_{\text{RB}}^{\text{DL}} N_{\text{sc}}^{\text{RB}} - 1$
Resource block
$N_{\text{symb}}^{\text{DL}} \times N_{\text{sc}}^{\text{RB}}$ resource elements
Resource element (k, l)
$N_{\text{RB}}^{\text{DL}} \times N_{\text{sc}}^{\text{RB}}$ subcarriers
$N_{\text{sc}}^{\text{RB}}$ subcarriers
$k = 0$
$l = 0$
$l = N_{\text{symb}}^{\text{DL}} - 1$

OFDM symbol allocations for a particular user (receiver) can be sparse (OFDMA) -> need efficient memory access for DSP for sub-bands (FEP)

2048 carriers -> 110 RBs can be allocated arbitrarily every ms!
Not like a WIFI receiver!

Mappings and Throughput



Decimate by 2
Freq. Corr
IQ imb. correction

IDFT/DFT
Mod/Demod
Channel Est.
Timing Acquis.
Detection
(First stage)

Viterbi
3GPP Turbo

MAC Interface
(Transport Ch)

Physical Ch
Control

Frame/TTI
Interleaving

Rate Matching

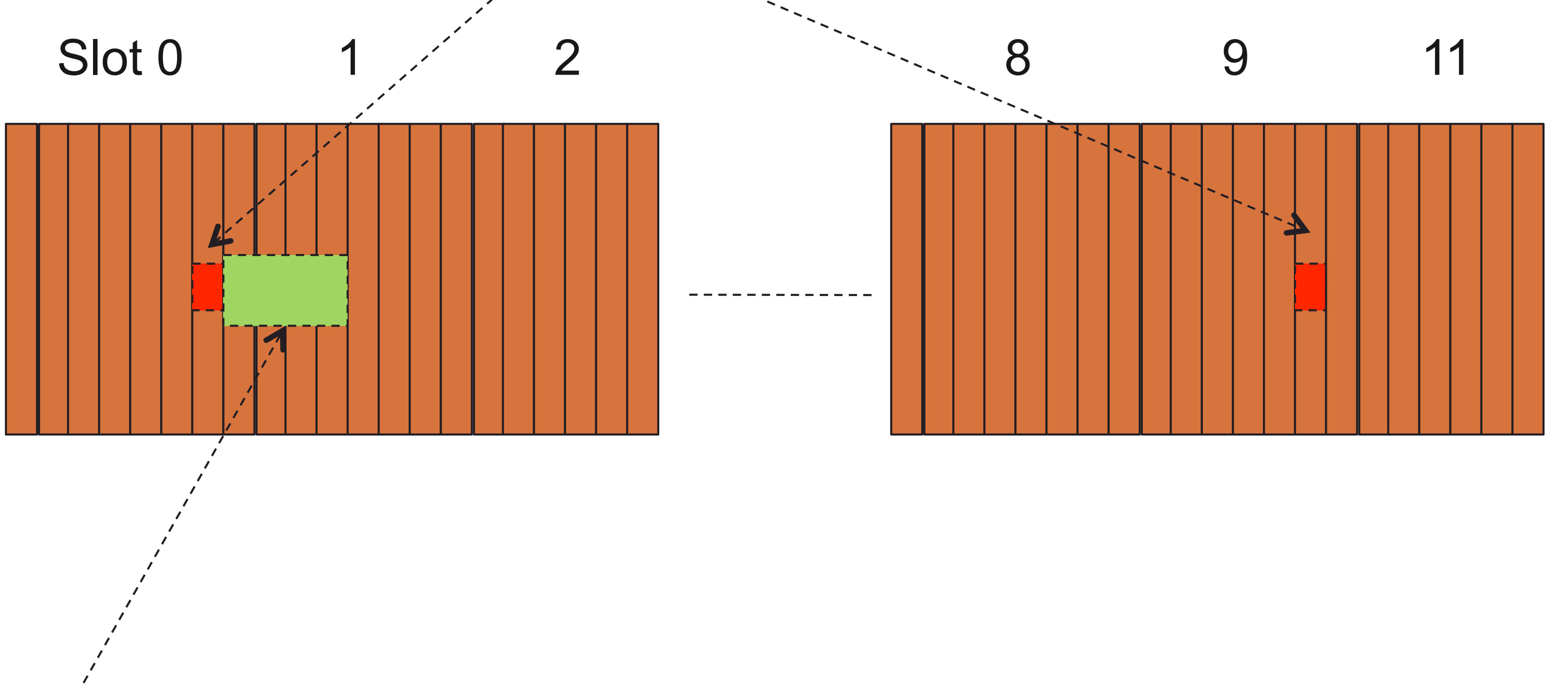
LLR Generation

(SISO/MIMO)

250 MHz 64-bit VCI = 16 Gbit/s
(tight !! -> large local memory in FEP/Cl

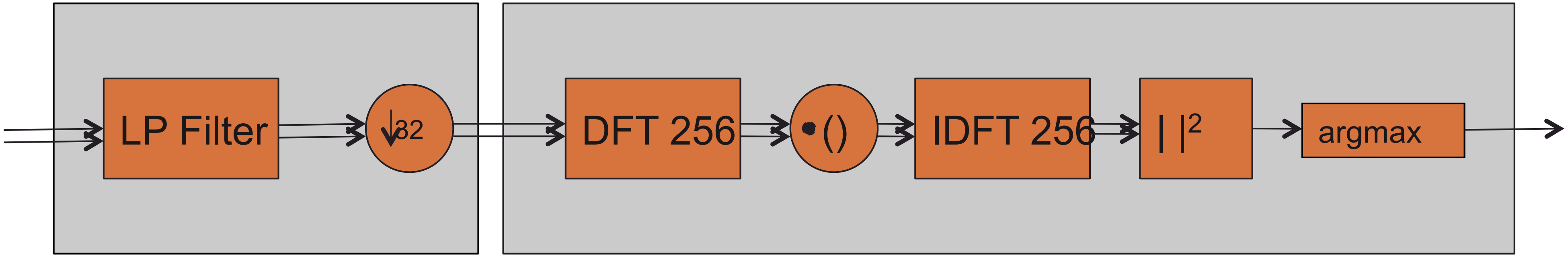
Some RX examples

- **Cell timing acquitision**
  - LTE uses “synchronization” signals (960 kHz BW), 62 resource elements (carriers)



BCH (6 RBs, 4 symbols, 1 per frame)

Some RX Examples (contd)



Preprocessor

Front-end Processor

Some RX Examples

- Channel Estimation across contiguous RBs

IDROMel platform performances

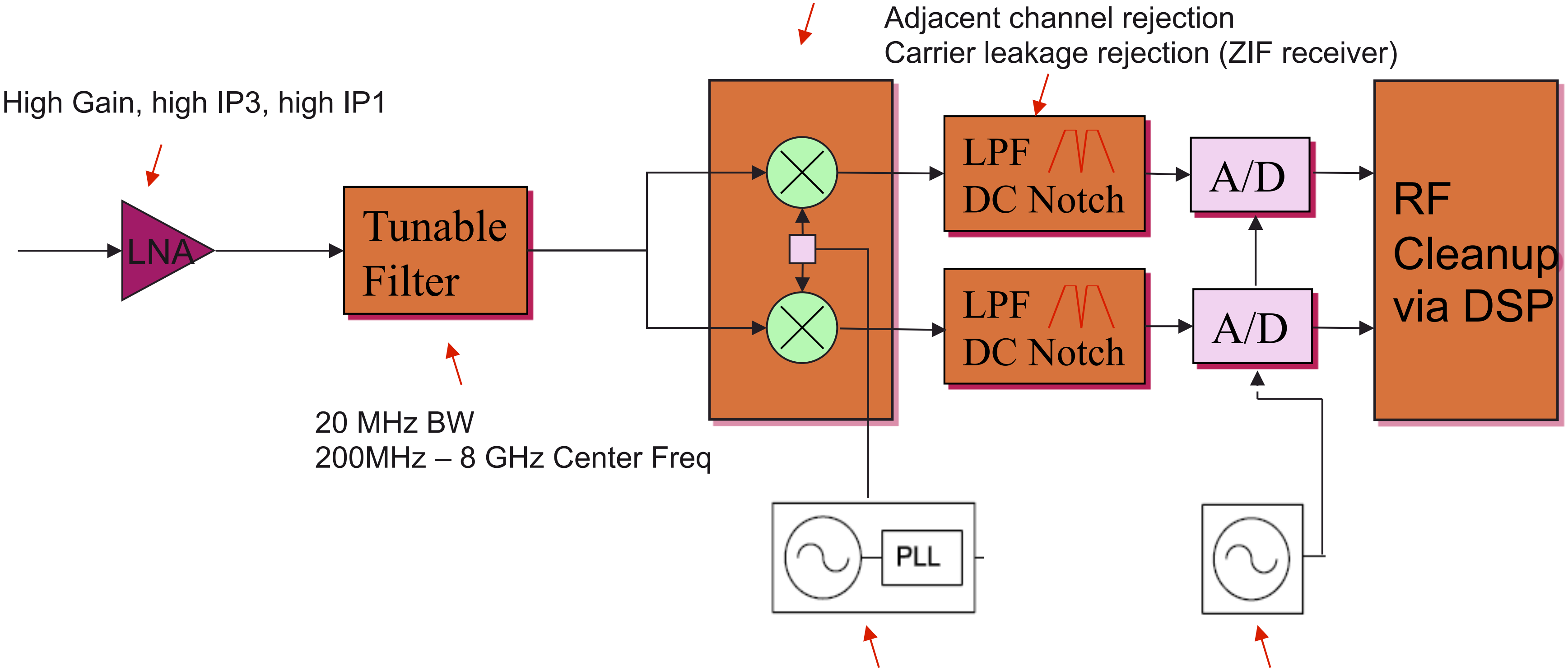
- 2 RATs
  - 3G (-like)
  - LTE (-like)
- Any other OFDM-based and/or CDMA-based RAT in the medium term
- Any frequency carrier from 200 MHz to 7.5 GHz
- Any BW till 20 MHz
- Vertical hand-over scenarios
- SISO, 2X2 MIMO or 4x4 MIMO
- Complete reconfigurability

Agile-RF

Agile-RF

- Ability to tune across large bandwidths (200 MHz – 6 GHz)
- Support both TDD and FDD
- Handle both narrowband (200 kHz) and wideband channels (20 MHz)
- Technologies
  - broadband antennas
  - reconfigurable analog filters (e.g. MEMS) -> bandselection/ interference rejection
  - Broadband linear amplifiers and image-reject (quadrature) mixers
  - Broadband VCO/PLL
  - High dynamic-range ADCs (to allow for digital interference rejection and advanced baseband processing)

Target Broadband RF Receiver (IdroMel/E2R2)



High linearity quadrature (image-reject) mixer (high IP3, IP1)
Excellent I/Q balance over whole frequency range

Adjacent channel rejection
Carrier leakage rejection (ZIF receiver)

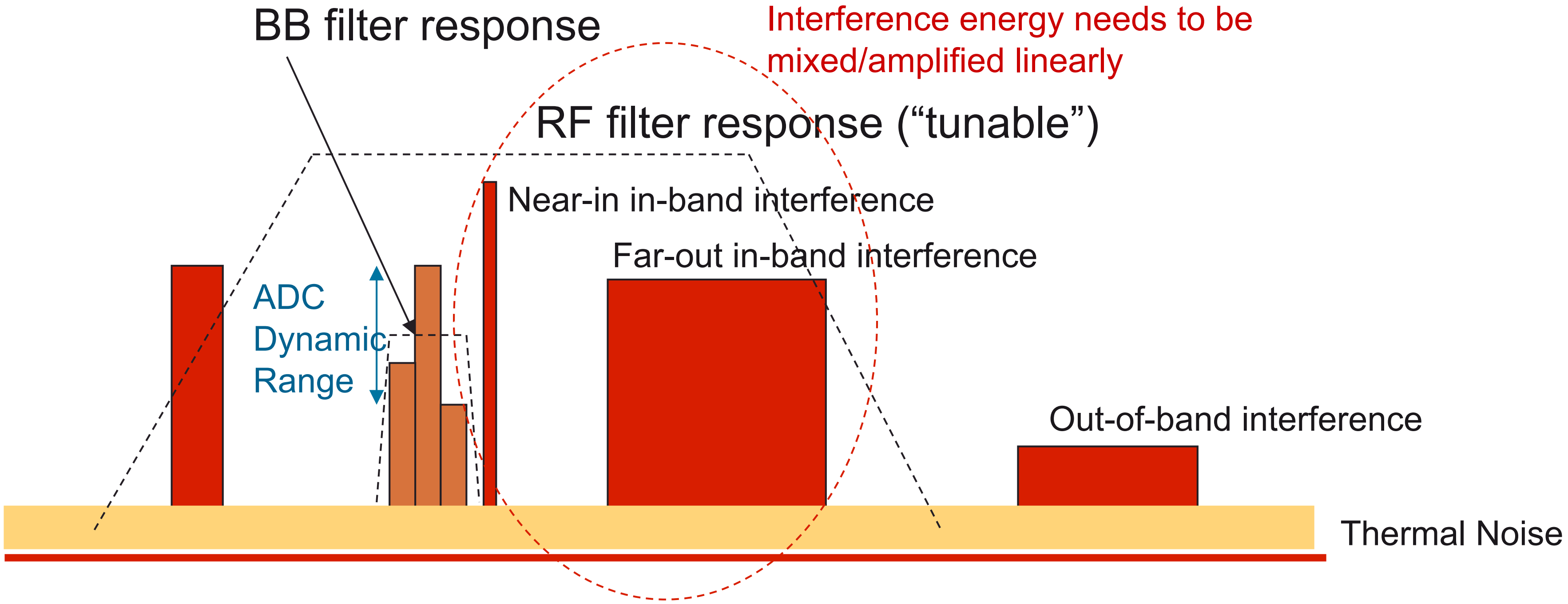
High Gain, high IP3, high IP1

20 MHz BW
200MHz – 8 GHz Center Freq

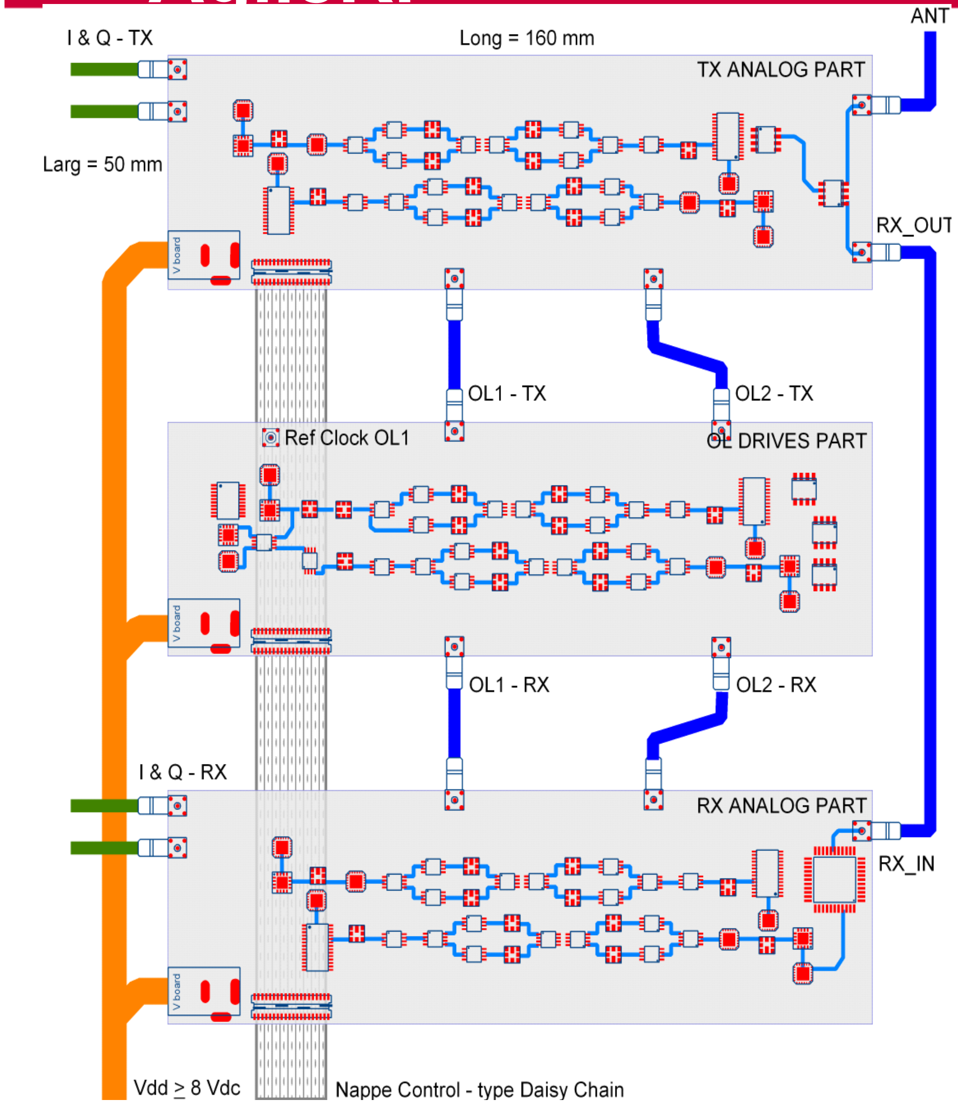
200MHz-8GHz synthesiszer

30 MHz TCXO

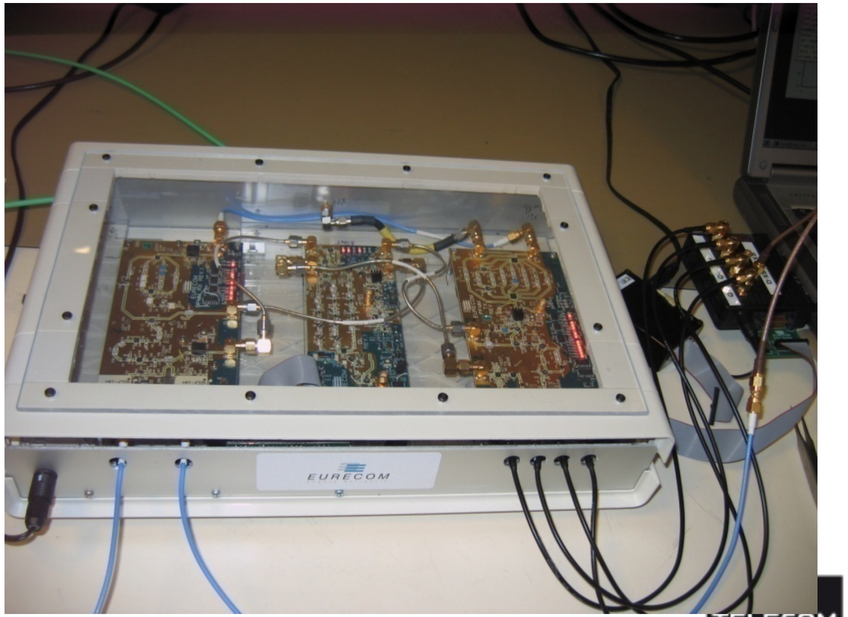
Importance of Linearity over Large Dynamic Range


BB filter response
Interference energy needs to be mixed/amplified linearly
RF filter response ("tunable")
Near-in in-band interference
Far-out in-band interference
ADC Dynamic Range
Out-of-band interference
Thermal Noise

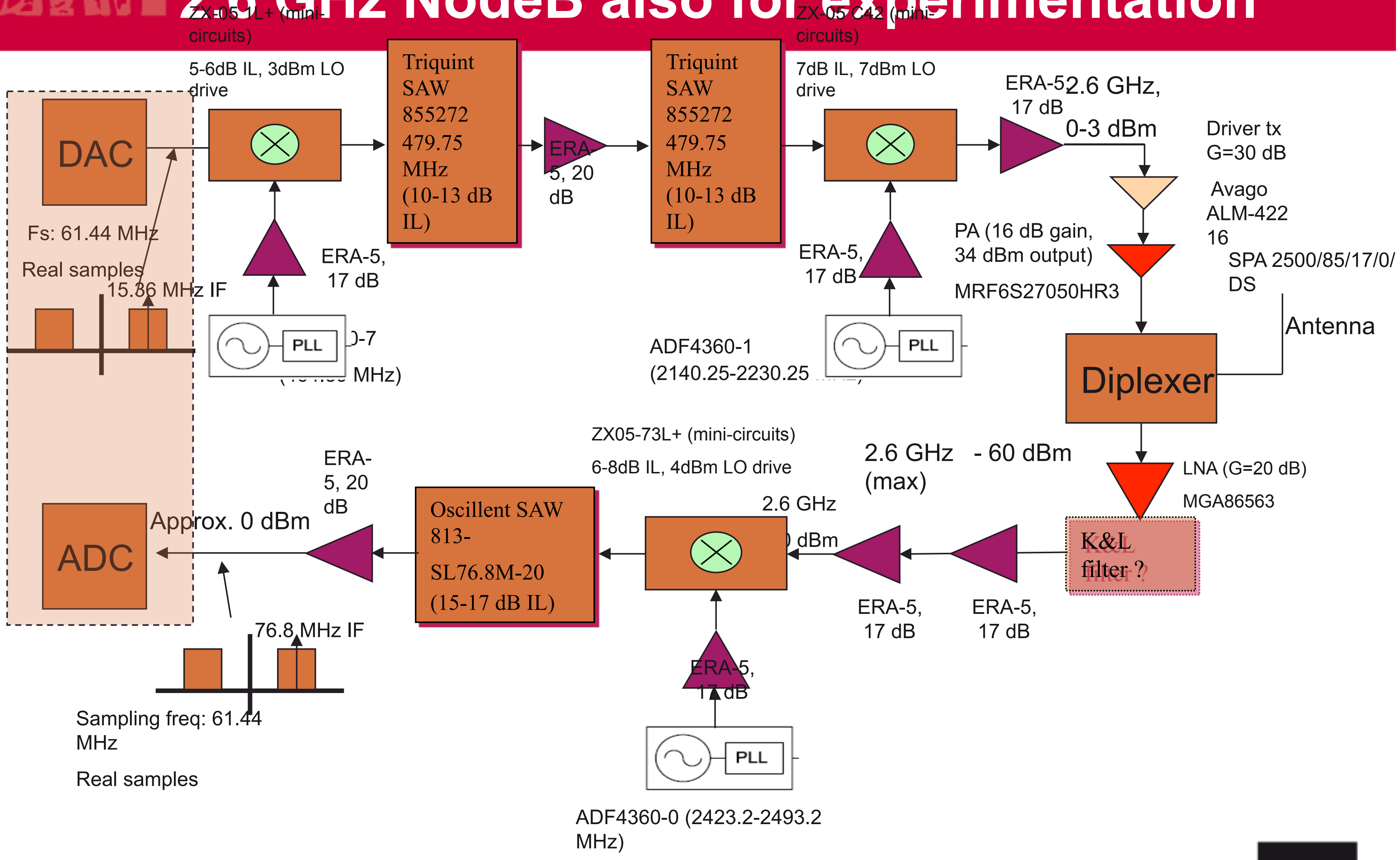
AgileRF



- **Characteristics:**
  - Frequency band: 200 MHz – 7.5 GHz
  - 500 kHz raster
  - Baseband channel BW: 20 MHz
  - Tx : +15 dBm (35 dB ACLR)
  - Rx NF : 8 dB



2.6 GHz NodeB also for experimentation



ZX-05 1L+ (mini-circuits)

5-6dB IL, 3dBm LO drive

DAC

Fs: 61.44 MHz

Real samples

15.36 MHz IF

ERA-5, 17 dB

)-7

MHz)

Triquint SAW 855272 479.75 MHz (10-13 dB IL)

ERA-5, 20 dB

Triquint SAW 855272 479.75 MHz (10-13 dB IL)

ZX-05 C42 (mini-circuits)

7dB IL, 7dBm LO drive

ERA-5, 17 dB

ADF4360-1 (2140.25-2230.25

ERA-5 17 dB

2.6 GHz, 0-3 dBm

Driver tx G=30 dB

Avago ALM-422 16

PA (16 dB gain, 34 dBm output)

MRF6S27050HR3

SPA 2500/85/17/0/DS

Antenna

Diplexer

LNA (G=20 dB)

MGA86563

K&L filter ?

2.6 GHz (max)

- 60 dBm

ERA-5, 17 dB

ERA-5, 17 dB

2.6 GHz

) dBm

ZX05-73L+ (mini-circuits)

6-8dB IL, 4dBm LO drive

ERA-5, 17 dB

ADF4360-0 (2423.2-2493.2 MHz)

Oscillent SAW 813-SL76.8M-20 (15-17 dB IL)

ERA-5, 20 dB

Approx. 0 dBm

ADC

76.8 MHz IF

Sampling freq: 61.44 MHz

Real samples

Difficulties

- **Synthesizer**
  - Broadband is hard to design (1.9-4.1 GHz is out there, but not cheap)
  - Large range comes with reduced frequency granularity (e.g. 500 kHz) -> requires digital frequency synthesis in baseband DSP to compensate
    - Now Analog Devices + RFMicro manufacture low-cost low-power wideband VCO/PLL (high-power LO!)
- **Quadrature Mixer**
  - Drive strength for LO input
- **LNA**
  - High IP3 to allow for interference mitigation in later stages of receiver
- **Tunable filters**
  - Still research topic in electronics community (MEMS-based technologies exist, but limited to tunability over small ranges)
  - Switched filter bank is not an “integrateable” technology and will consume space
- **A/D**
  - High resolution/low-power (modern sigma-delta is a good choice with high-end DSP behind). Resolution for near-in interference mitigation in DSP.
  - Fixed sampling clock for high-quality (low jitter/phase noise) requires retiming circuit in DSP to cover the plethora of radio standards in nature.