High Speed Mixed Signal PCB Design

Some Practical Considerations

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Innovative solutions
for tomorrows challenges

Renesas Mobile Corporation

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Renesas Mobile - What We Do…

- Renesas Mobile is well placed to help customers maximise the potential of the wireless revolution by delivering ground breaking solutions that **drive the wide adoption of LTE** multi-mode devices into high volume segments from smartphones and tablets to embedded devices

- Our portfolio of solutions to OEMs and ODMs worldwide includes:-

  - Versatile and flexible **Mobile Platforms**
  - High performance **Application processors**
  - Highly integrated **Slim multi-mode cellular modems**

Renesas Mobile Pedigree

Renesas Electronics

Mobile Multimedia Business
- Global No.1 APE & Co-processor
- Global No.5 RF Device
- Most Efficient SoC Implementation Technology
- Software & Integration

Dec. 2010

Renesas Mobile

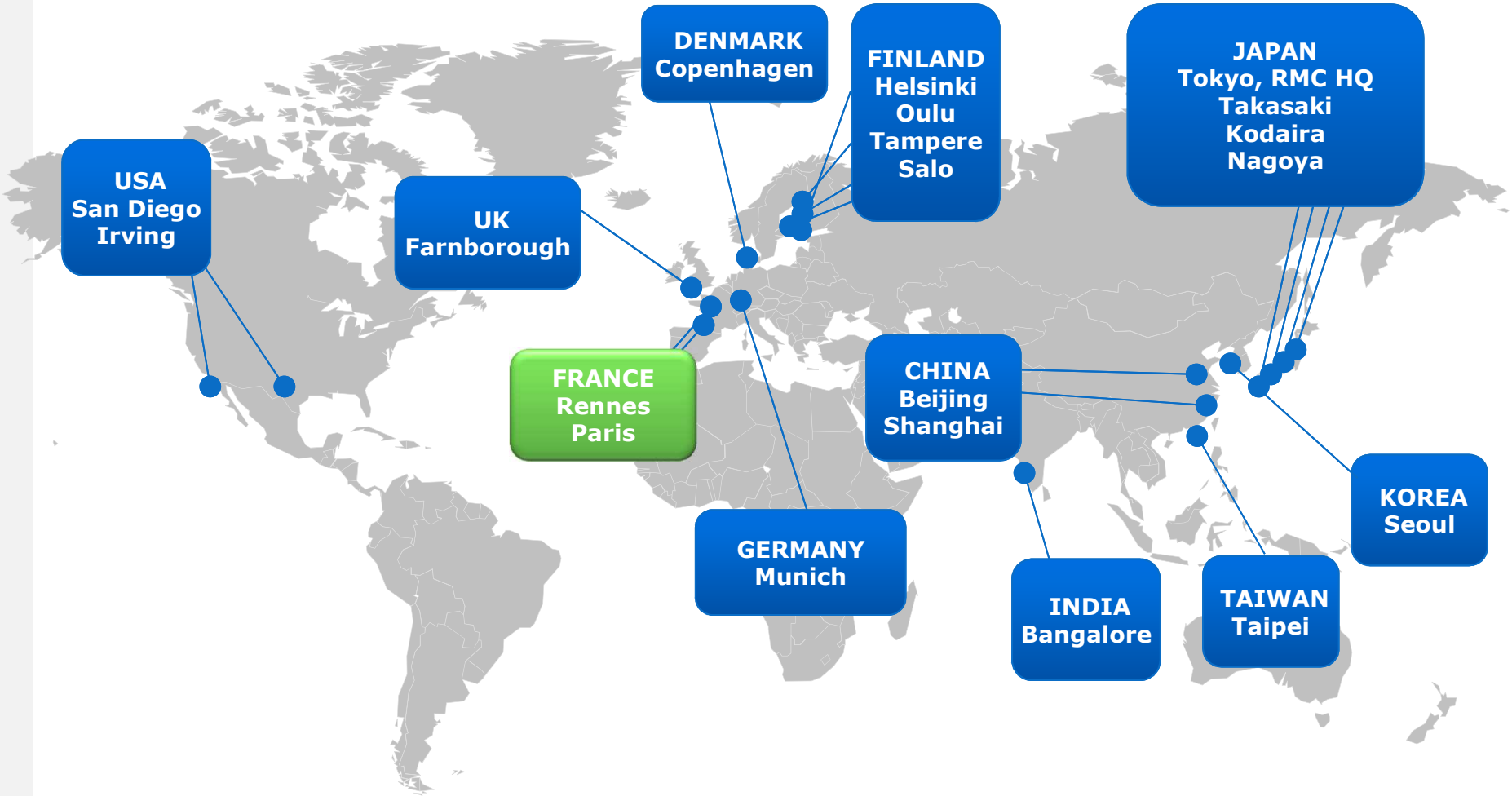
NOKIA

Wireless Modem Unit
- Most robust & Widely deployed Modem Technology
- Global Field support Infrastructure
- Strong IPR & Contributions for Standardization

- REL one of the largest Semiconductor Suppliers
- REL Created on April 1st, 2010 as the combined operations of former NEC Electronics and Renesas Technology
- REL has a consolidated turnover of around ~10B$

Legacy experience across GSM/EDGE, WCDMA/HSPA, and LTE, having shipped modems powering over 2 Billion mobile devices

Renesas Mobile's Worldwide Presence



Outline

- PCB stack-up and material losses (ε_r, tanδ, skin effect)
- Signal layers topologies and return current path
- Mixed signal design rules
  - Power and Ground stack-up
  - Ground routing rules
  - Signal routing rules
- Decoupling strategy: Frequency Domain Target Impedance Method (FDTIM)
- Decoupling placement rules
  - RF/analog ICs
  - High current power rails
- References

PCB stack-up construction

- PCB constructed from multiple alternating layers of core, prepreg and copper foil materials heat-pressed and glued together.
- Example of a 10-layers PCB stack-up

- Core:

  hardened fiber glass-weaves material with epoxy resin. It acts as an insulation layer between the copper foils.

- Prepreg:

  non-hardened fiber glass-weaves material with epoxy resin. It acts as an insulation layer between core layers and is the gluing agent for the cores

Material : LX-67Y

Layers	Type	Copper(*) (microns)	Symbol	Laminate Thickness (microns)	Preg Thickness (microns)	Laminate (mils)	Dielectric Thickness (microns)	1037	1080	3313
1	E	45	====							
					106		106	2		
2	P	17,5	----							
				130		5	130			
3	L	17,5	----							
					234		217		3	
4	P	17,5	----							
				130		5	130			
5	L	17,5	----							
					234		217		3	
6	P	17,5	----							
				130		5	130			
7	L	17,5	----							
					234		199		3	
8	L	17,5	----							
				130		5	130			
9	P	17,5	----							
					106		106	2		
10	E	45	====							
TOTAL		230		520	914		1364			

(mm)

Thickness on material	1,50
Thickness on finished copper	1,59

====		External copper
-------		Internal copper
		Preg
		Core

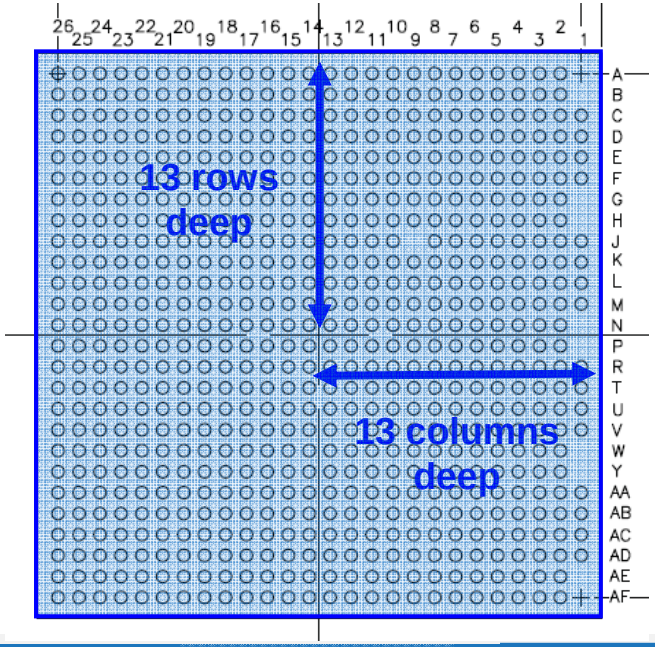
(*) : E = Base copper 9 µ + Electroplating copper
(*) : L, P ou LP = Base copper
(*) :EL,EP ou ELP = Base copper + Electroplating copper
E = External layer
L = Inner logical layer
P = Plane copper layer (Gnd or Power)
LP = Mixed layer

Signal layers: Layer count estimation

- In high density BGAs, many signal layers are required to achieve full break of all available IOs
- Estimation of the minimum number of layers N_{min} required for a balanced PCB stack-up:

$$N_{min} = \begin{cases} \left\lceil \frac{\max(\text{depth row}, \text{depth column})}{2} \right\rceil & , \text{if } \left\lceil \frac{\max(\text{depth row}, \text{depth column})}{2} \right\rceil \text{ is even} \\ \left\lceil \frac{\max(\text{depth row}, \text{depth column})}{2} \right\rceil + 1 & , \text{if } \left\lceil \frac{\max(\text{depth row}, \text{depth column})}{2} \right\rceil \text{ is odd} \end{cases}$$

- Example: Xilinx Virtex 5 SXT in a FF665 BGA package:
  - **N_{min}=8**



Material loss consideration: Relative dielectric constant ε_r

- ε_r is a measure of material's ability :
  - to be polarized by an electric field and store electrostatic energy
  - to facilitate signal propagation.
  - The higher the relative dielectric constant:
    - the slower a signal travels on a wire,
    - the lower the impedance of a given trace geometry
    - the larger the stray capacitance along a transmission line.
- ε_r is generally an inverse function of its frequency.
  - Digital signals are comprised of many harmonics
  - The impedance of a transmission line goes down as frequency goes up resulting in faster edges reflecting more than slower ones.
  - Differences in impedance for RF Broadband can cause signal loss from both reflections and phase distortion (phase jitter) arising from the different frequencies arriving at the destination at different times
- **Always choose lower ε_r material with flat frequency response for best signal performance and to minimize signal distortion and phase jitter especially for broadband RF and high speed applications**

Material loss consideration: loss tangent tan(δ)

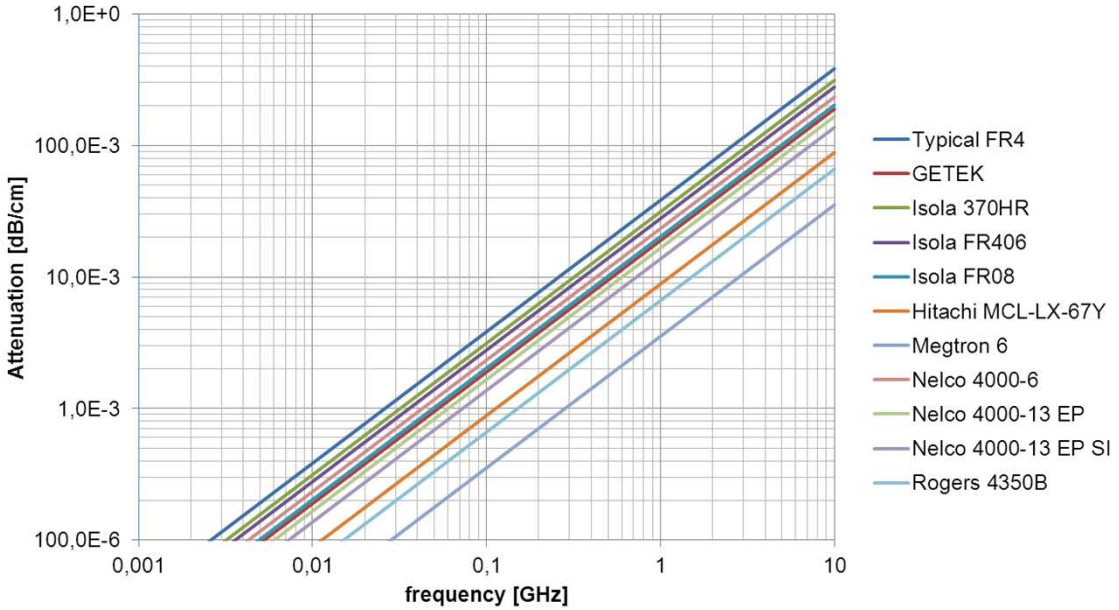
- tan(δ) is a measure of signal loss as the signal propagates down the trasmission line.
- It is the result of electromagnetic wave absorption by the dielectric material and depends on the material's structure and glass-resin composition
- **A lower tan(δ) results in more of the original transmitted signal getting through to its destination.**
- Attenuation can be calculated according to:

$$\text{Attenuation}[\text{dB.cm}] = \frac{2.3}{2.4}.f.\tan(\delta).\sqrt{\varepsilon_r}$$

  - f is the frequency in GHz
  - tan(δ) is the dimensionless loss tangent
  - ε_r is the relative dielectric constant of the material

Comparison of loss tangent attenuation

Material	ε_r	tan(δ)
Typical FR4	4	0,02
GETEK	3,9	0,01
Isola 370HR	4,17	0,016
Isola FR406	4,29	0,014
Isola FR08	3,7	0,011
Hitachi MCL-LX-67Y	3,4	0,005
Megtron 6	3,4	0,002
Nelco 4000-6	4,12	0,012
Nelco 4000-13 EP	3,7	0,009
Nelco 4000-13 EP SI	3,2	0,008
Rogers 4350B	3,48	0,0037



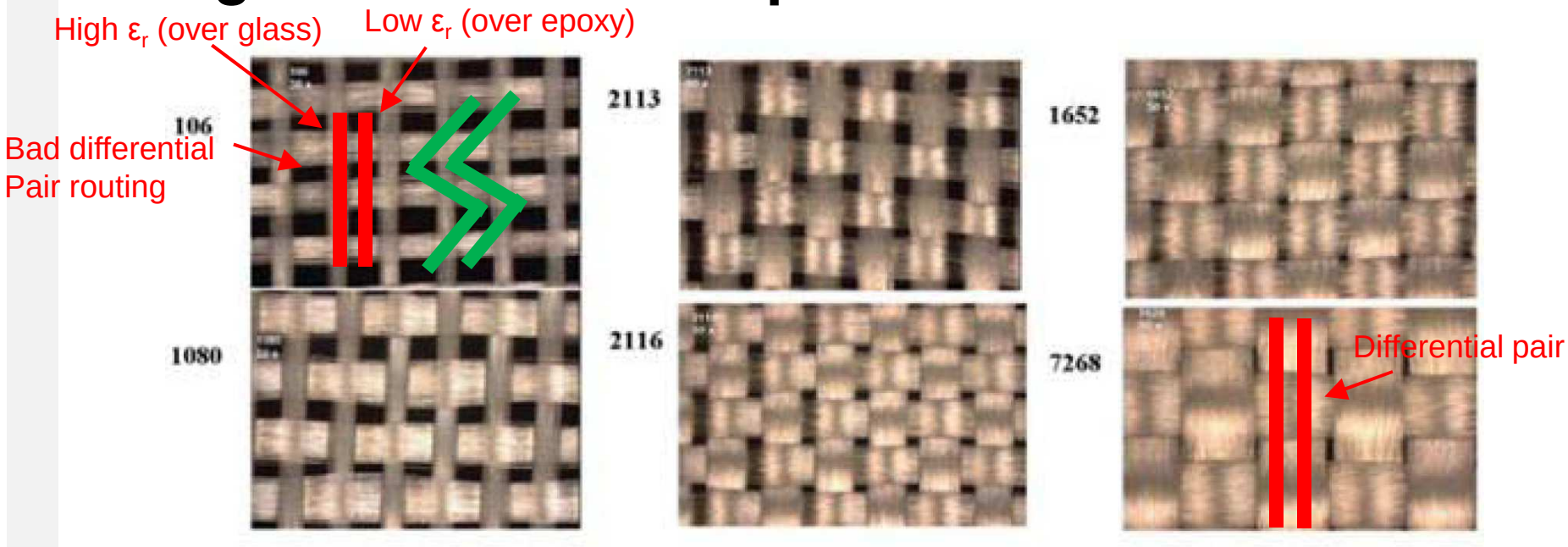
- Example:
  - Trace length 10 cm
  - Design running at 240MSps (I,Q data time interleaved)
  - Nyquist equivalent frequency is 120MHz
  - Loss due to the dielectric absorption of :
    - Typical FR4 is 0.0046dB per cm and ≈0.05dB for 10cm trace length
    - Hitachi MCL-LX-67Y is 5 times smaller and ≈0.01dB for 10cm trace length.

Material cost comparison

Material group	Vendor reference	FR4 relative cost factor
FR4 baseline	Nelco 4000-6	1
High Tg / Reliability Filled	Isola 370HR	1.1
High speed / Low loss	Isola FR08	1.8
High speed / Low loss	Nelco 4000-13 EP	2.1
High speed / Very low loss	Hitachi MCL-LX-67Y	3
High speed / Very low loss	Nelco 4000-13 EP SI	3.2
High frequency	Megtron 6	5
High frequency	Rogers 4350B	5.6

- Hitachi MCL-LX-67Y is the good trade-off between performance and cost for high speed and very low loss application.

Fiberglass weaves composition



- The tighter the weave netting the more uniform the dielectric constant
- On a sparse weaving, one leg of the differential pair may be routed directly over a fiber weave while the other leg is routed between the fiber weaves.
  - This result in different ε_r for each leg of the differential pair
  - Loose weaves can cause trace impedance variations and propagation skew in tightly matched signal such as differential pairs

Skin effect (1)

- In addition to dielectric absorption, signal attenuation can also occur because of resitive losses from the copper trace.
- DC copper trace resistance

$$R_{DC} = \rho \frac{L}{A}$$

  - ρ: resistivity of the copper: $1{,}68.10^{-11}\Omega.mm$
  - L: trace length in mm
  - A: cross-section area of the trace in mm^2

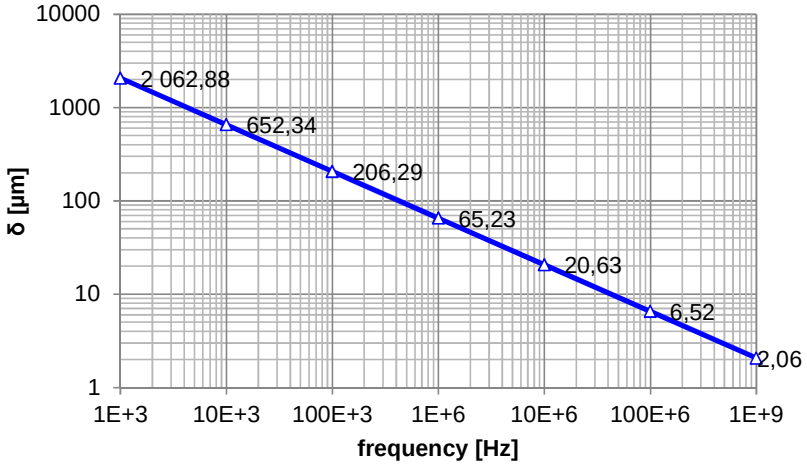
- Increasing frequency, the resistive channel increase because current flows through the surface of the copper trace.
- The surface penetration of the current flow is referred to as the skin depth (δ).
- The skin effect reduces the cross section area of the copper trace
- **Countering this effect typically requires widening the tracewidth to increase the surface area.**

Skin effect (2)

- Skin depth

$$\delta = \sqrt{\frac{\rho}{\pi.\mu_0.\mu_r}}.\sqrt{\frac{1}{f}} \approx 65{,}23.10^{-3}\sqrt{\frac{1}{f}}$$

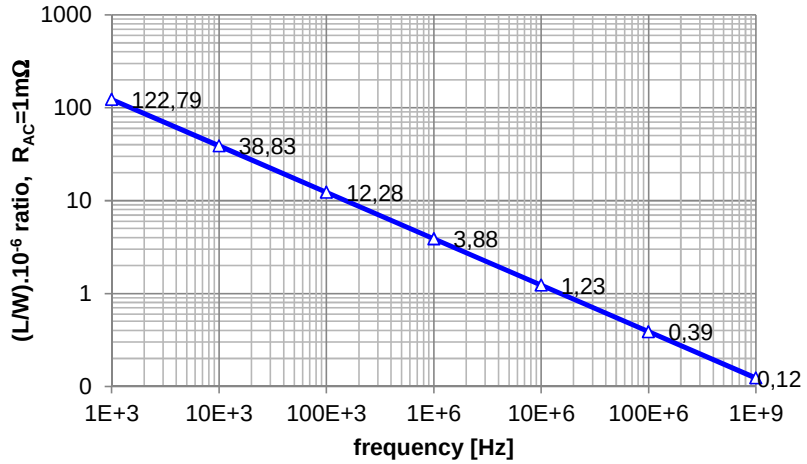
  - δ: skin depth in mm
  - f: frequency in MHz
  - ρ: resistivity of the copper: $1{,}68.10^{-10}\Omega.\ mm$
  - $\mu_0 = 4.\pi.10^{-10} H.mm^{-1}$
  - $\mu_r = 1$ relative permeability of nonmagnetic material



- Copper trace resistance

$$R_{AC} = \frac{\rho}{\delta}\frac{L}{W}$$

  - δ: skin depth in mm
  - ρ: resistivity of the copper: $1{,}68.10^{-11}\Omega.\ mm$
  - L: trace length in mm
  - W: trace width in mm



- Based on the skin depth value for a signal frequency *f*, signal traces must be sized appropriately to reduce losses because of the skin effect

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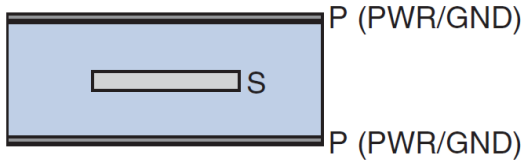
Signal layers topologies

- Microstrip

- external layer signaling topology
- Reference plane layer directly adjacent to the signal layer
- Difference between ε_r of air and ε_r of dielectric material causes odd (both lines drive in phase) and even (lines driven 180 out of phase) mode trace velocity differences that results in far-end cross-talk in differential pair routing

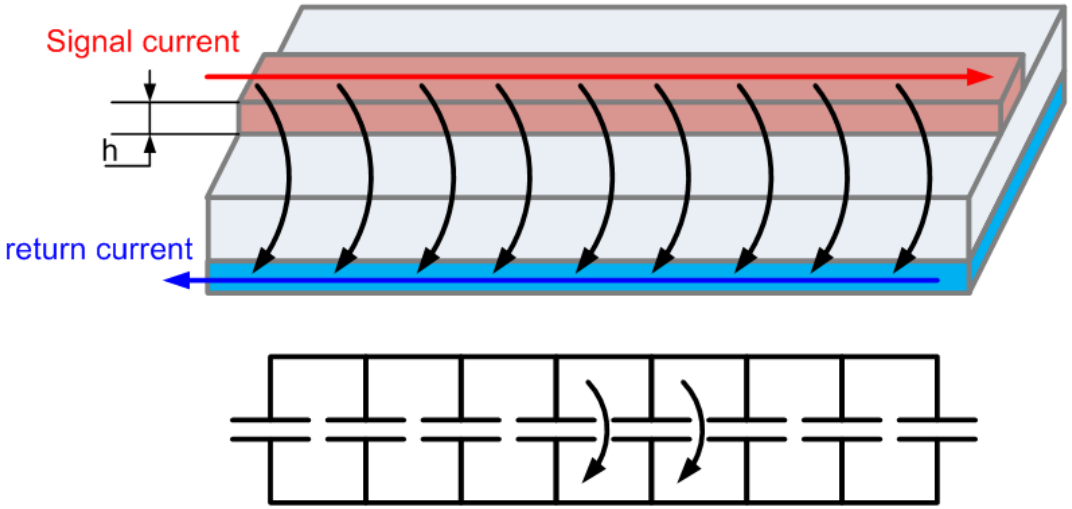
- Stripline



- internal layer signaling topology
- Reference plane layer on top and below the signal layer: provides the best signal isolation
- Zero far-end cross-talk because of uniform ε_r surrounding the signal lane

Used stripline for routing differential pairs

Return current path

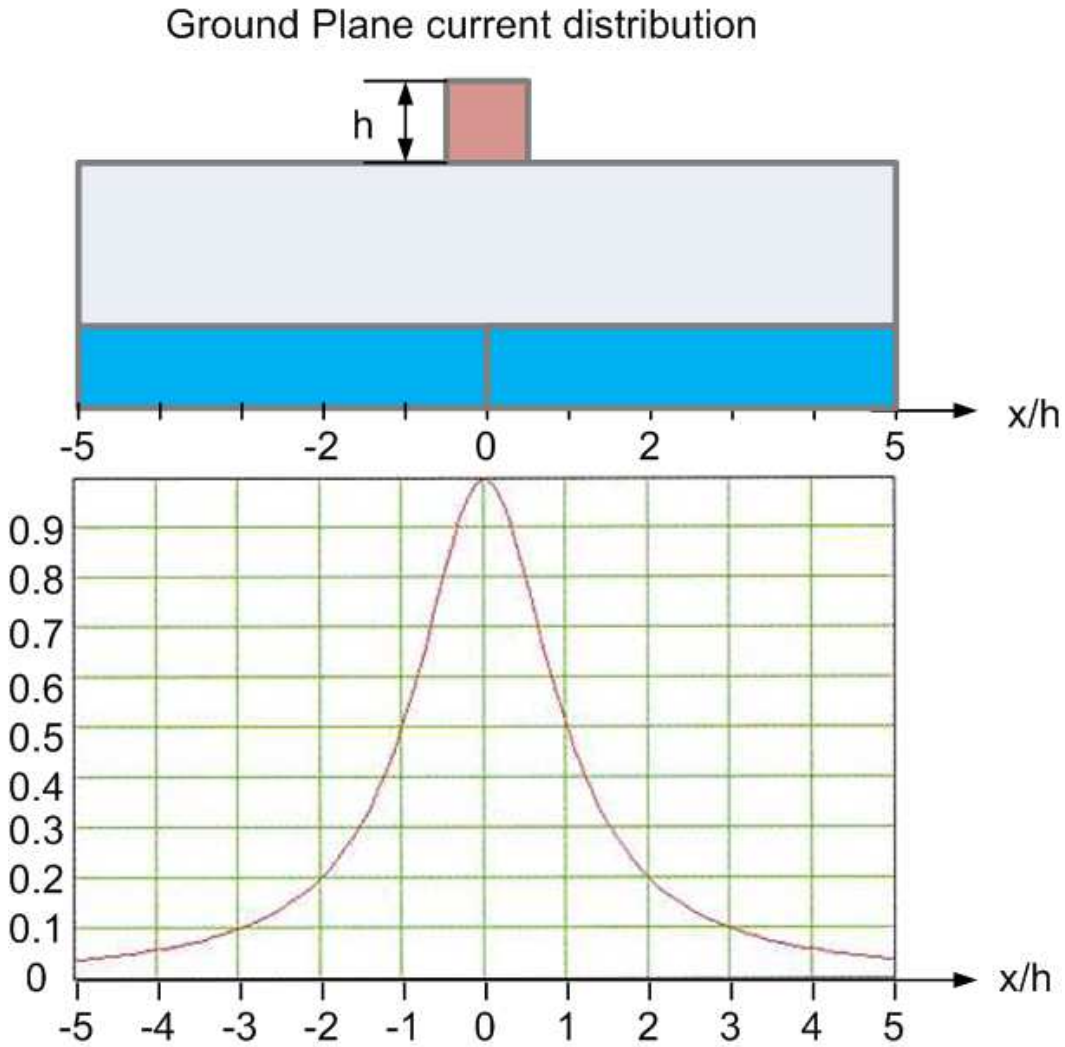


- There is always a current loop, and if some current goes out to somewhere, it will always come back to the source
- High frequency currents get to the return path through the distribute capacitance of the transmission line since this is the lowest impedance path
- Return current will flow on the plane adjacent to the trace regardless the plane is Ground, Power, or even other parallel traces.

Return current path Distribution

x/h ratio	Ground plane current contained within a distance of +/- x/h from the center trace
2	70% of current
5	87% of current
10	94% of current
20	97% of current

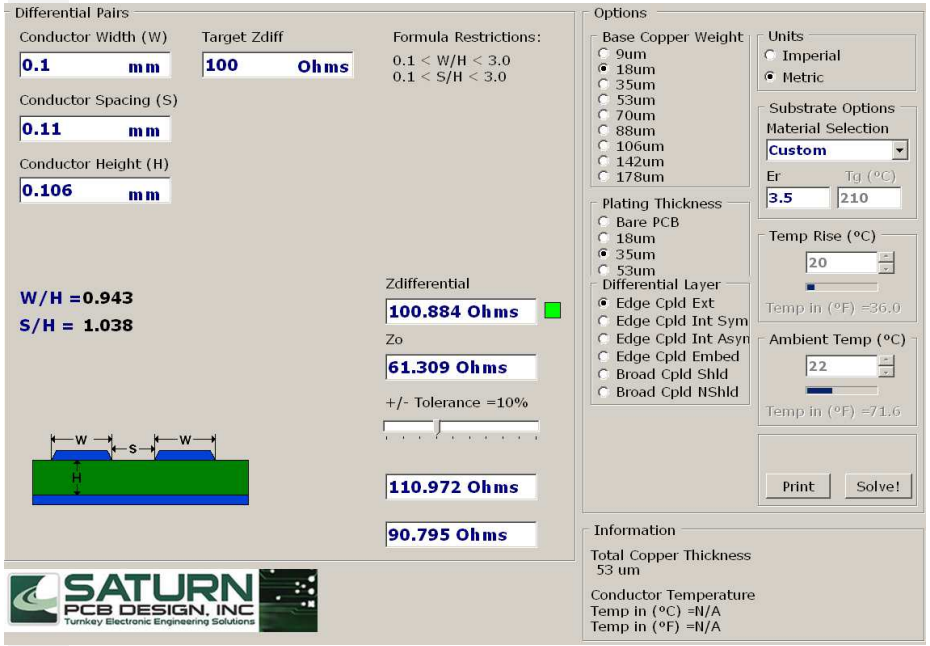
- Return current is slightly spread out in the adjacent plane but it stays under the trace



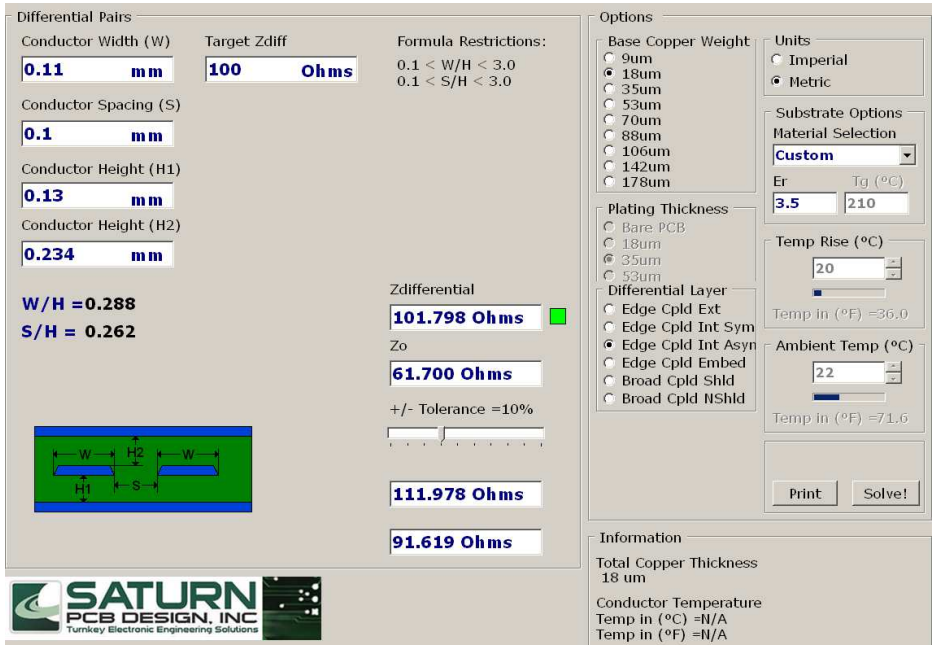
High speed signal layer differential pairs

- Plan the differential pair routing during the stack-up definition

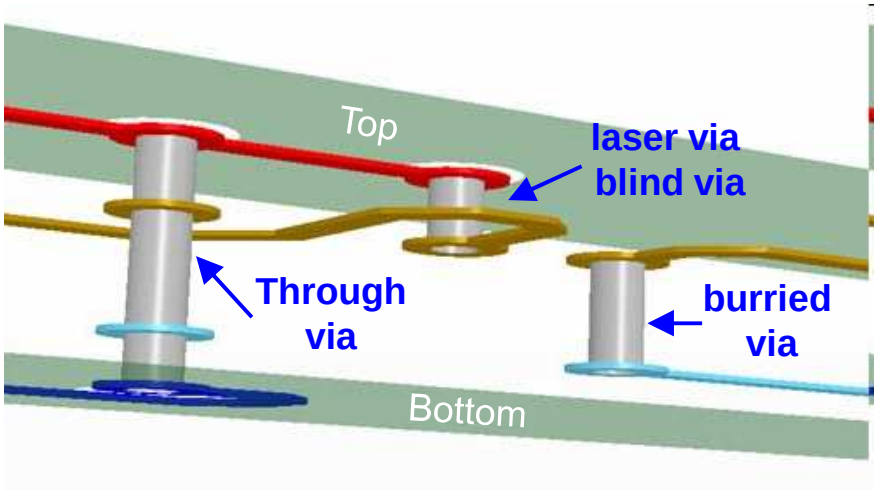
microstrip



stripline



Different via technology



- For high density routing PCB due to high channel count FPGA and RF, mixed signal and digital signal domain insulation laser via must be used for the best signal integrity performance

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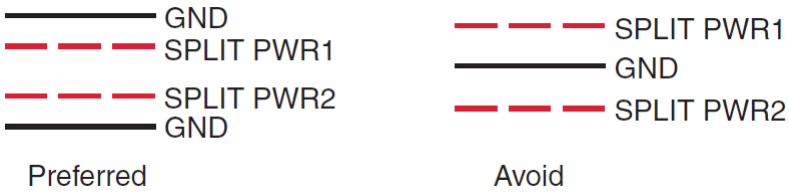
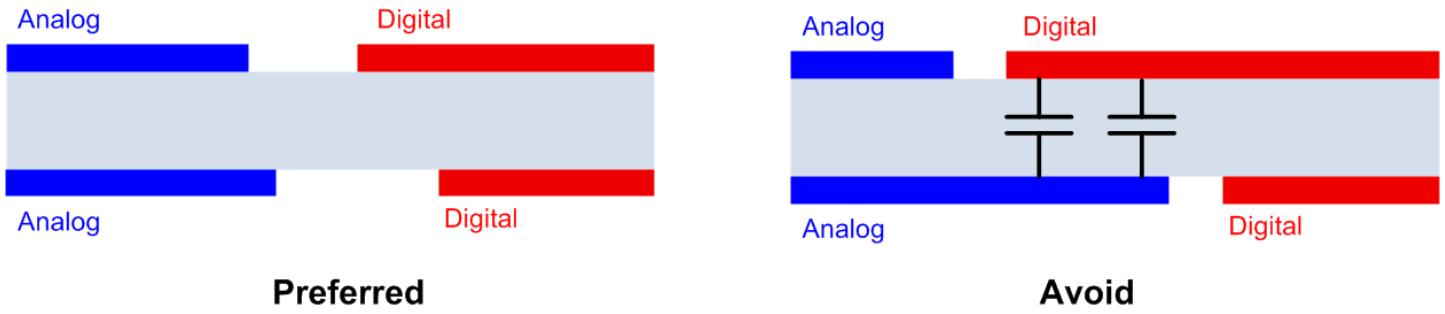
Power & Ground layers



- Segmented Power planes
  - Power shared as much as possible on any designated power layer to reduce the total layer count
- Solid Ground planes
  - Fill the entire layer
- Power placed next to a ground
  - Creates planar capacitance
    - Aids high frequency decoupling
    - Reduces electromagnetic Interference (EMI) radiation
    - Enhance electromagnetic compliance (EMC) robusness
- Given a choice between ground plane or power plane as return current path always choose ground plane
  - Using power plane as return current path for high speed routing layers allows switching noise to couple to the power plane. This must be avoided especially for sensitive power plane such as:
    - RF and analog transceivers
    - PLLs
    - ADCs / DACs
- To avoid this situation sensitive power plane must be isolated from signal layers by sandwiching segmented power layers between solid ground layers

Power Plane rules and layout

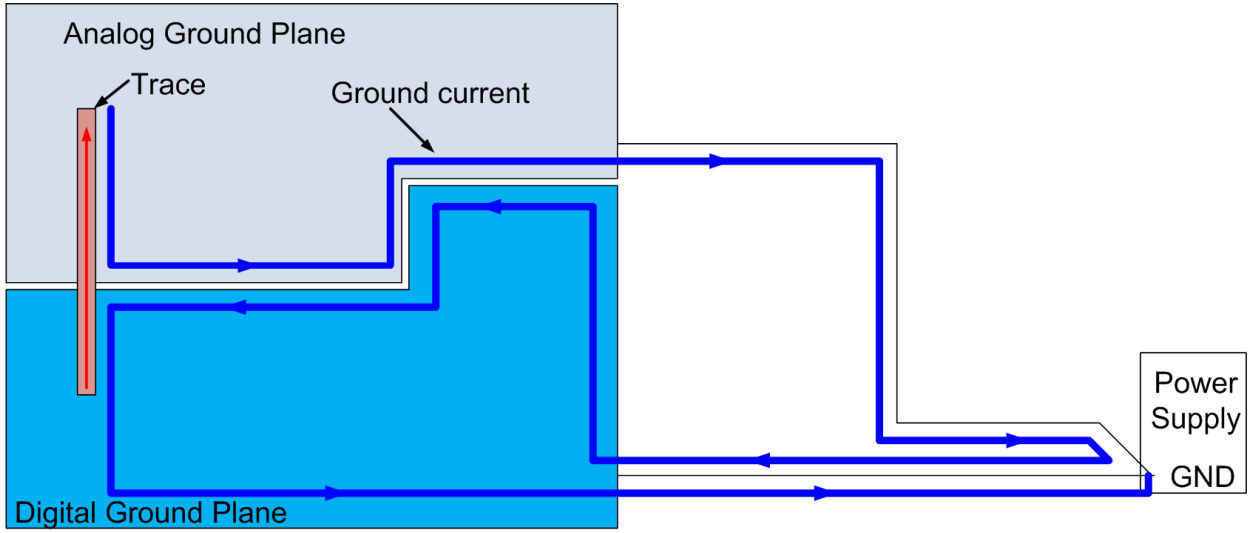


- Use separate supplies for analog and digital (even if this is the same voltage)
- **A digital power plane must never overlap an analog power plane**
  - capacitance between the overlapping areas, which is likely to cause RF emissions to pass from one plane to another

Basic principle of EMC: introduction to ground rules and layout in Mixed Signal PCB design

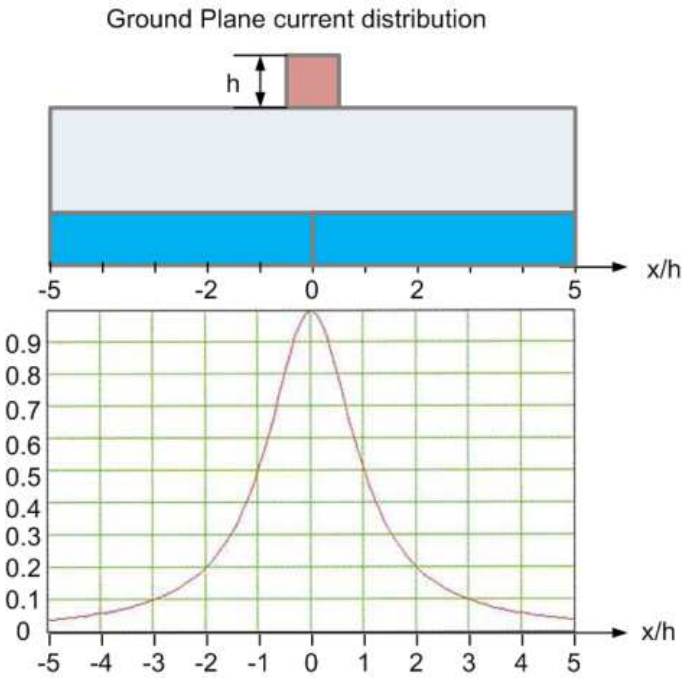
- Current should return to their source as locally and compactly as possible (through the smallest possible loop area)
  - If we do not return current locally and compactly we create a loop antenna
  - Magnitude radiation from small loop antenna is proportional to the:
    - area of the loop
    - Amount of current in the loop
    - Frequency squared
- System should only have one reference.
  - If we create 2 references for a system we create a dipole
  - Magnitude radiation from a small dipole is proportional to the:
    - Length of the wire
    - Amount of current in the wire
    - Frequency
- What we must care in High speed mixed signal PCB design is the possibility that the high-speed digital logic might interfere with low level analog circuits

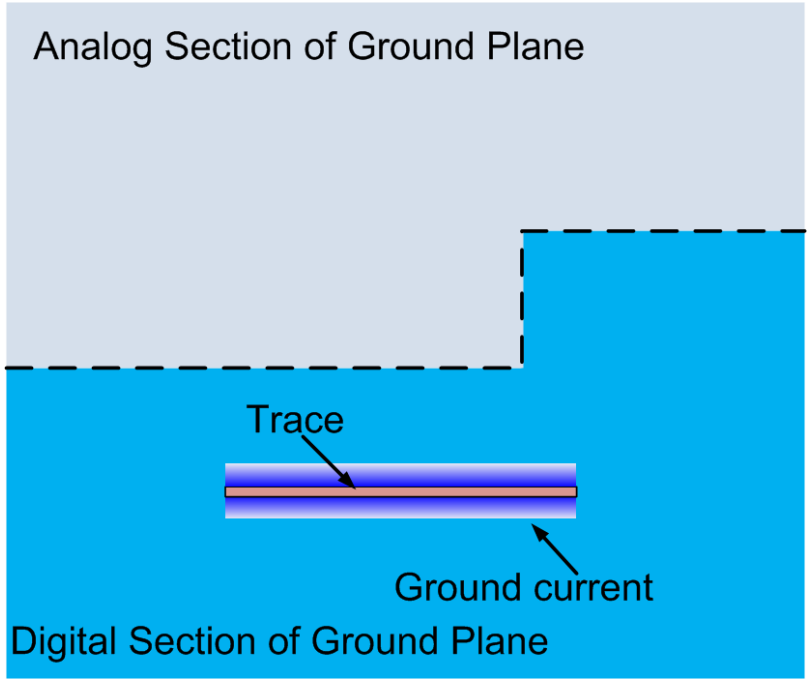
Separate Analog and Digital grounds ?



- Trace crossing over the split between the isolated analog and digital ground plane connected together only at the power supply.
  - High frequency return current have to flow in a large loop producing radiation and high ground inductance
  - Low levels analog current flowing in a large loop are susceptible to interference
  - Analog ground and digital ground planes are at different RF potentials and connected together with long wires: this is a very effective dipole
- **Never ever separate analog and digital grounds when designing a mixed signal PCB**

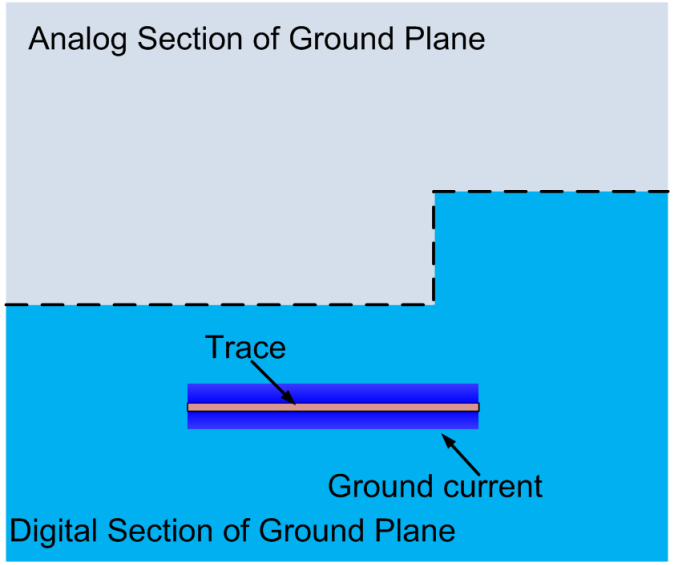
Ground rule: use one solid ground plane



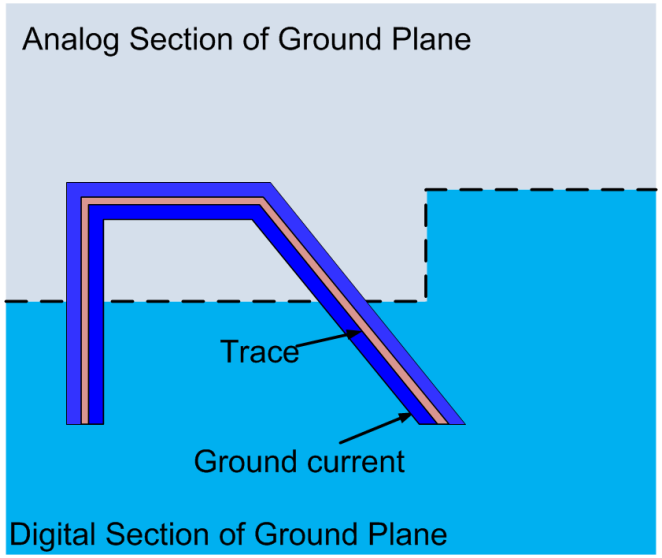


- Digital ground signal have no desire to flow through the analog portion of the ground plane and corrupt the analog signal
- **Use one solid ground plane for Mixed PCB design and partition the PCB routing in analog and digital sections**

Trace rule: Digital signal routed in digital section



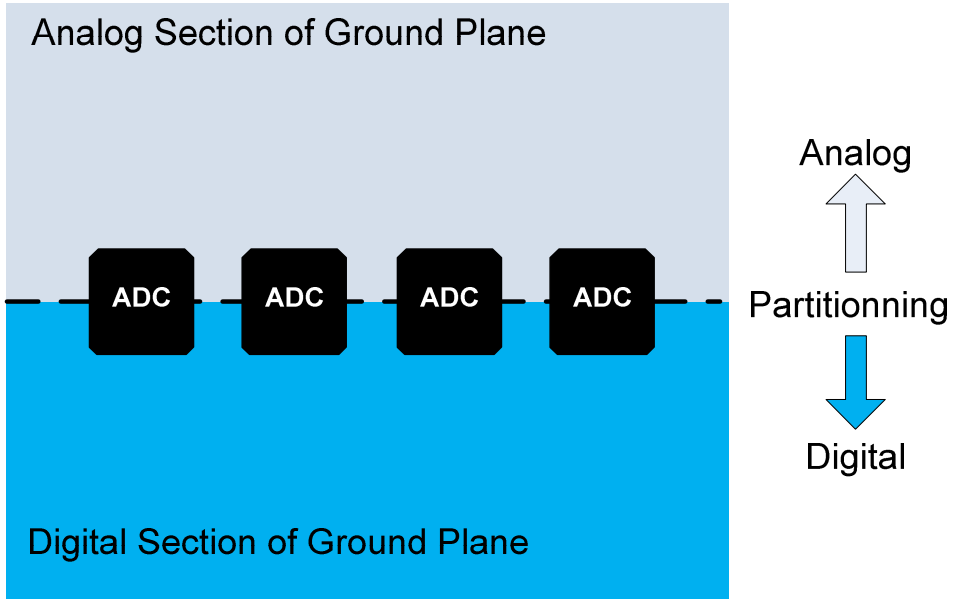
- Preferred



- Poor: digital ground current now flow in the analog section

- **Digital signal must be routed only in the digital section of the board (all layers)**
- **Respect this rule 100%**
- 1 improperly routed trace can destroy an otherwise perfectly good layout

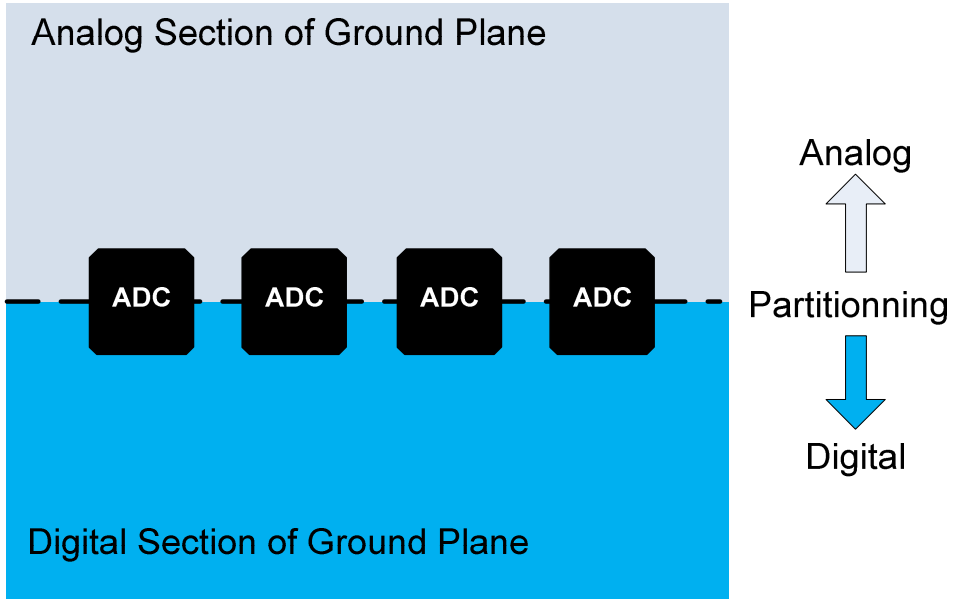
Mixed signal devices Component placement and ground strategy



- How to connect ADC analog and digital ground pins
  - ADC manufacturers suggest the following:

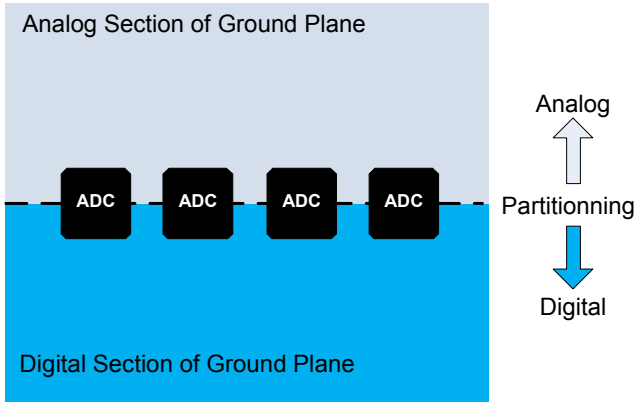
  “The AGND and DGND pins must be connected together externally to the same low impedance ground plane with minimum lead length. Any extra impedance in the DGND connection will couple more digital noise into the analog circuit through the stray capacitance internal to the IC”

Mixed signal devices Component placement and ground strategy



- Remember: **Rules for mixed signal design PCB is to use only one solid ground plane and then partitioned into analog and digital sections:**
  - It satisfies IC's manufacturers requirement: connecting AGND and DGND pins together through low impedance
  - It meets EMC concern of not creating any unintentional loop or dipole antenna

Summary: Mixed signal PCB partitioning and routing rules



- Do not split the ground plane, use one solid plane under both analog and digital sections of the board
- Use large area ground planes for low impedance current return paths
- Keep over 75% board area for the ground plane
- Separate analog and digital power planes
- Use solid ground planes next to power planes
- Locate all analogue components and lines over the analogue power plane and all digital components and lines over the digital power plane
- Do not route traces over the split in the power planes, unless if traces that must go over the power
- plane split must be on layers adjacent to the solid ground plane
- Think about where and how the ground return currents are actually flowing
- Partition your PCB with separate analog and digital sections
- Place components properly

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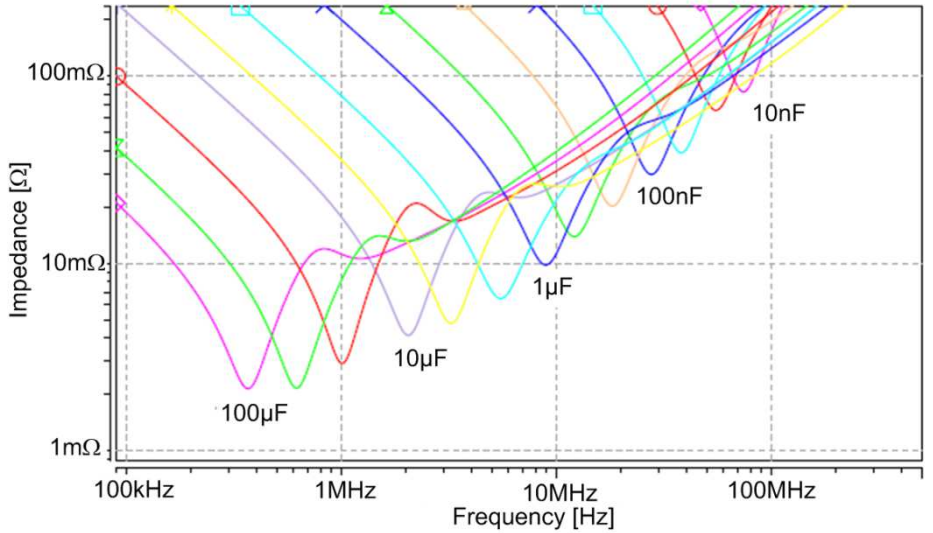
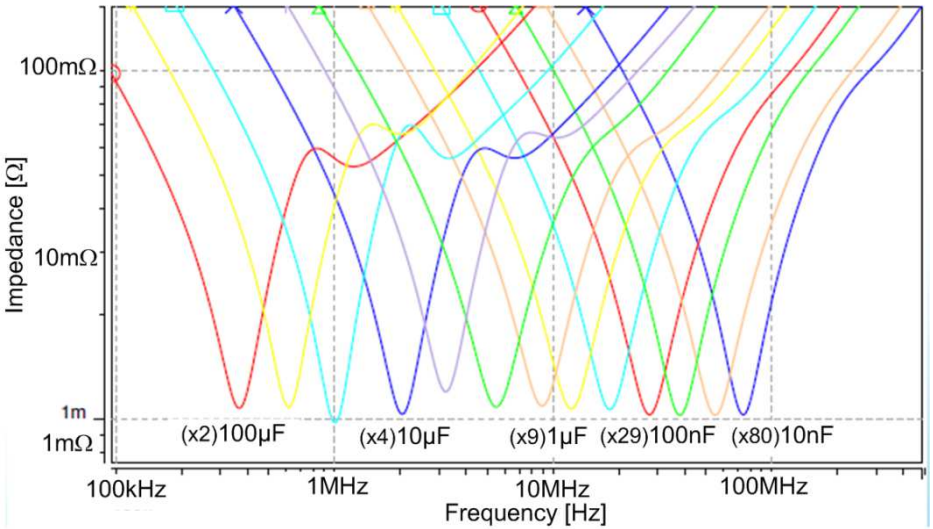
Capacitor characteristics

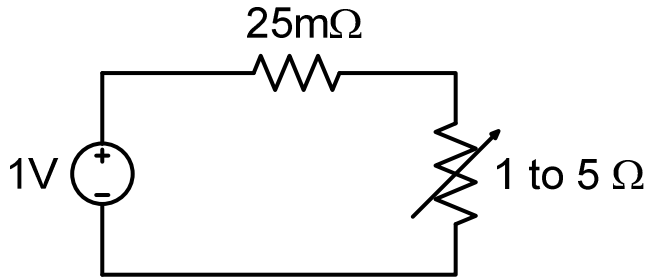
- Family of Ceramic surface mount capacitor
- X5R and X7R dielectric
- Minimum impedance value is frequency and capacitance dependent

- Several quantities in parallel to reach target impedance





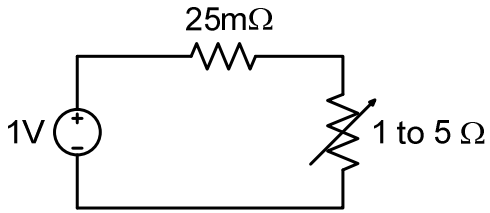
Target impedance definition



- $Z_{TARGET} = \frac{V_{DD}xTolerance}{I_{MAX} - I_{MIN}} = \frac{1Vx0.02}{1A - 0.1A} = 25m\Omega$
- Based on Ohms Law
- Transient current are important

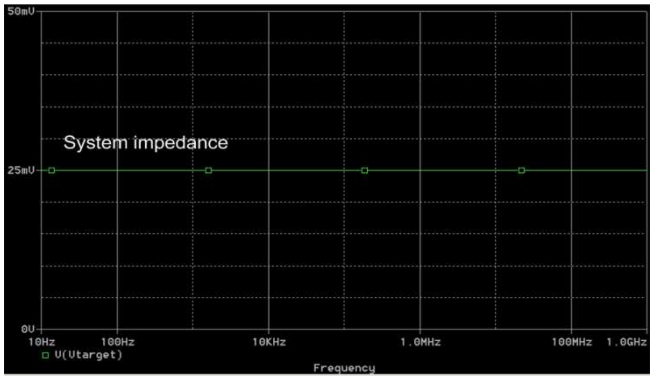
Must Guarantee that supply will not exceed specified tolerance with given transient current

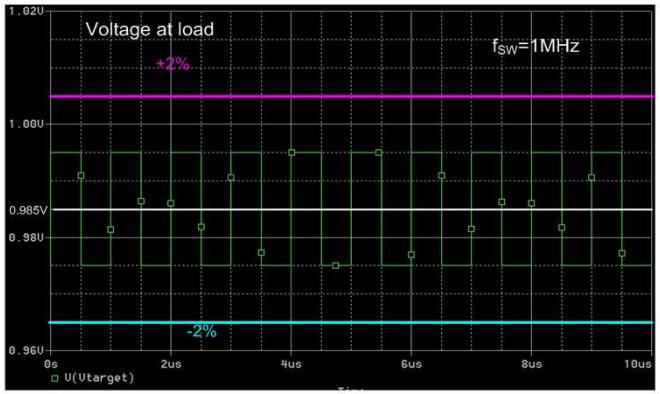
System that meet target impedance

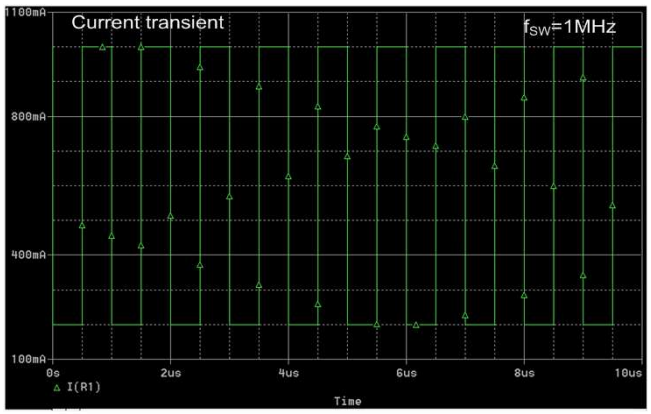


Voltage	1	V	
Power	1	W	
Max current	1	A	1 Ω
Transient current	50	%	
Min current	0.2	A	5 Ω
Ripple	2	%	
Target impedance	25	mΩ	

Voltage drop @ Min current, Z_{TARGET}	0.005 V
Voltage drop @ Max current, Z_{TARGET}	0.025 V
IR Drop=Voltage drop average, Z_{TARGET}	0.015 V
	1.5 %
Voltage average, Z_{TARGET}	0.985 V

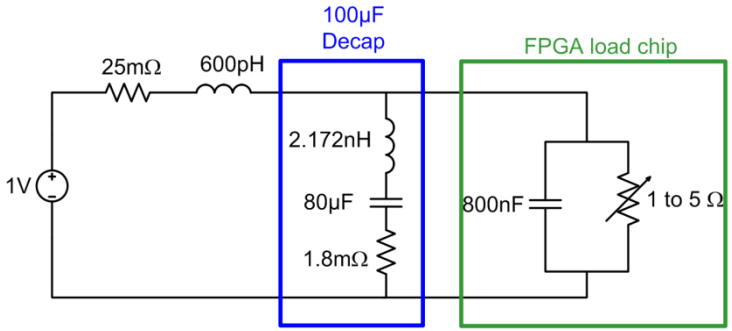


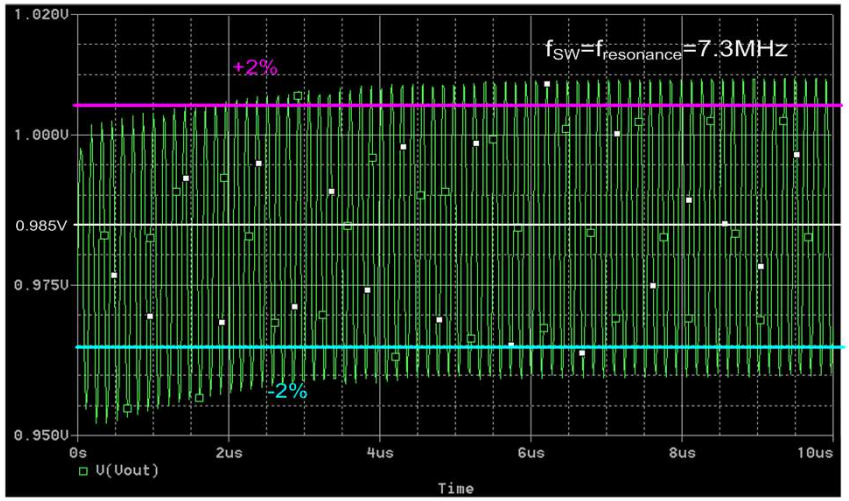




- Flat in frequency domain
- Acceptable regulation in time domain

System with resonant peak





- Peak in frequency domain
- Excessive noise in time domain
  - Fail to meet ± 2%
- Resonant peak must be avoided

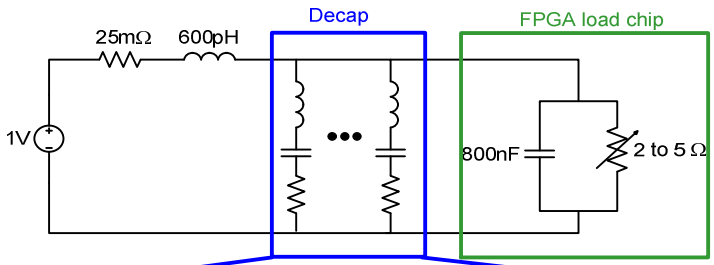
Menu of Capacitors

Cap Value	Size	Dielectric	Measured value	ESR (mΩ)	L internal (nH)	L mount (nH)	SRF (MHz)	Q	# cap to meet 1mΩ target	# cap to meet 25mΩ target
100 µF	1812	X5R	80.3 µF	1.8	2.112	0.6	0.341	3.2	2	0
47 µF	1210	X5R	42.1 µF	1.9	1.487	0.6	0.537	3.7	2	0
22 µF	1210	X5R	17.7 µF	2.5	1.3	0.6	0.868	4.1	3	0
10 µF	0805	X5R	7.26 µF	3.6	0.773	0.6	1.594	3.8	4	0
4.7 µF	0805	X5R	4.12 µF	4.2	0.544	0.6	2.318	4.0	4	0
2.2 µF	0805	X5R	1.98 µF	6.1	0.413	0.6	3.554	3.7	6	0
1 µF	0603	X5R	0.79 µF	9.1	0.391	0.6	5.688	3.9	9	0
470 nF	0603	X5R	404 nF	13	0.419	0.6	7.844	3.9	13	1
220 nF	0603	X7R	172 nF	19	0.438	0.6	11.911	4.1	19	1
100 nF	0603	X7R	75 nF	29	0.443	0.6	17.995	4.1	29	1
47 nF	0603	X7R	39 nF	38	0.451	0.6	24.859	4.3	38	2
22 nF	0603	X7R	17 nF	64	0.492	0.6	36.939	4.0	64	3
10 nF	0603	X7R	8.9 nF	80	0.518	0.6	50.455	4.4	80	3
								Totals	273	11

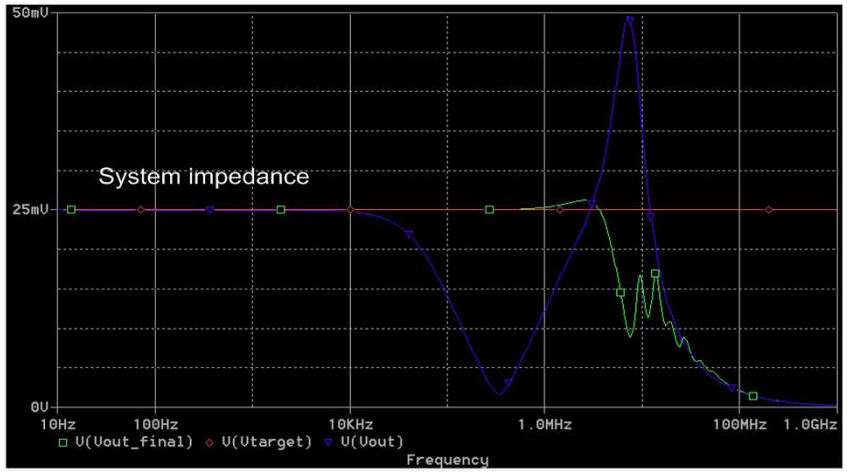
ESR: Equivalent Series Resistance
SRF: Series resonant frequency

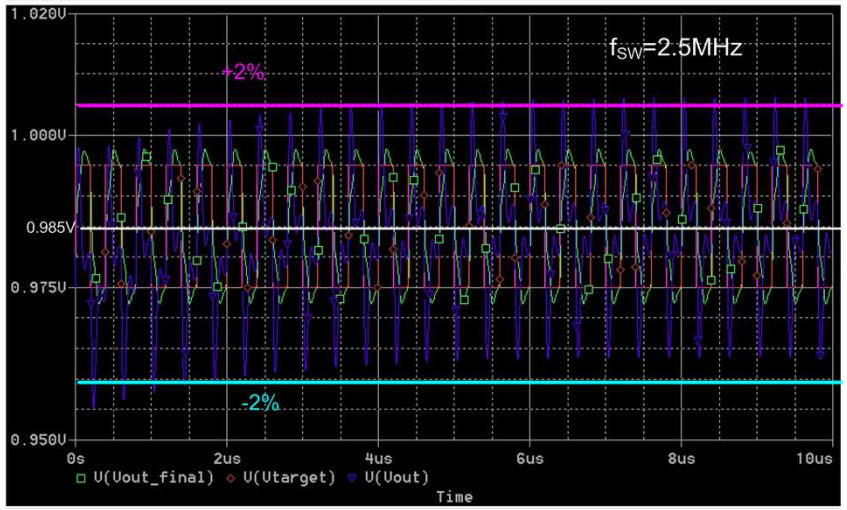
- 3 capacitor values per decade
- Q is important. High peaks are associated with deep dips

FDTIM



Cap Value	Size	Dielectric	Measured value	ESR (mΩ)	L internal (nH)	L mount (nH)	SRF (MHz)	Q	# cap to meet 25mΩ target
470 nF	0603	X5R	404 nF	13	0.419	0.6	7.844	3.9	1
220 nF	0603	X7R	172 nF	19	0.438	0.6	11.911	4.1	1
100 nF	0603	X7R	75 nF	29	0.443	0.6	17.995	4.1	1
47 nF	0603	X7R	39 nF	38	0.451	0.6	24.859	4.3	2
22 nF	0603	X7R	17 nF	64	0.492	0.6	36.939	4.0	3
10 nF	0603	X7R	8.9 nF	80	0.518	0.6	50.455	4.4	3
								Totals	11



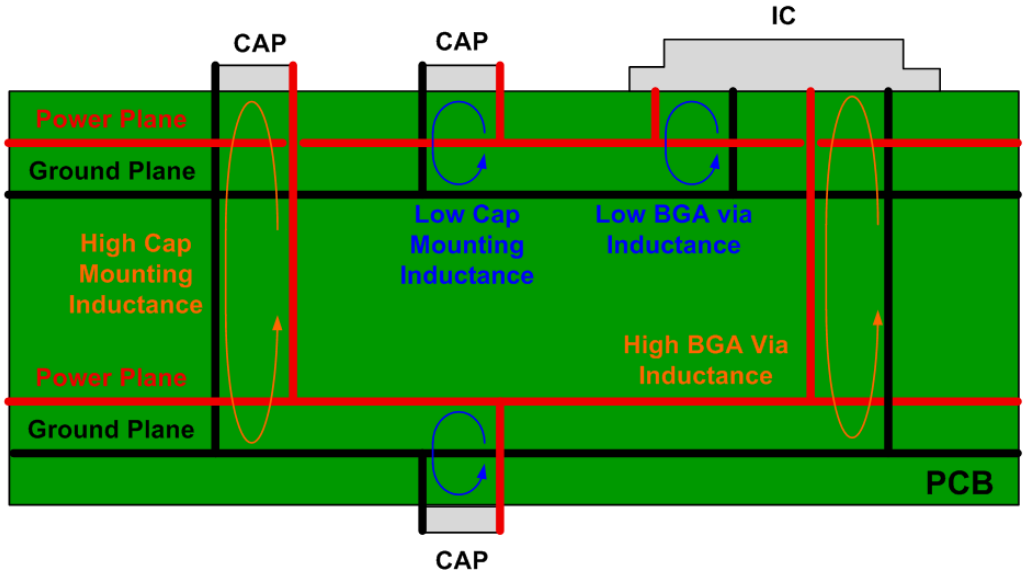


- Frequency Domain Target Impedance Method (FDTIM) attributes:
  - Use many different capacitor values
    - Perhaps a dozen
    - 3 values per decade (10, 22, 47)
  - Usually the least expensive BOM
    - Standard capacitor (1205, 0805, 0603, 0402 sizes)
    - Smaller capacitor size
  - Usually the least board area
    - Only use large size capacitors where necessary
  - Uses capacitor that are readily available

Outline

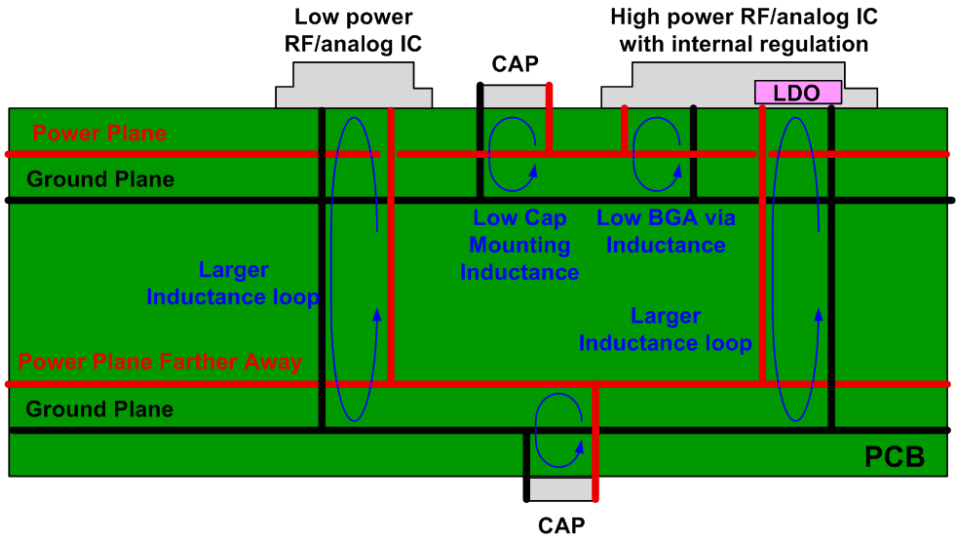
- PCB stack-up and material losses (ε_r, tanδ, skin effect)
- Signal layers topologies and return current path
- Mixed signal design rules
  - Power and Ground stack-up
  - Ground routing rules
  - Signal routing rules
- Decoupling strategy: Frequency Domain Target Impedance Method (FDTIM)
- Decoupling placement rules
  - RF/analog Ics
  - High current power rails

Power plane and decoupling capacitor placement strategy



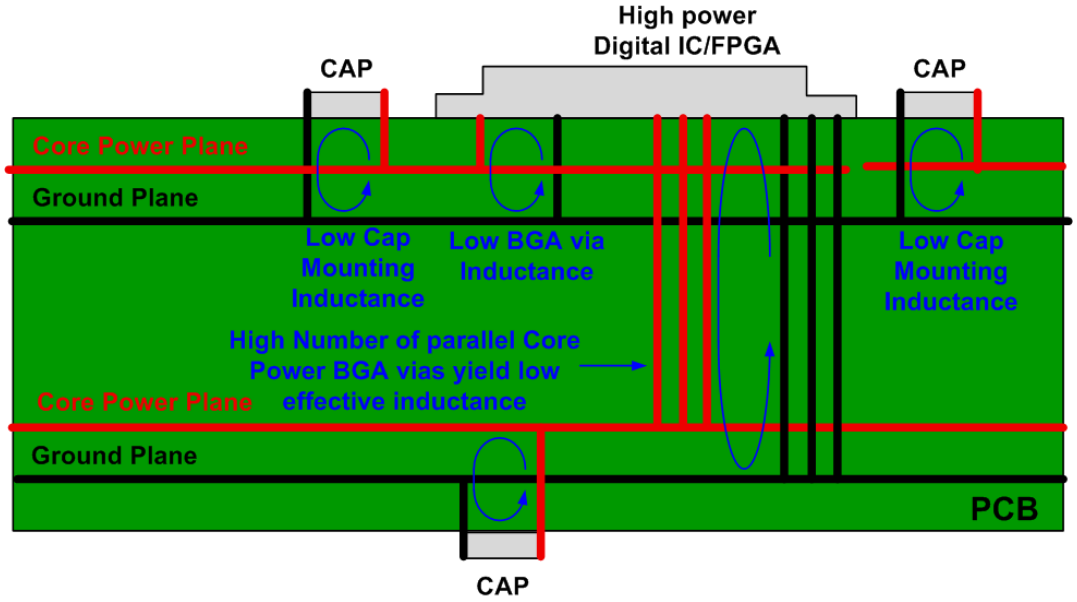
- Place each decoupling capacitor in close proximity to the corresponding power plane it decouples to minimize the capacitor mounting inductance loop
- Place the power and ground planes in close proximity to the device so they minimize the BGA via inductance loop

Rules for RF, Analog Power plane placement



- RF and analog (including PLL and ADC) power rails are susceptible to noise/spurious that can directly impact sensitivity performances.
- RF and analog power planes have the highest priority in the power plane stack-up placement over other power rails unless:
  - RF/analog ICs have internal regulation that helps isolate from on-board noise. Internally regulated power rails can be placed further away from the RF/analog device
  - Current demand of the RF/analog ICs power rails are low enough to yield a high impedance target that is easily decoupled even when their power planes are placed further away from the IC
- General rule: Place RF/analog power rails closest to the RF/analog ICs

Rules for High current Power rails



- High-current power rails result in lower target impedance and present a greater challenge for decoupling:
  - As a general rule, high-current power rails should typically be placed close to the IC to minimize BGA via inductance
  - However, for high-current core power in digital IC / FPGA, place the rails furthest from the device to minimize the capacitor mounting inductance while benefiting from the reduced effective BGA via inductance that result from having an increased number of parallel core power and ground via pairs

Glossary

ADC	Analogue to Digital Converter
BGA	Ball Grid Array
EMC	Electromagnetic conformance
EMI	Electromagnetic Interference
ESR	Effective Series Resistance
FDTIM	Frequency Domain Target Impedance Method
FPGA	Field Programmable Gate Array
GND	Ground
IC	Integrated Circuit
IOs	Inputs/Outputs
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PWR	Power
Q	Quality factor
RF	Radiofrequency
SI	Signal Integrity
SRF	Series Resonant Frequency
tan(δ)	Loss tangent
δ	Skin depth
ε_r	Dielectric constant

References

- PCB Stackup Design Considerations for Altera FPGAs, AN-613, Oct. 2010, http://www.altera.com/literature/an/an613.pdf
- H.W. Ott, “Partitioning and Layout of a Mixed-Signal PCB”, Printed Circuit Design, June 2001.

  http://www.hottconsultants.com/pdf_files/june2001pcd_mixedsignal.pdf
- Guidelines for Designing High-Speed FPGA PCBs, AN-315, Jul. 2002, http://www.altera.com/literature/an/an315.pdf
- L.D. Smith, “Frequency Domain Target Impedance Method for Bypass Capacitor Selection for Power Distribution Systems”, DesignCon2006. http://www.ipblox.com/pubs/DesignCon_2006/DC06_PDN-design_panel-slides.pdf

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