Convertisseurs analogiques/numériques : applications, défis de conception et développements futurs

Authors : C2S members

presented by Patricia Desgreys

C2S research group
Institut TELECOM – TELECOM ParisTech – Comelec
LTCI – CNRS UMR 4151
46, rue Barrault 75013 Paris
Tel. +33 1 45 81 78 43
Fax +33 1 45 80 40 36
Patricia.Desgreys@telecom-paristech.fr
http://www.comelec.enst.fr/

LTCI - UMR5141

Outline

- Introduction
- ADC fundamental architectures
- ADC performance: State-of-the-art
- Challenges and promising techniques
- Conclusion

Planning R&D (1)

Wireless Systems (LTE-A, IMT Advanced, CRN, WSN)

- Analog to Digital Converter – Wideband - Flexible
- Predistorsion – Algorithms – Digital signal processing associated
- System design – Transceivers – Definitions and specifications

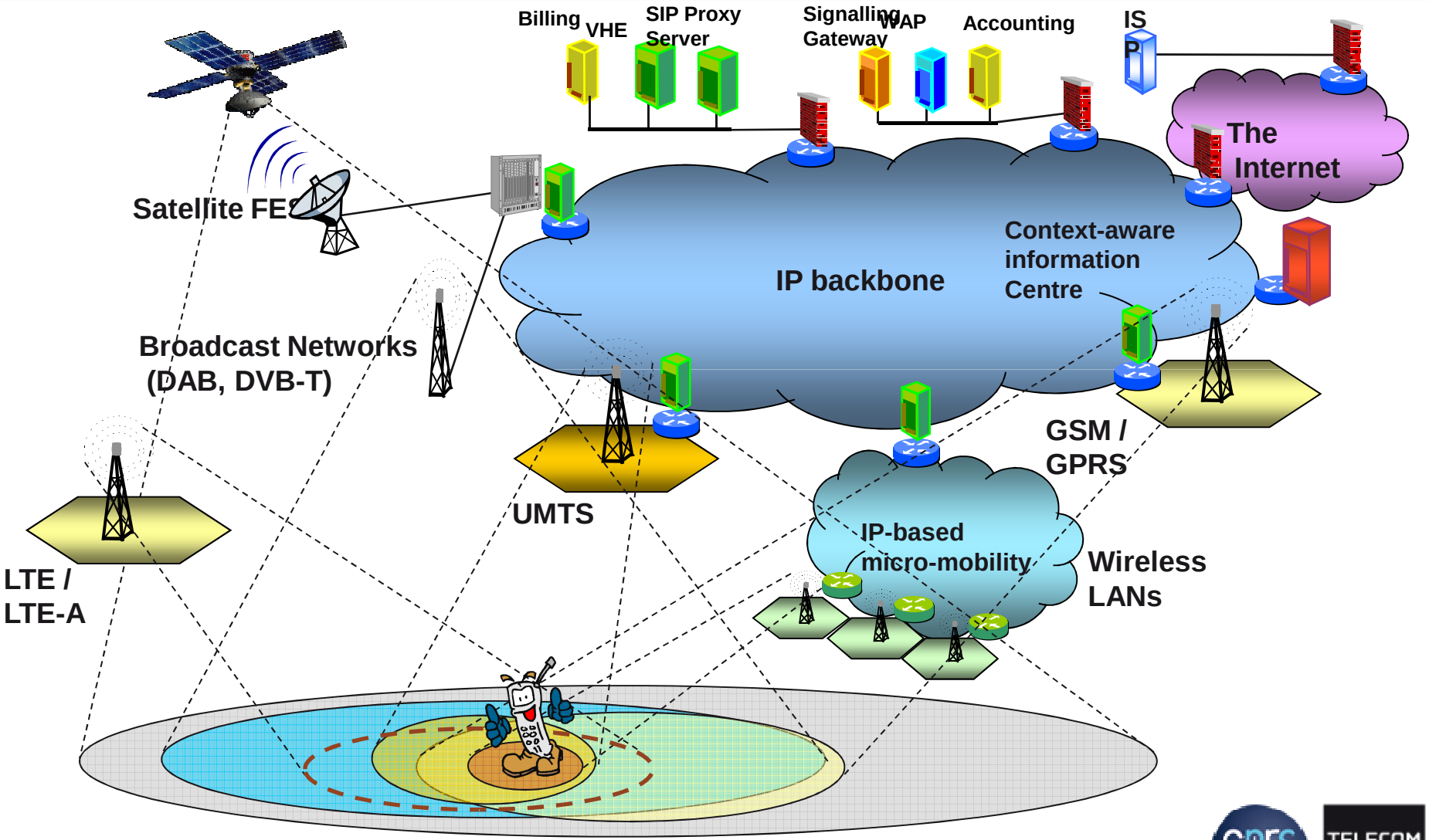
Group C²S : Circuits and Communication Systems

Design Techniques for Nanoscale Circuits

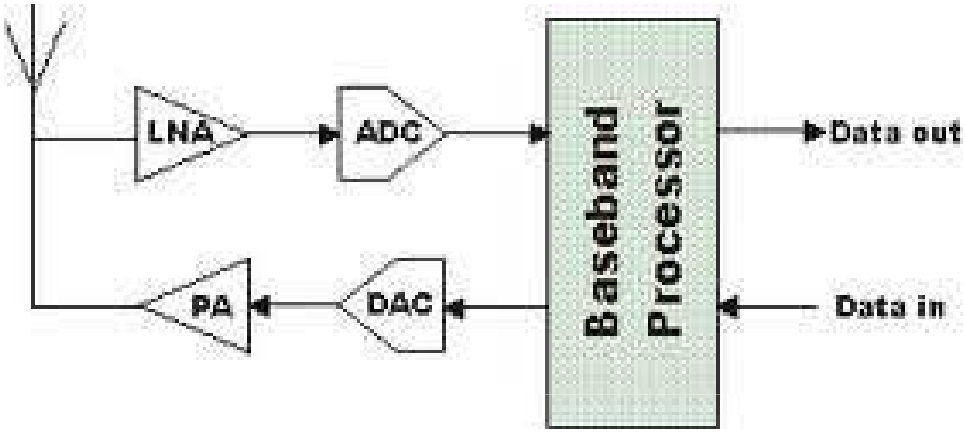
- Methodology and Design for Manufacturability & for Variability
- Design for Low-Power and AMS Simulation

1ier sem 2011	2ième sem 2011	1ier sem 2012	2ième sem 2012	1ier sem 2013	2ième sem 2013	1ier sem 2014	2ième sem 2014

New communications standards



Software radio



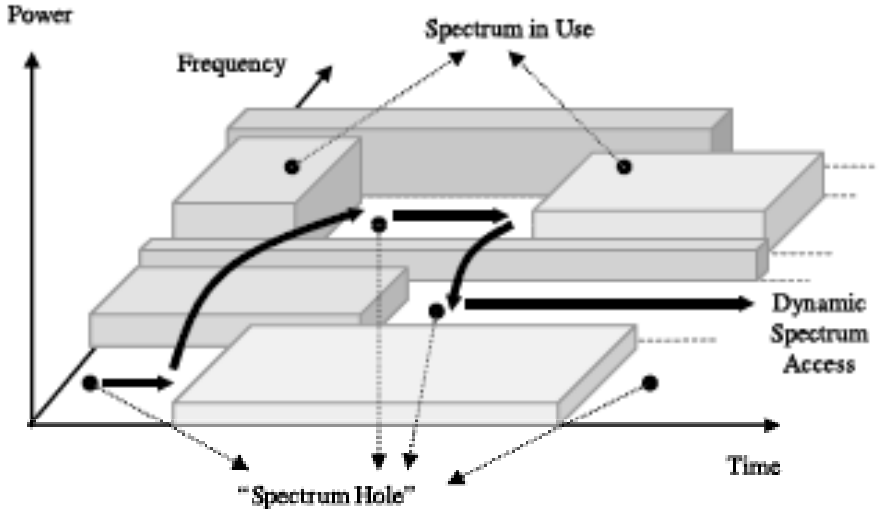
This concept is very demanding concerning **analog, mixed and RF blocks**

ADC speed > 2Gbit/s, Resolution > 16 bits,

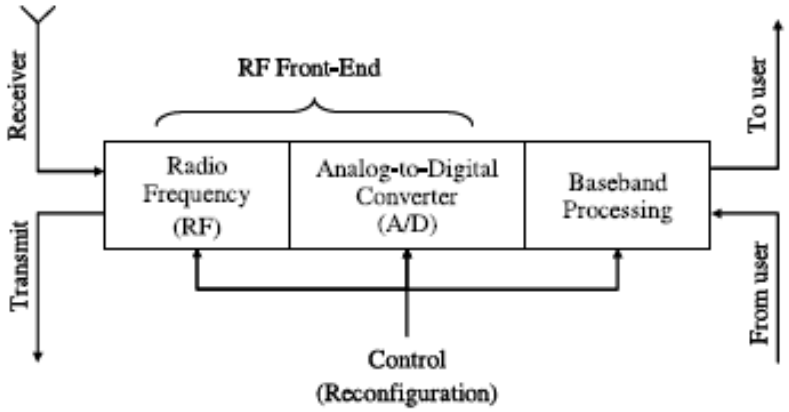
- For instance : ADC 16 bits, 2.2 GHz: power 1 to 10 W

This performance is achievable but at a cost too high in terms of power consumption

Cognitive radio



Source :
NeXt generation/dynamic spectrum access/cognitive radio wireless networks: A survey
Ian F. Akyildiz, Won-Yeol Lee, Mehmet C. Vuran *, Shantidev Mohanty
Computer Networks Elsevier 2006



Physical architecture of the cognitive radio

The key challenge of the physical architecture of the cognitive radio is an accurate detection of weak signals of licensed users over a wide spectrum range. Hence, the implementation of **RF wideband front-end and A/D converter are critical issues**

Required specifications on the ADC

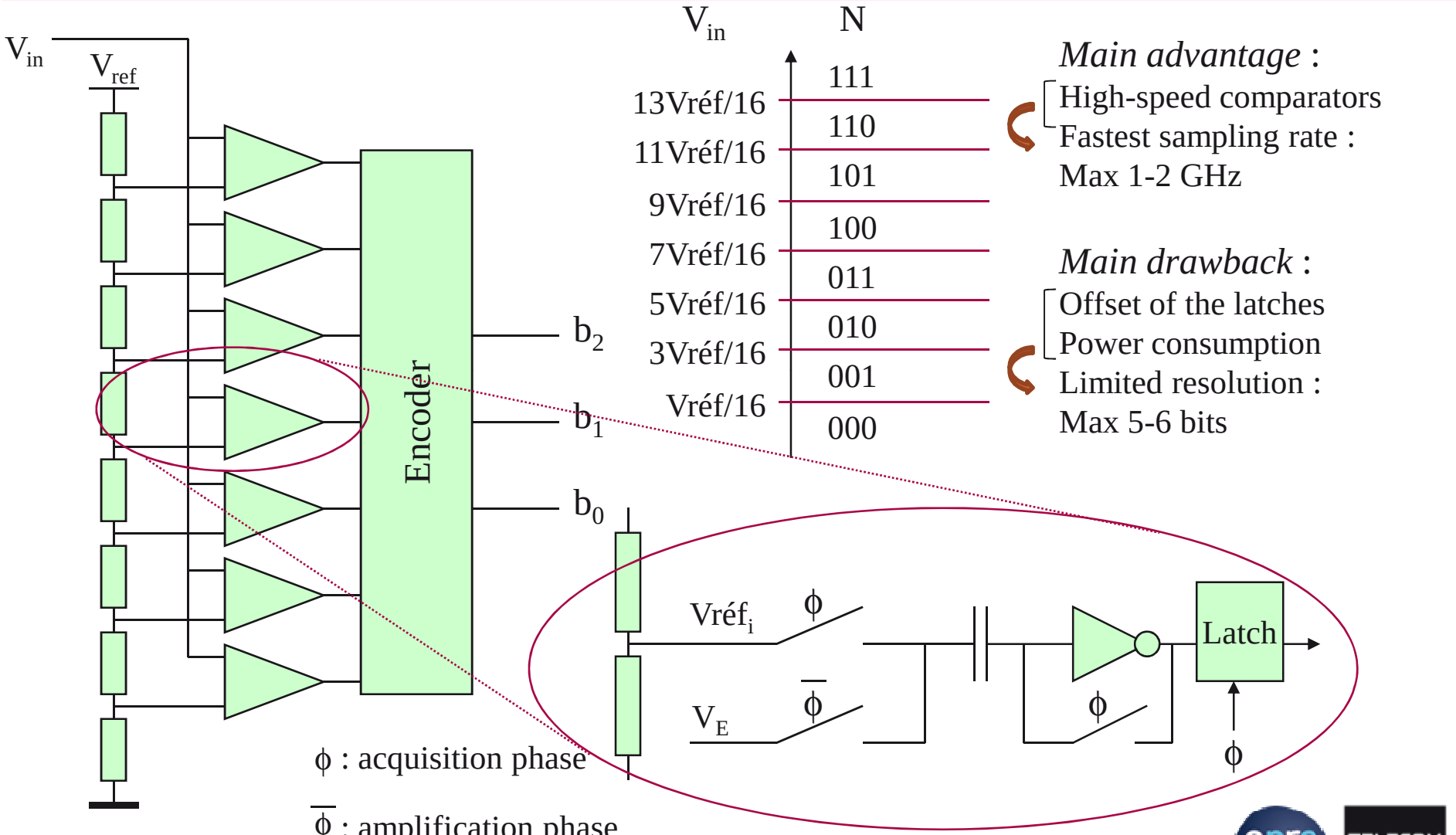
Analog-to-digital converters are key blocks in modern communication systems.

- 80 to 90 dB of SNR
- more than 90dB of SFDR
- 10-100 MHz of Bandwidth
- 0.5 pJ by conversion step

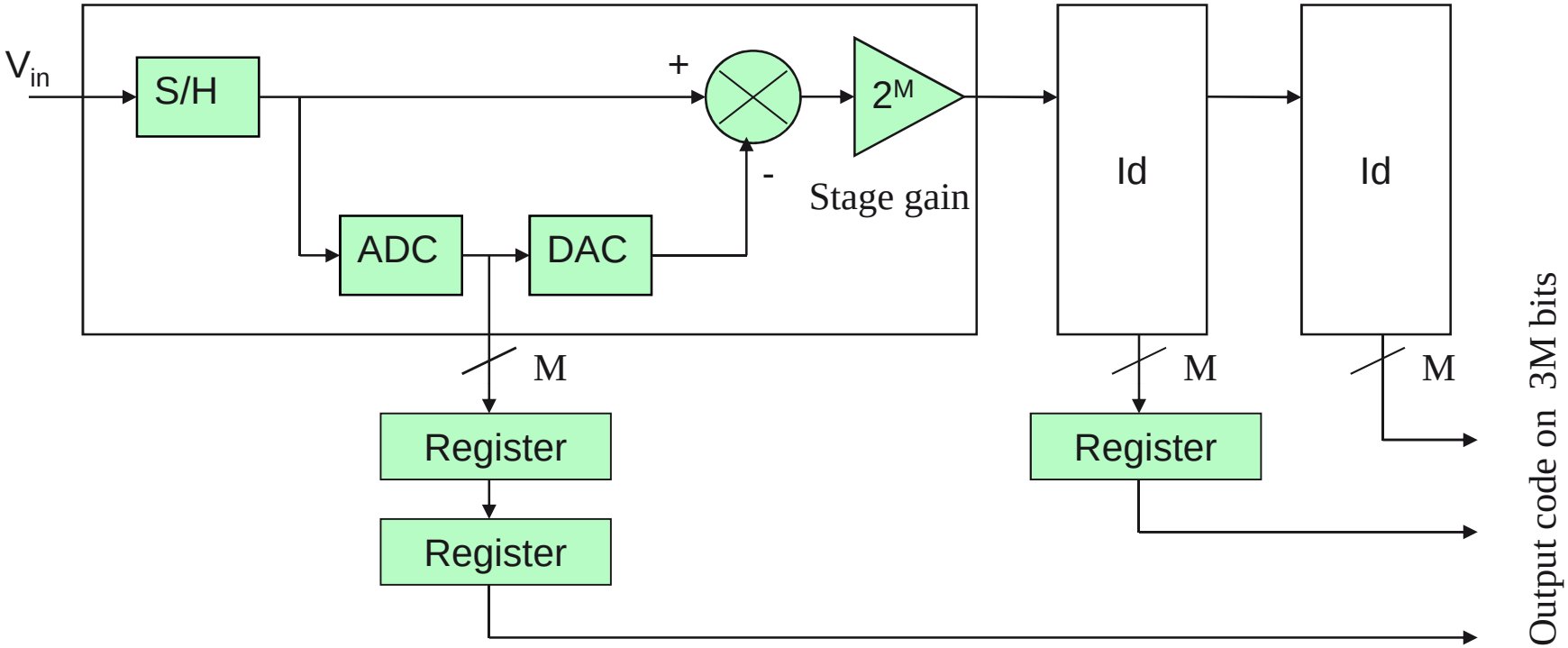
Outline

- Introduction
- ADC fundamental architectures
- ADC performance: State-of-the-art
- Challenges and promising techniques
- Conclusion

Flash converters



Pipeline converters



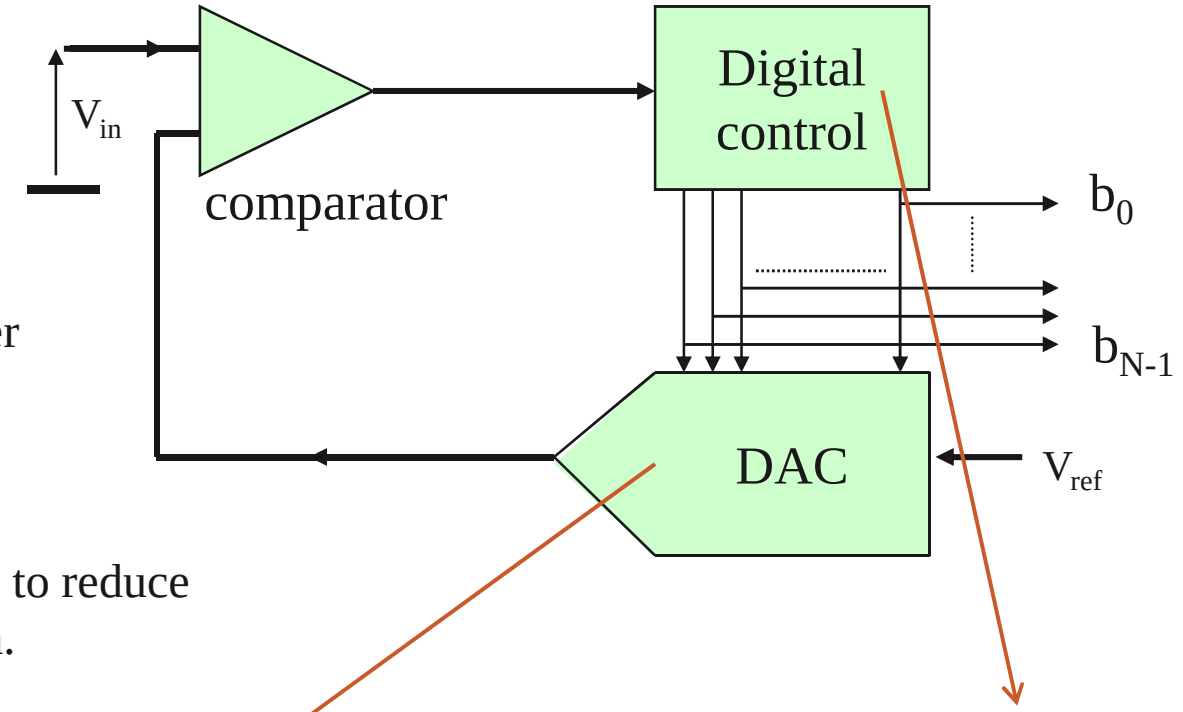
Advantage : Increased resolution (medium to high resolution) with large bandwidth (several 10 MHz) and limitation of power consumption.

Drawback : non idealities of each block generate distortions

Successive Approximation ADCs

Drawback : low speed

Advantages : medium resolution (10 bits), not expensive, low power consumption



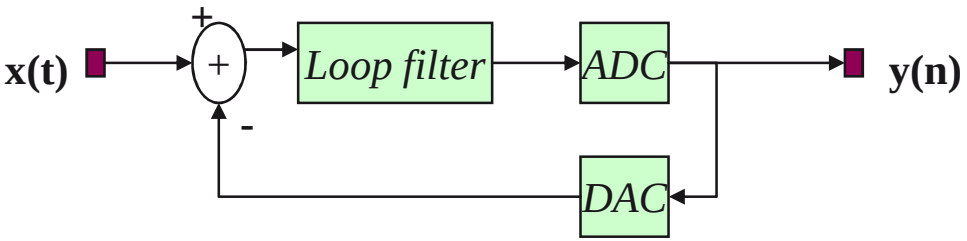
A large amount of efforts are done to reduce drastically the power consumption.

« Two-Step Junction-Splitting SAR Analog-to-Digital Converter », ISCAS 2010
Wenhuan Yu, Jiaming Lin and Gabor C. Temes
School of EECS, Oregon State University

« A Novel Energy Efficient Digital Controller for Charge Sharing Successive Approximation ADC », LASCAS 2011
T. G. Rabuske, F. A. Rabuske, C. R. Rodrigues
UFSM, Santa Maria, Brazil

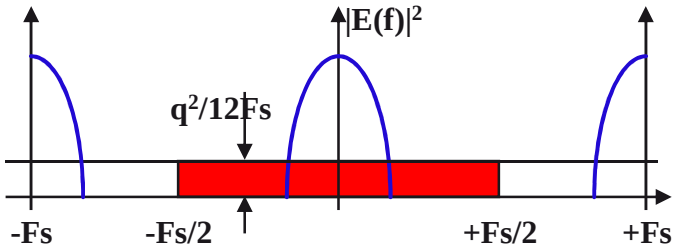
Delta Sigma converters

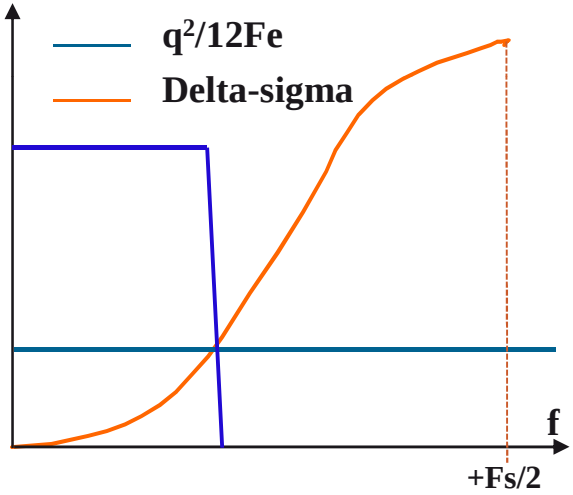
- Oversampling technique
  - SNR_{dB} = 6,02 N + 1,76 + 10 log M
  - with M = Fs / 2BW the oversampling ratio.
- Delta-sigma modulation
  - Spectral splitting of signal and noise



- Digital decimation filter

Advantage : High resolution (14-16 bits)
Drawback : Oversampling limits input signal bandwidth (a few MHz, max 10-20 MHz)





Noise shaping with low pass filter

Outline

- Introduction
- ADC fundamental architectures
- ADC performance: State-of-the-art 
- Challenges and promising techniques
- Conclusion

Performance parameters

- Speed :
  - Nyquist sampling rate : F_N
  - Bandwidth : BW
  - Over Sampling Ratio : OSR

$$F_N = 2BW$$

$$OSR = \frac{F_s}{2BW}$$

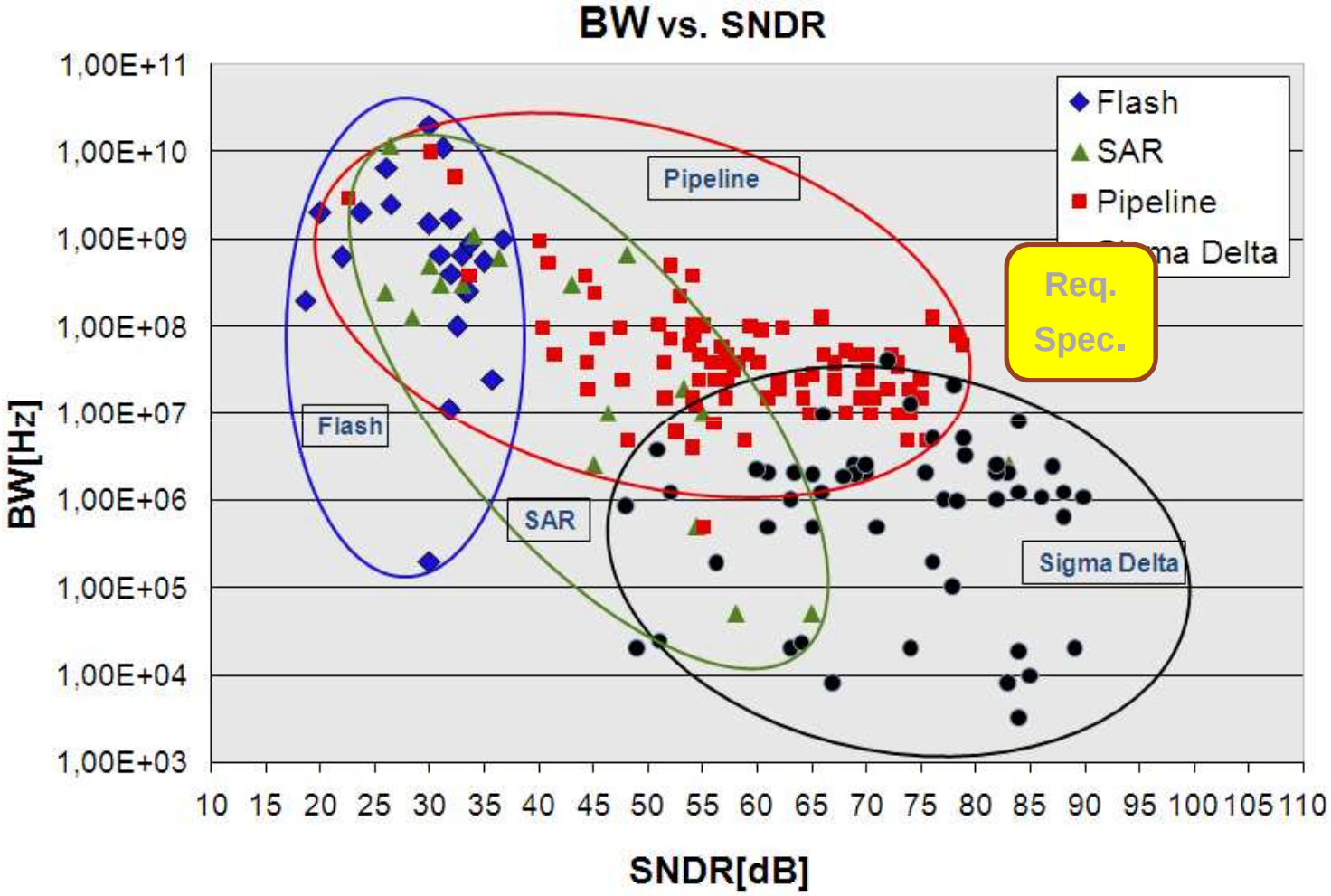
- Accuracy :
  - Stated resolution : N
  - Signal to Noise and Distortion Ratio : SNDR
  - Effective number of bits : ENOB
  - Spurious Free Dynamic Range : SFDR

$$ENOB = \frac{SNDR - 1.76}{6.02}$$

- Power :
  - Power consumption : P_{diss}
  - Figure of Merit : FoM

$$FoM = \frac{P_{diss}}{2^{ENOB} \cdot 2BW} \quad \text{[pJ/step]}$$

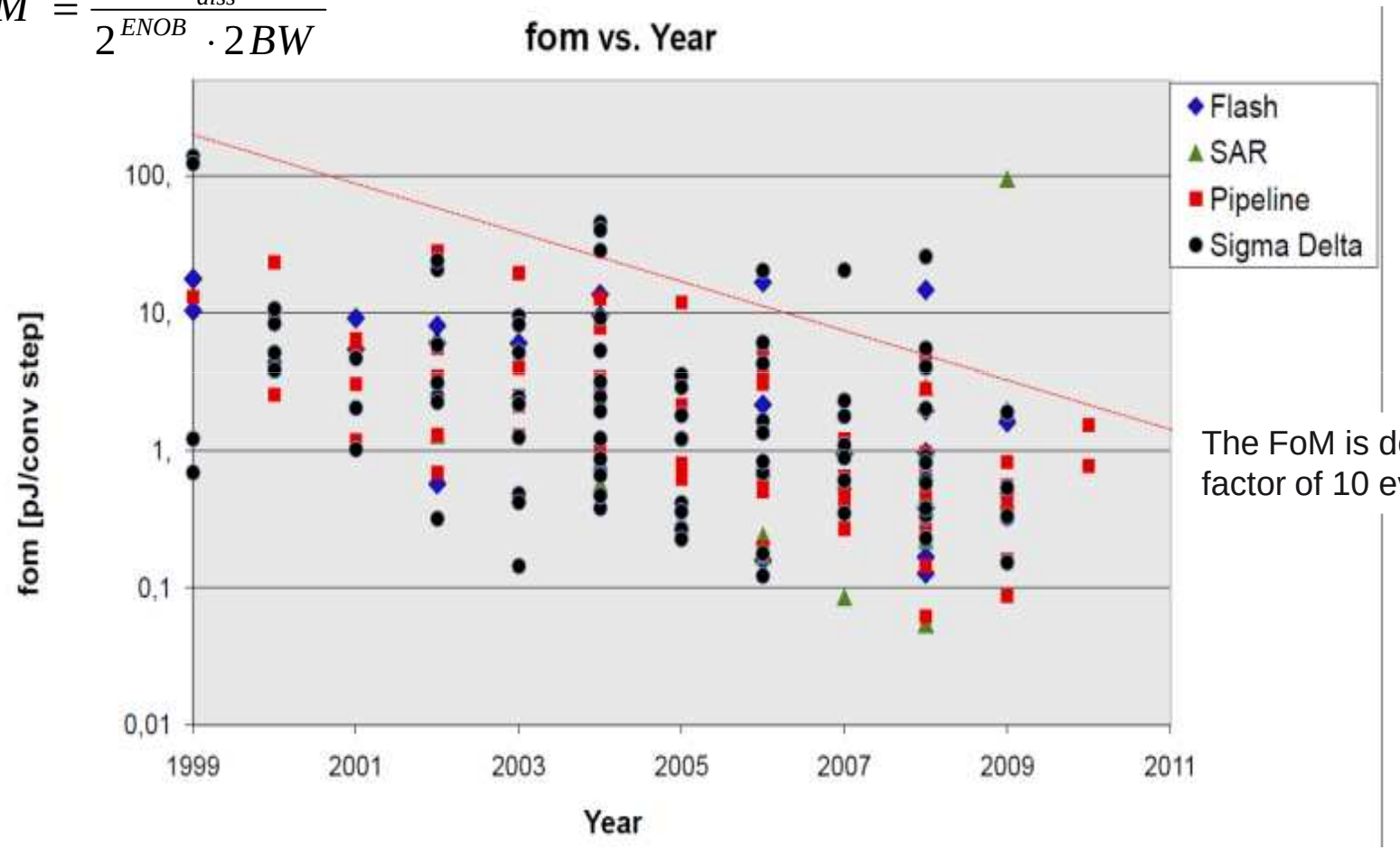
Bandwidth versus SNDR overview



Overview of the last decade ADCs published in ISSCC, VLSI and CICC conferences

Figure of Merit trends

$$FoM = \frac{P_{diss}}{2^{ENOB} \cdot 2BW}$$



The FoM is decreasing by a factor of 10 every 6 years.

Evolution of ADCs Figure of Merit over the years

Outline

- Introduction
- ADC fundamental architectures
- ADC performance: State-of-the-art
- Challenges and promising techniques
- Conclusion

ADC design in nanoscale CMOS

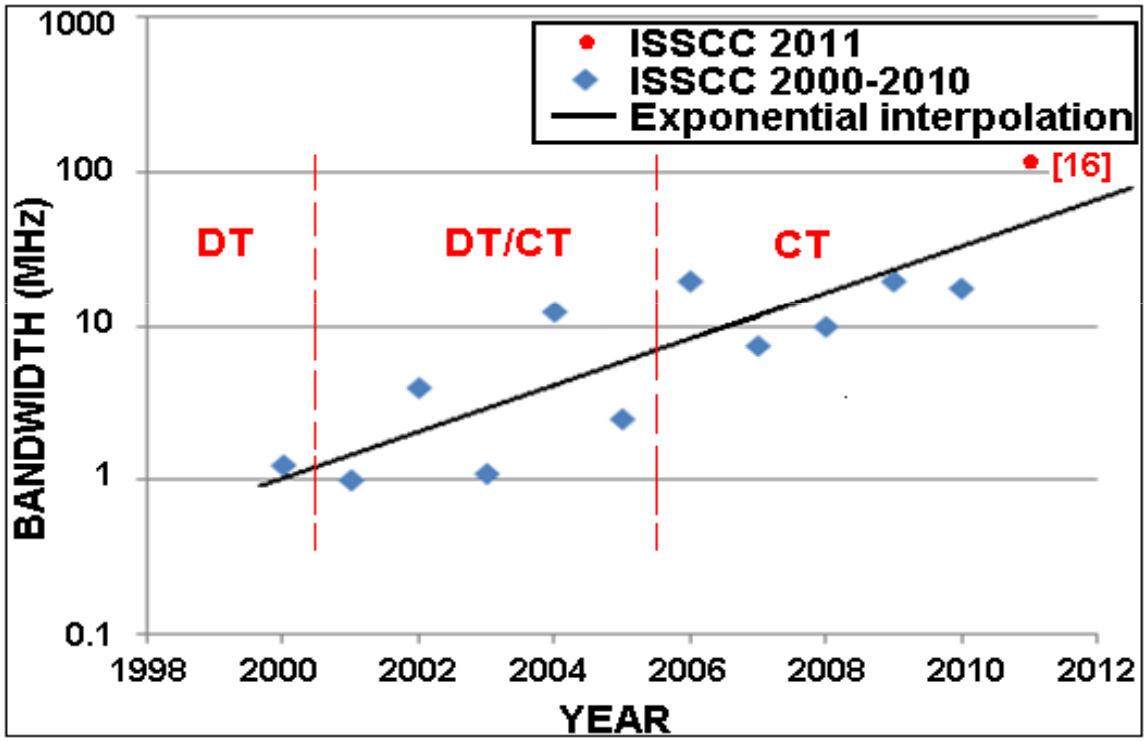
- Evolution of process technology
  - Area ✓
  - Bandwidth ✓
  - Linearity ✗

- Issues
  - Components matching and long-term reliability
  - Process variability
  - Flicker noise
  - High threshold voltage at low voltage supply

→ The design of an ADC becomes a serious challenge when high performances are targeted with low power constraint

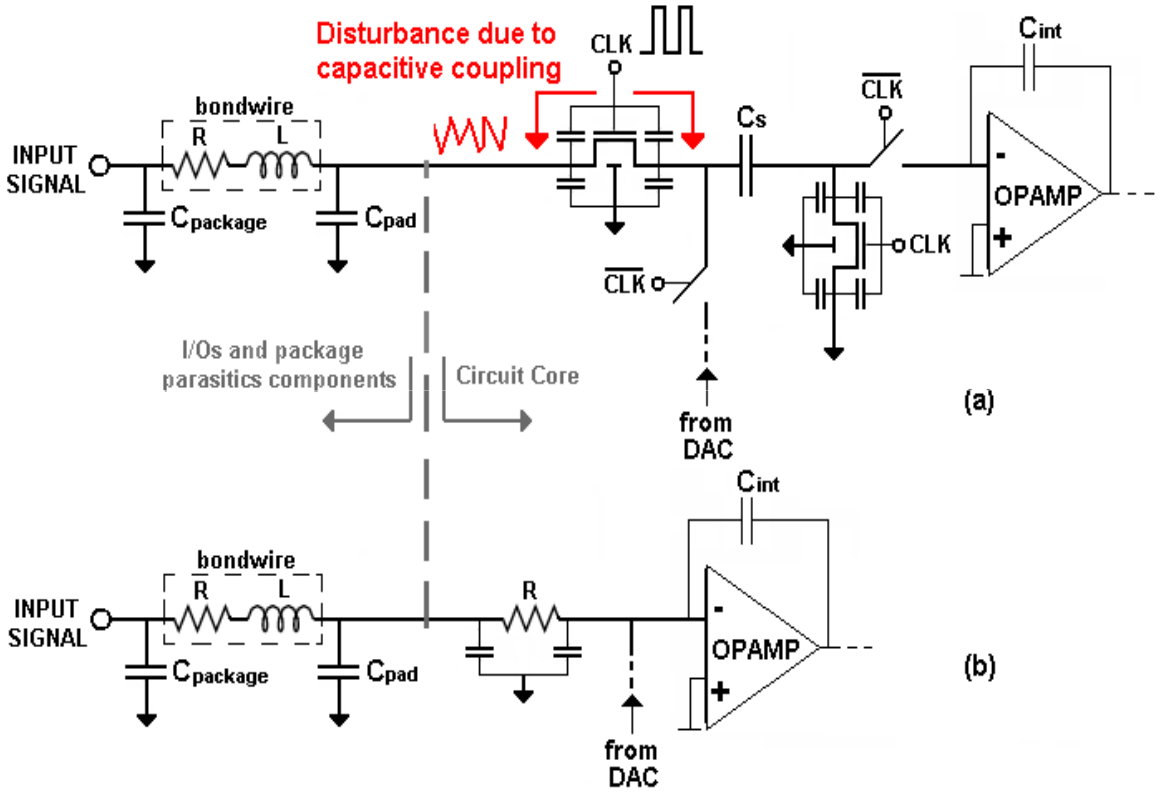
ΔΣ modulator and CT implementation

➡ Oversampled ADCs benefit of CMOS scaling because they trade sampling speed for resolution.



Bandwidth evolution over last decade of CMOS ΔΣ ADC with ENOB>11-bit, presented at ISSCC (2000-2011)

ΔΣ modulator and CT implementation



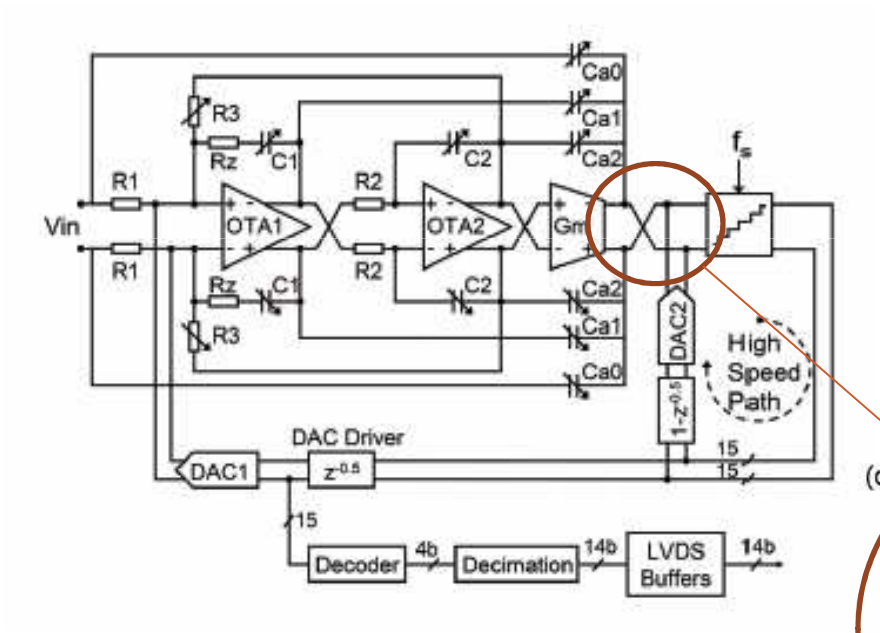
Simplified schematic of a ΔΣ front-end in
(a) discrete-time implementation,
(b) continuous-time implementation.

Advantages :
Speed
Power consumption
Easier to drive
Inherent anti-aliasing

Limitations :
Sensitivity to PVT variation
Loop delay
Clock jitter

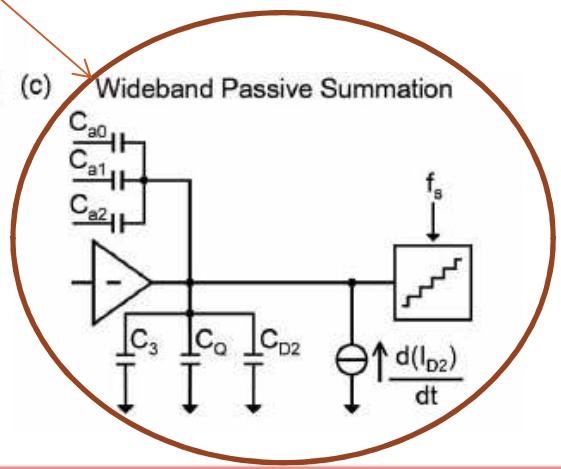
ΔΣ modulator and CT implementation

[16] M. Bolatkale et al., NXP Semiconductors, Eindhoven and DUT, Delft "A 4GHz **CT ΔΣ ADC** with 70dB DR and -74dBFS THD in **125MHz** BW," *ISSCC Dig. Tech. Papers*, pp. 470-473, Feb. 2011.
Implemented in **CMOS 45nm**

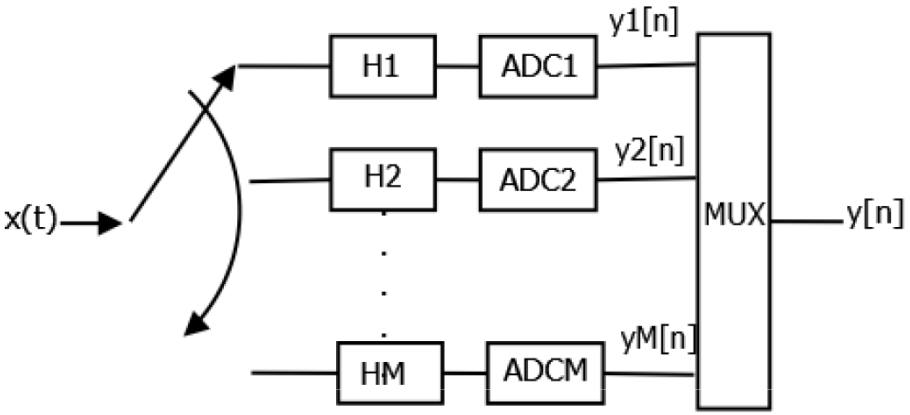


4b 3rd-order CT ΔΣ ADC

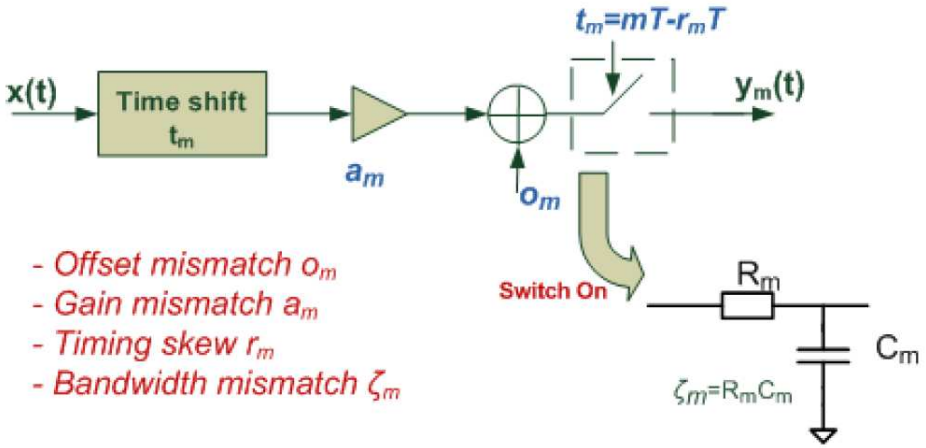
- The last integrator is implemented as a Gm-C integrator which absorbs C_Q, as well as the DAC2's output capacitance (C_{D2}), into its integration capacitance.



Parallel implementation



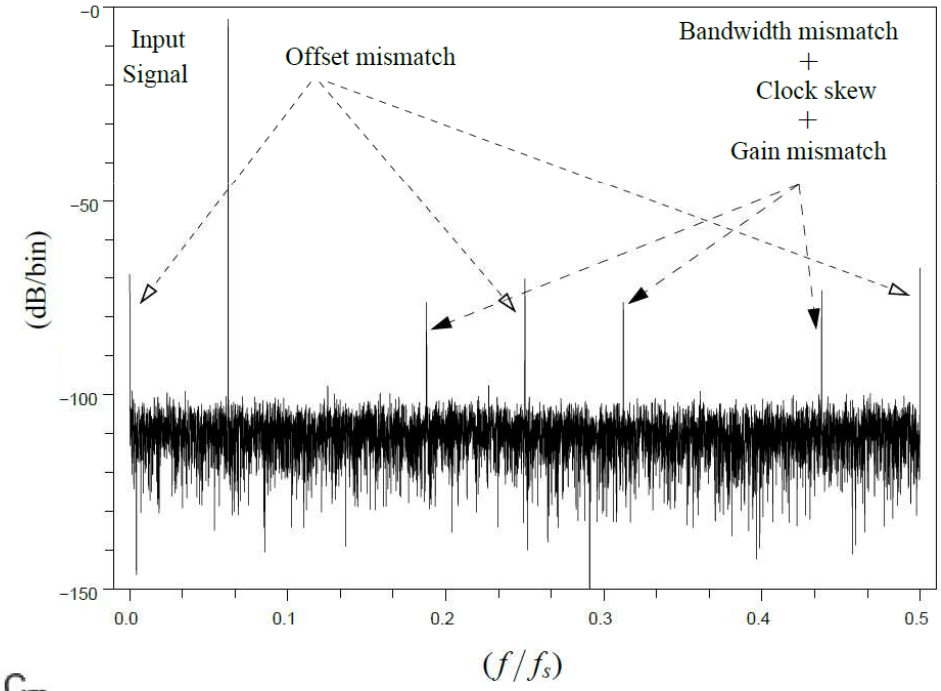
Time-Interleaved Architecture



- *Offset mismatch* o_m
- *Gain mismatch* a_m
- *Timing skew* r_m
- *Bandwidth mismatch* ζ_m

Advantage : Speed × M

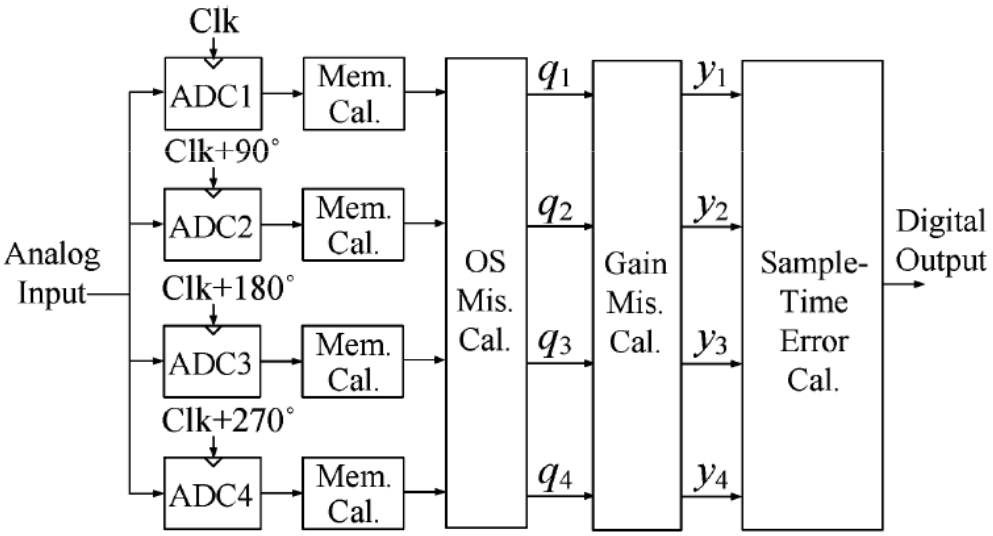
Limitations : Mismatch errors



additional tones caused by the presence of all mismatch errors

Parallel implementation and digital correction

Digital calibration techniques benefit from advances in nanoscale digital circuits and can be now implemented without suffering large cost in area and power.



Block diagram of the adaptive calibration system.

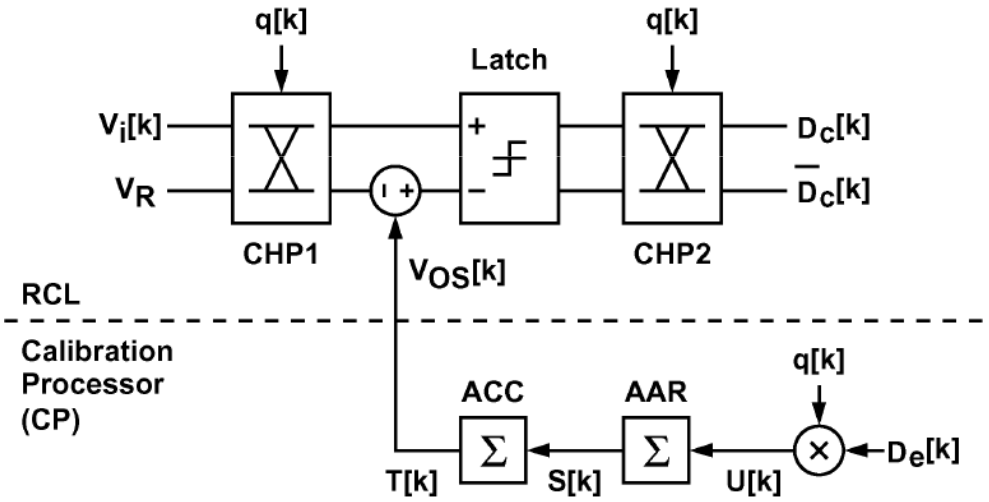
- 4 parallel pipelined ADCs with use of double sampling **to save power and die area**
- Offset foreground calibration by digitizing and subtracting the mean of each channel
- Digital background calibrations are used to remove gain and sample-time mismatches

[19] C. H. Law, P. J. Hurst and S. H. Lewis, "A Four-Channel Time-Interleaved ADC with Digital Calibration of Interchannel Timing and Memory Errors," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, Oct. 2010.

Parallel implementation and digital correction

[18] C.-C. Huang, C.-Y. Wang and J.-T. Wu, “A CMOS 6-Bit 16-GS/s Time-Interleaved ADC Using Digital Background Calibration Techniques,” *IEEE J. Solid-State Circuits*, vol. 46, no. 4, April 2011.

Statistics-based offset calibration technique

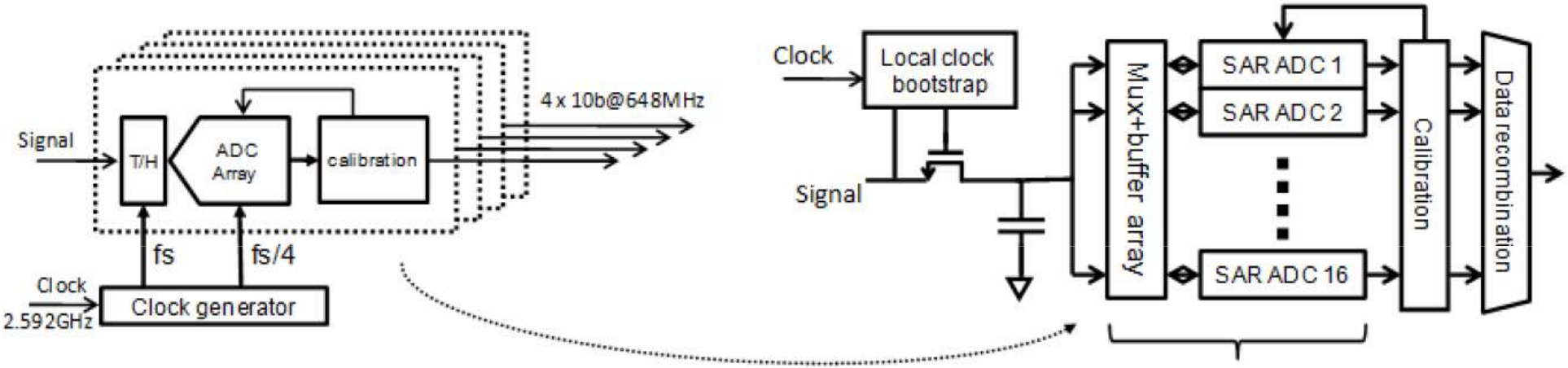


Background-calibrated comparator (BCC) block diagram.

- 8 parallel flash ADCs using latches without preamplifiers **to save power**
- Digital background calibrations are used to reduce the input-referred offsets of the latches
- Digital background offset calibration and digital background timing-skew calibration.

Parallel implementation

[20] K. Doris et al., NXP Semiconductors, Eindhoven, “A 480 mW 2.6GS/s 10b 65nm CMOS Time-Interleaved ADC with 48.5dB SNDR up to Nyquist ,” *ISSCC Dig. Tech. Papers*, pp. 180-182, Feb. 2011.



- 64 parallel SAR ADCs **naturally low power consuming**
- Interleaving hierarchy based on 4 T&H at 650MHz
- Calibration per ADC deals with offset, gain and DAC nonlinearities at start-up and makes non-binary-to-binary conversion prior to data recombination

Performance summary

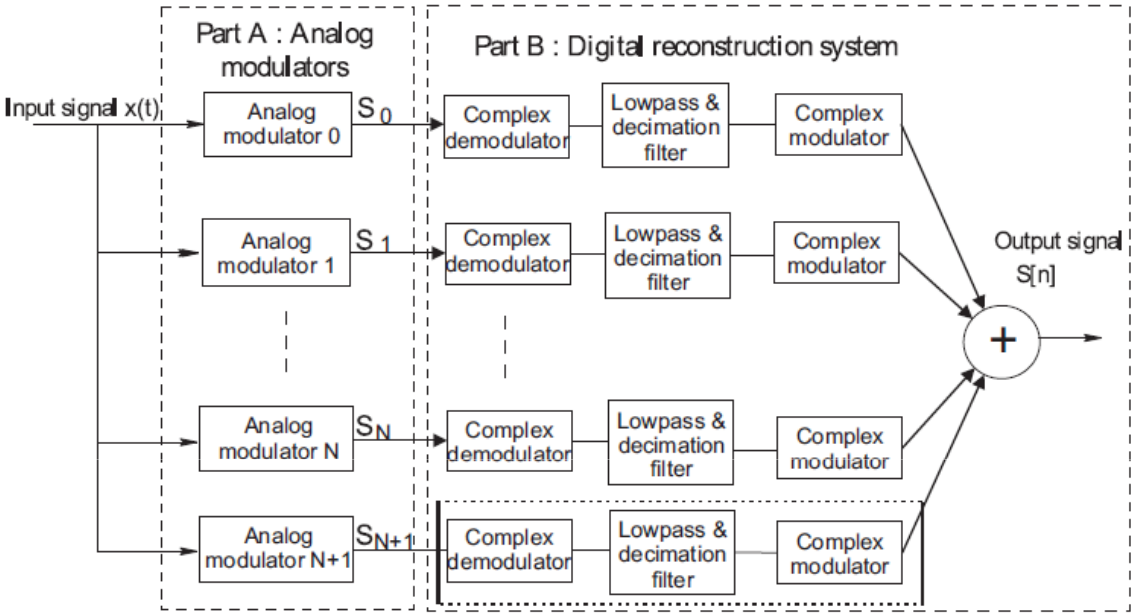
Ref / year	Architec Sture	Techno CMOS	Fs (GHz)	BW (MHz)	SNDR (dB)	Power (mW)	FoM (pJ/step)
[16] 2011	CT ΔΣ	45 nm	4	125	65	256	0.7
[18] 2011	TI Flash	65 nm	16	3000	28	435	3.5
[20] 2011	TI SAR	65 nm	2.6	1250	48.5	480	0.88
[21] 2010	TI Pipeline	90 nm	0.205	100	75.5	71	0.07 *

Performance summary for outstanding implementation of each architecture.

[21] M. Mohsen and M. Dessouky, “13-bit 205 MS/s Time-Interleaved Pipelined ADC with Digital Background Calibration,” ISCAS 2010, pp. 1727-1730, April 2010. *Simulation results

TI ΔΣ converter ?

- TI CT ΔΣ converters :
  - Hybrid filter banks
  - Frequency band decomposition
  - Very large band



P. Benabes, A. Beydoun, M. Javidan, "Frequency-Band-Decomposition converters using continuous-time Sigma-Delta A/D modulators," NEWCAS-TAISA'09, June 2009.

- TI DT ΔΣ converters
  - Abilities for reconfiguration :
  - High resolution / medium band
  - Medium resolution / Wide band

Planning R&D (2)

Wireless Systems (LTE-A, IMT Advanced, CRN, WSN)

Inter Carnot Franhofer TEROPP
Van-Tam/Patrick

Charge sampling, hybrid filter banks, parallel receiver, multi-path receiver, white spaces, sensing, cognitive radio

CATRENE PANAMA
Patrick/Patricia

Band-pass CT ΣΔ ADC, non linearity correction path of the base station PA

FP7 SACRA
Van-Tam/Hussein/Chadi/Patrick

CT ΣΔ ADC, sensing algorithms, cognitive engine and control, cognitive radio systems

ENIAC ARTEMOS
Van-Tam/Hussein/Chadi/Patrick

Sigma delta receiver, RF transceiver specifications for LTE-A, Low-power Reconfigurable ΣΔ ADC , Bandpass ΣΔ modulator with passive filter, sensing algorithms, mixed signal cancellation of interference, cognitive engine and control

CATRENE/ENIAC/FP7 (set-tup)
AppsGate/Quarante/R2S3 …

Circuits, algorithms, digital signal calibration and correction techniques, systems architecture, definition and specifications for STB (applications Gate), LTE-A and Beyond, Wireless Sensor Network

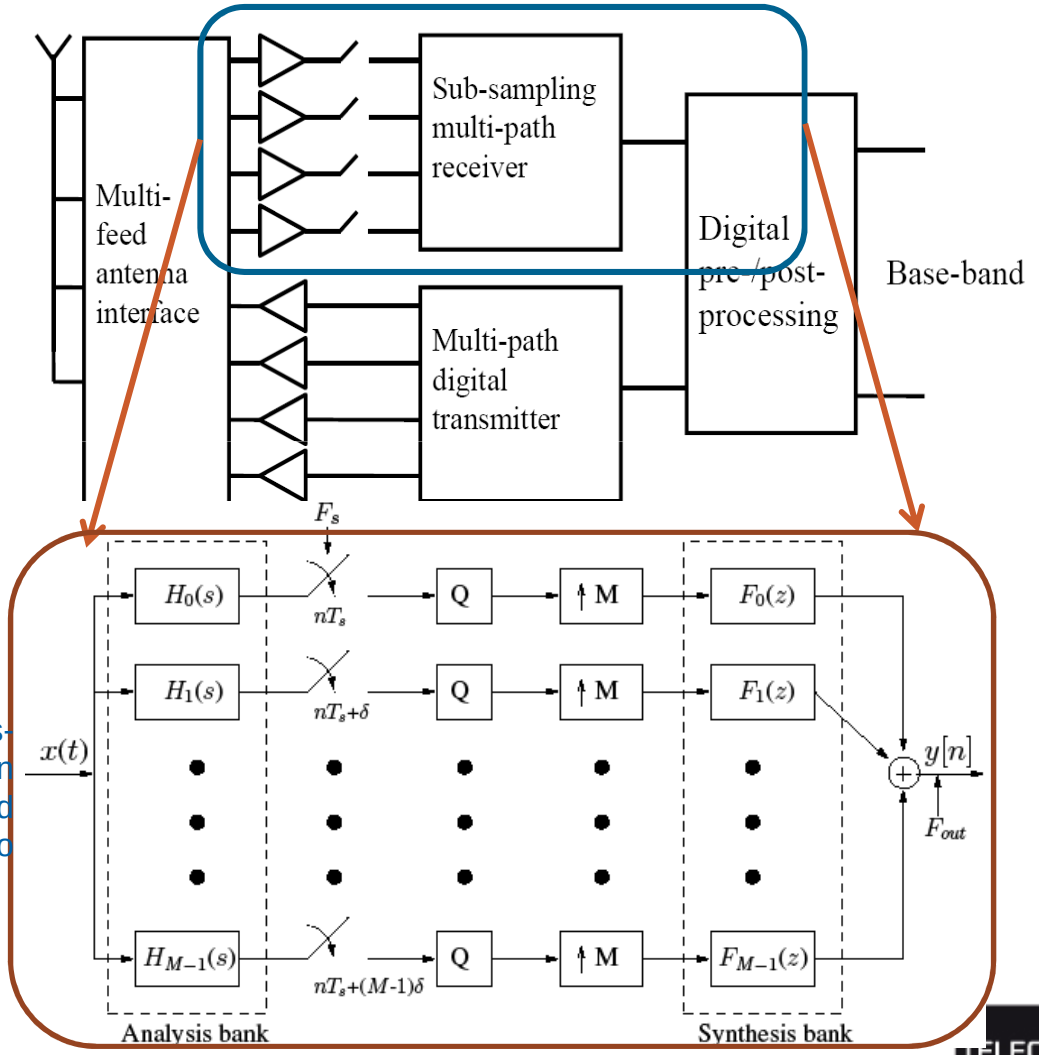
Joint laboratory ADC NXP
Patricia/Van-Tam/Hussein/Patrick/Hervé

ADC design, Time Interleaved ADC, pipelined ADC, CT ΣΔ ADC, reconfigurable ADC

1ier sem 2011 | 2ième sem 2011 | 1ier sem 2012 | 2ième sem 2012 | 1ier sem 2013 | 2ième sem 2013 | 1ier sem 2014 | 2ième sem 2014

TEROPP project : Proposal for Multipath frequency agile RF receiver

- **Multipath receiver**
  - Agile RF receiver
  - CMOS Technologie
  - Spectrum sensing
  - Focus on narrowband
  - Hybrid Filter Band



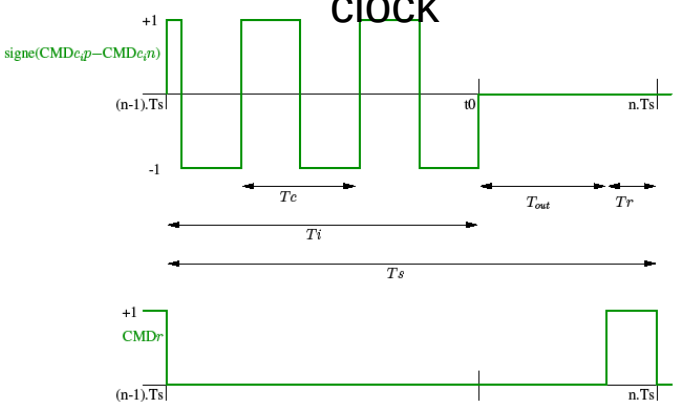
A. Gruget, M. Roger, V-T Nguyen, C. Lelandais-Perraud, P. Benabes, P. Loumeau, "Optimization of Bandpass Charge Sampling Filters in Hybrid Filter Banks Converters for Cognitive Radio applications," ECCTD 2011

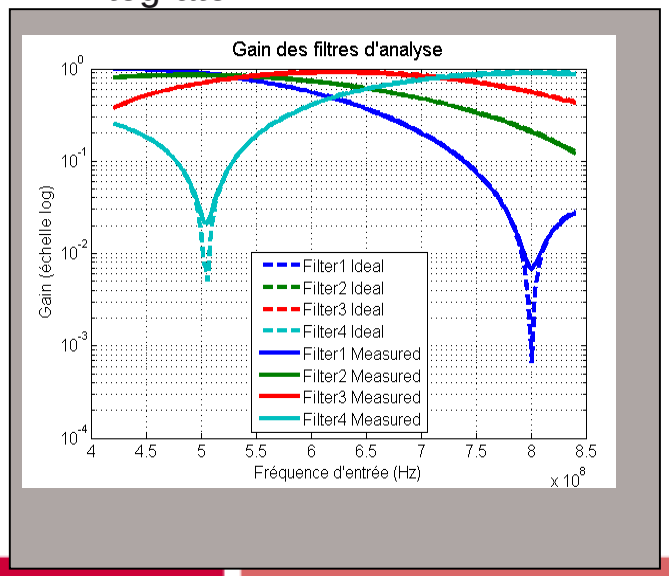
B. Patent

TEROPP Innovative solution

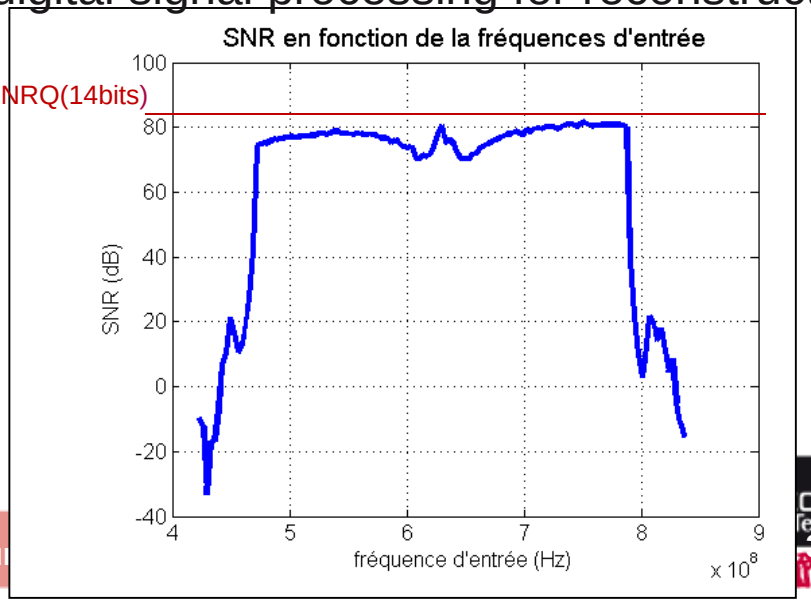
- **After the LNAs : samplers give different bandpass filters by control clocks**
- **Example**
  - Band : [470 790] MHz
  - 4 channels
  - F_{sample} = 210 MHz
  - F_{center}=[480 560 672 840] MHz
  - $F_{integrate}$=[320 373 336 336] MHz

Example of control clock

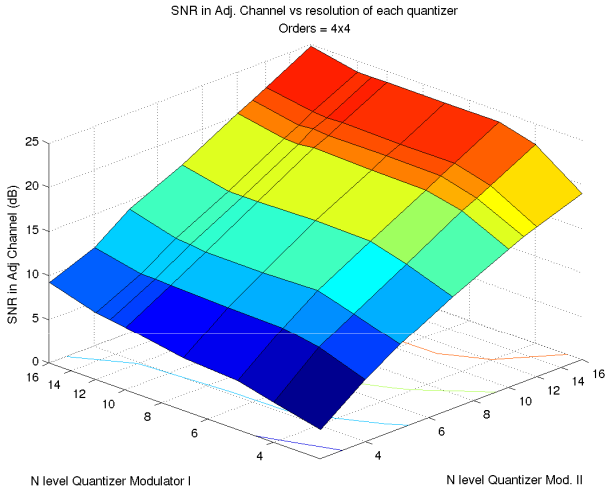


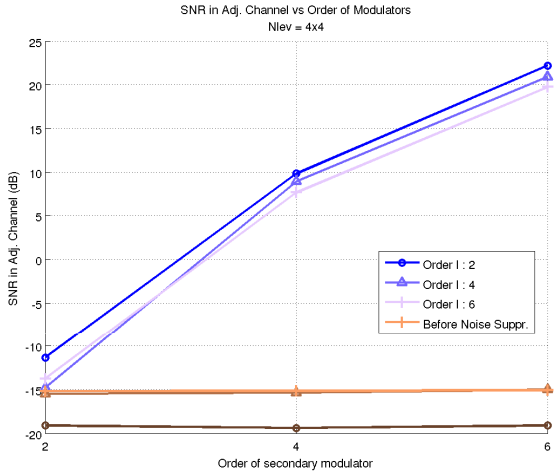


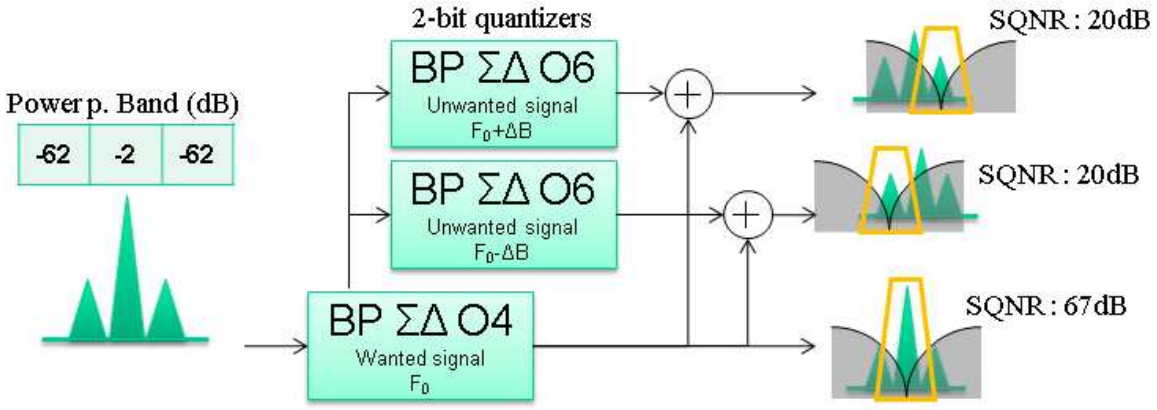
Need digital signal processing for reconstruction



Innovative solution : BP ΣΔ ADC





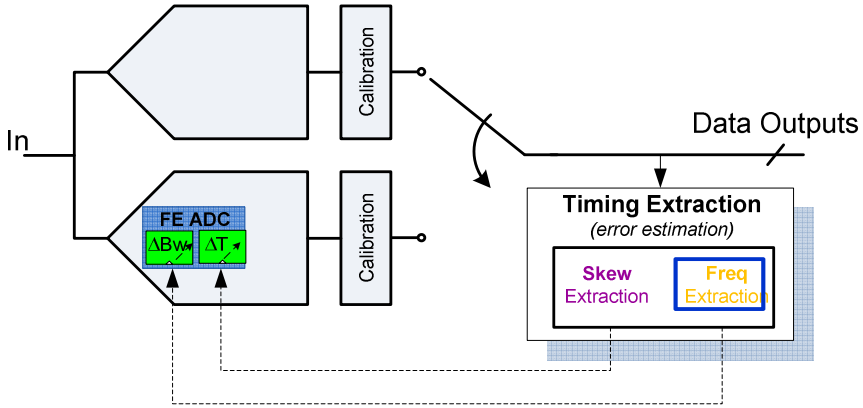


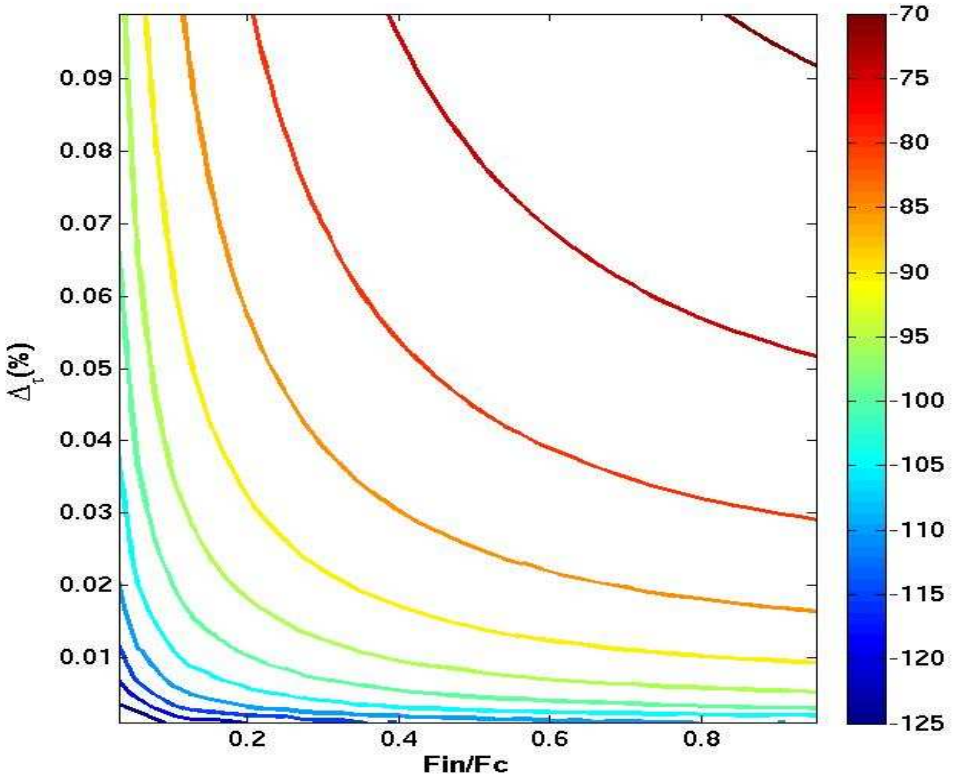
Time Interleaved Pipeline ADC (Bandwidth Mismatch Extraction)

SFDR > 85dB for Fin/Fc=0.4 => Bandwidth mismatch ≤ 0.03%. *(for Fc=1GHz)*

$$SFDR = 20\log\left\{\frac{H_1+H_2}{H_1-H_2}\right\}$$

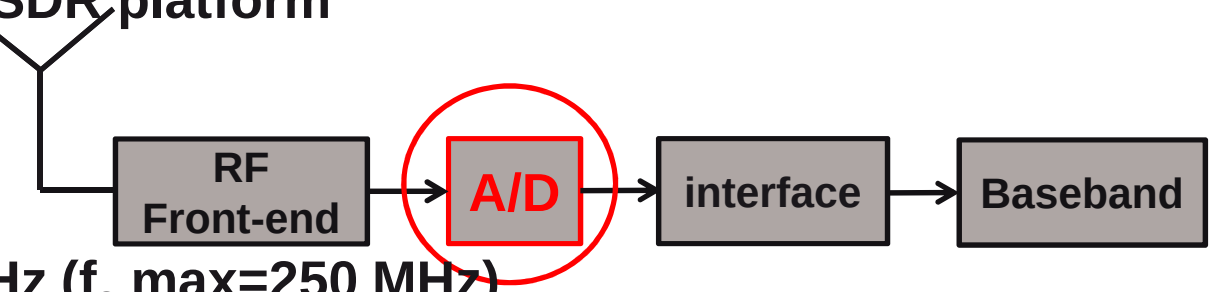
$$H1=\frac{1}{1+j\omega\tau_1};\ H2=\frac{1}{1+j\omega\tau_2}: Frequency\ responses\ of\ each\ channel$$





High-speed ADC design for cognitive radio

- Actual solution uses a pipeline ADC from Texas Instruments (ADS5484) is embedded on the IIS SDR platform

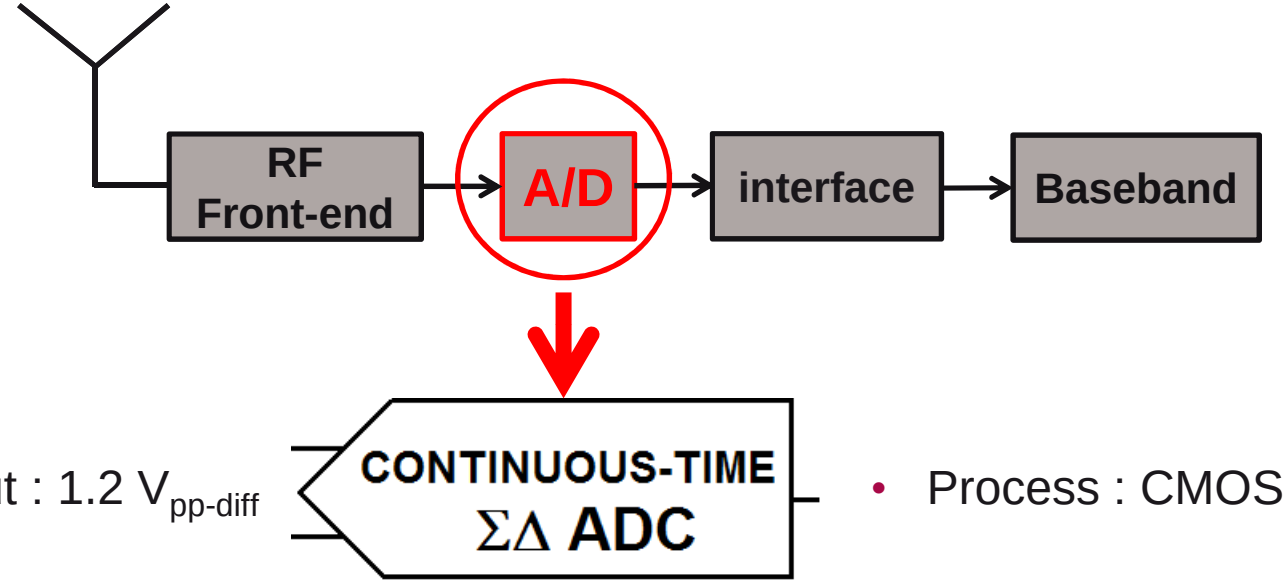


ADS5484
-SNR=75.9@f_{in}=30MHz
-SFDR=91@f_{in}=30MHz
-Power=2.16 W@f_{in}=30MHz (f_s max=250 MHz)
-Temp=[-45°C:+85°C]
-Process : BiCOM3 (BiCMOS on SOI)

- High power consumption ! Even in sleep mode (70mW) ☹

Goal of the project

- **Solution proposed by IT is based on Zero-IF scenario with a Continuous-Time ΣΔ ADC**



- Max input : 1.2 $V_{pp\text{-}diff}$
- Process : CMOS 65nm

- **Dynamics performances of the ΣΔ ADC @f_{in}=[0:40MHz] :**
  - SNR=76dB
  - SFDR=88dB
  - $Power_{ADC}$ < 100mW (ADC core only, I/Os buffers not included)

FoM=0.24pJ/step

Outline

- Introduction
- ADC fundamental architectures
- ADC performance: State-of-the-art
- Challenges and promising techniques
- Conclusion

Conclusion

- **For future 4G/LTE/LTE-A radio requirements :**
  - ΔΣ converters and CT implementations
  - Pipeline converters
- **Parallel implementation and increasing use of calibration and digital correction**
- **For multi-channel cable receiver :**
  - TI SAR converters
- **An attractive solution:**
  - CT BP ΔΣ converters and Parallelism

References

•B. Murmann, "A/D converter trends: power dissipation, scaling and digitally assisted architectures," in *Proc. IEEE Custom Integrated Circuits Conference*, pp.105-112, Sept. 2008.
•R. H. Walden, “Analog-to-digital converter survey and analysis,” *IEEE J. Sel. Areas Commun.,* vol. 17, pp. 539–550, Apr. 1999.
•B. E. Jonsson, "A survey of A/D-Converter performance evolution," in *Proc. 17th IEEE International Conference on Electronics, Circuits, and Systems*, pp.766-769, Dec. 2010.
•L. L. Lewyn, T. Ytterdal, C. Wulff and K. Martin, "Analog circuit design in nanoscale CMOS Technologies," in *Proceedings of the IEEE*, vol. 97, no. 10, pp. 1687-1714, Oct. 2009.
•A. Matsuzawa, "Trends in high speed ADC design," in *Proc. 7th International Conference on ASIC*, pp.245-248, Oct. 2007.
•R. Schreier, G. C. Temes, “Understanding Delta-Sigma Data Converters,” *ed. IEEE Press*, 2005.
•c.
•J. Brunsilius et al., “A 16b 80MS/s 100mW 77.6dB SNR CMOS Pipeline ADC,” in *Proc. ISSCC Dig. Tech. Papers*, pp. 186-188, Feb. 2011.
• A. M. A. Ali et al., “A 16-bit 250-MS/s IF Sampling Pipelined ADC With Background Calibration,” *IEEE J. Solid-State Circuits*, vol. 45, no. 12, May 2010.
•R. Payne et al., “A 16-Bit 100 to 160 MS/s SiGe BiCMOS Pipelined ADC with 100 dBFS SFDR,” *IEEE J. Solid-State Circuits*, vol. 45, no. 12, May 2010.
•W. Yang et al., “A 100mW 10MHz-BW CT SD Modulator with 87dB Dr and 91 dBc IMD,” *ISSCC Dig. Tech. Papers*, pp. 498-499, Feb. 2008.
•G. Mitteregger et al., “A 20-mW 640-MHz CMOS Continuous-Time ΣΔ ADC With 20-MHz Signal Bandwidth, 80-dB Dynamic Range and 12-bit ENOB,” *IEEE J. Solid-State Circuits*, vol. 45, no. 12, Dec. 2006.
•D. Gubbins, Sunwoo Kwon, Bumha Lee, P. K. Hanumolu and Un-Ku Moon, “A Continuous-Time Input Pipeline ADC with Inherent Anti-Alias Filtering,” in *Proc. IEEE Custom Integrated Circuit Conference*, pp. 275-278, Sept. 2009.
•M. Bolatkale et al., “A 4GHz CT DS ADC with 70dB DR and -74dBFS THD in 125MHz BW,” *ISSCC Dig. Tech. Papers*, pp. 470-473, Feb. 2011.
•C. Jabbour, D. Camarero, V.T. Nguyen and P. Loumeau, “Optimizing the number of channels for time-interleaved sample-and-hold circuits,” in *Proc. Joint 6th International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference*, pp. 245-248, June 2008.
•C.-C. Huang, C.-Y. Wang and J.-T. Wu, “A CMOS 6-Bit 16-GS/s Time-Interleaved ADC with Digital Background Calibration,” in *Proc. IEEE Symposium on VLSI Circuits/ Dig. Tech. Papers*, pp. 159-160, June 2010.
•C. H. Law, P. J. Hurst and S. H. Lewis, “A Four-Channel Time-Interleaved ADC with Digital Calibration of Interchannel Timing and Memory Errors,” *IEEE J. Solid-State Circuits*, vol. 45, no. 10, Oct. 2010.