- **Name of the company *:** STMicroelectronics
- **City and zip code *:** Crolles, 38926
- **Name of the partner academic laboratory (so already known):** TIMA, CEA-LIST
- **Title of research theme (without any confidential character) *:**

3D Heterogeneous technologies for Digital secured & sovereign solutions

- **Description of the theme of research (without any confidential character) *:**

Digital ASICs are heavily impacted by intrusion attempts, carried out by software and/or hardware attacks. Ensuring their resilience is critical for sovereign ASICs or solutions dedicated for the automotive market.

The advent of heterogeneous 2.5D/3D technologies offers an opportunity in the construction of secure circuits, by allowing the development and use of a secure hardware, which can accommodate an assembly of chips from various origins, while guaranteeing the secure operation of the whole system.

- **Description of job *:**

The target of this thesis is to develop the digital hardware that will guarantee the integrity of the heterogeneous system. You will join the team in charge of exploring heterogeneous 2.5D/3D solutions, and will work closely with the research laboratory partner of this project. The team is composed of experts in design and robustness, as well as phd students and interns.

Your objective will be to investigate the potential sources of failure of a system-on-chip, and the existing hardware solutions. You will then propose secure solutions using the design of heterogeneous system-on-chip, assembled in 2.5D or 3D. At the end of the thesis, you will be able to propose a reusable hardware chip that can be interfaced with different types of computing units (CPU, AI).

- **Function *:** PhD Student
- **Research Profile*:** Semiconductors, digital circuits
- **E-mail address to which the candidate has to send his candidacy :** fady.abouzeid@st.com