Opening for PhD thesis

Sensitivity Analysis and Design Methodology for Secure Digital Circuits against X-Rays

Context

In digital applications, electronic components must guarantee the security of the processed information. Attacks based on laser or EM illumination, electrical pulses on the power supply or the clock (glitches) or Focused Ion Beam (FIB) are now well-known threats. However, the search for new attack techniques remains a very active field: the use of X-ray illumination has been recently proved feasible to alter the content of memory cells.

In this context, the MITIX project (***M****odification non* ***I****nvasive de circui****T****s* ***I****ntegrés par rayons* ***X***, Noninvasive modification of integrated circuits by X-Rays) aims at proving that X-Rays can effectively constitute a serious threat for secure implementations, even when more affordable equipment is used. Within the projects, several experimental campaigns will be the basis for modelling the interaction between RX beam and the transistors, and hence propose design guidelines and/or solutions in order to protect against this novel attack technique.

Description

The candidate is expected to analyze the sensitivity of MITIX circuits under X-ray beams thanks to simulation models and compare them with experimental results. The goal will be to reproduce the experimental conditions, in particular the positioning and the interaction of the X-ray beam with respect to the circuit, possibly extending the analyses on the circuit (a few selected positions) and extract sensitivity maps extended to a larger area of the topology.

The candidate will then be able to use the developed models and flow in order to evaluate hardening techniques or fault attack countermeasures. This subtask will consist in using the multi-physics and multi-level methodology to study and optimize the layout/routing of the cells, and extract high-level models of the injected faults. This will be essential in order to evaluate techniques from the state of the art, and propose novel solutions against fault attacks.

Profile

The candidate should be in possession of a BAC+5 degree in Electrical or Computer Engineering.
Knowledge of low-level (transistor/gate level) simulation techniques will be greatly appreciated.
Knowledge of hardware security and physical attacks is a plus, but not strictly required.

The PhD will be based at TIMA Laboratory, Grenoble, France, and codirected with ONERA, Toulouse, and will begin approximately on October 2021 and last 3 years. Gross salary will be about 25600€/year (net about 20590€/year, before income taxes).

Contacts

The potential candidates should send their CV, motivation, and recommendation letters to:

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