AnadyneDesigner
Preliminary Information

AnadyneDesigner – Version 1.0
Field Programmable Analog Array Design Software

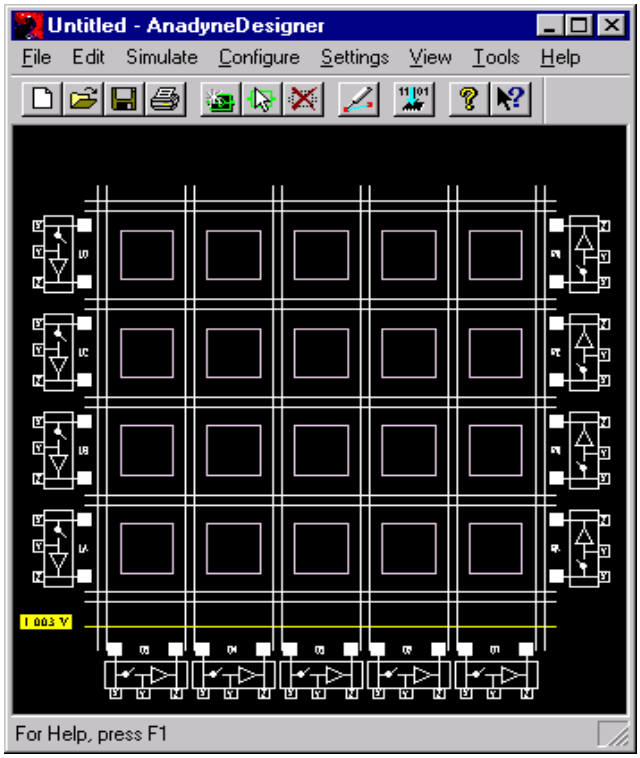
Anadyne Microelectronics Field Programmable Analog Arrays bring to analog what FPGAs brought to digital: extremely rapid production and prototype circuit realization with field re-programmability. AnadyneDesigner is the PC hosted design system that gives you access to this pivotal technology.

AnadyneDesigner presents the user with a simplified view of the FPAA chip. Constructing a circuit is accomplished in an intuitive drag and drop GUI. Input and output connections are made with a pair of equally intuitive mouse clicks. IPmodule parameters are set with sensible pop up menus. AnadyneDesigner won't let you make a mistake; your circuits are correct by construction. A few minutes to design your analog circuit, and a few seconds to generate the configuration memory image for the FPAA and you're done. Say goodbye to soldering irons, hay wires, trim pots and discrete passive components. Building analog circuits just got a whole lot easier.

Anadyne's FPAAs coupled with the intuitive AnadyneDesigner software gives both digital and analog designers a unique competitive advantage in designing analog circuits that can't really be compared to any other design system in existence. Quickly constructed, accurate, drift free, temperature compensated and *programmable* analog circuits are now yours. Imagine the power of programmable with the versatility of analog.

The software installs easily and includes an extensive library of proven high performance IPmodule circuits. Configuration memory images are assembled with just a click of a mouse. A configuration file is then used to boot the FPAA in any one of several methods. Analog design will never be the same.

Benefits



- Intuitive Drag and Drop GUI
- Extensive Context Sensitive On Line Help
- Painless Installation
- Extremely Rapid Analog Design
- Minutes not weeks to re-spin a new design idea
- In Circuit Programmable
- Behavior can be adjusted on the fly
- Re-Configurable Using Conventional Logic
- Re-Configurable using Serial PROMs
- Re-Configurable using Microcontrollers
- Flexible Internal Clock and Routing Resources
- No More Trimming Components
- No More Tuning Components
- Extremely Stable over Voltage and Temperature
- No Component Aging
- Reliable and Repeatable Performance

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Quick Start

What does this software do?

AnadyneDesigner software allows you to quickly and easily construct complex analog circuits by selecting, placing and wiring building-block circuits referred to as IPmodules. The analog circuits that you build may then be down-loaded to Anadyne's Field Programmable Analog Array (FPAA) chips via your PC's serial port. The chip will then begin functioning as the circuit you constructed. You can see the results of your analog design immediately using a signal generator and an oscilloscope.

The chip can be reprogrammed as many times as desired so you can try out as many circuits as you like.

Also note that multiple, independent circuits can be constructed and run simultaneously, each with its own independent inputs and outputs. For example, you could have 3 gain stages, 2 rectifiers and a comparator operating totally independently and simultaneously each with its own input and output terminals.

How does an Anadyne FPAA work?

Anadyne's Field Programmable Analog array is based on switched-capacitor technology. Switched capacitor circuits have been around for several decades and their operation is well characterized. The complexity of switched capacitor circuits (along with the mathematics used to design them) can be daunting, and as such has kept their use limited to special function integrated circuits. Many high performance filter chips available today are based on switched capacitor technology. Anadyne has combined switch capacitor circuit topology, with FPGA like programmability and established the only truly flexible Field Programmable Analog Array.

There are twenty usable analog zones on the chip. Each zone contains an op-amp and five programmable feedback capacitors. Each capacitor is actually made up of a bank of 255 tiny capacitors that can be switched on or off, allowing for one of 255 different values. The capacitor values are set using "static" switches. There are also "dynamic" switches on the chip that handle the dynamic switching that makes a capacitor function as if it were a resistor. There are also dynamic switches that switch with respect to the phase of the input signal. There are also numerous other static switches that allow the capacitors and op-amp within each analog zone to be connected in various ways.

In addition, there are switches that allow local connections to be made between the components of two zones. There are also "global wires" on the chip that allow connections between zones that are so far apart that they cannot be connected using the local interconnect scheme.

AnadyneDesigner's IPmodule library, is composed in part of switch settings that set up the internal connectivity of the op-amps and capacitors of one or more zones. AnadyneDesigner handles all of the details for you so you don't have to learn about all of the internal switches. All you have to do is select the IPmodules you want to use, connect them with "wires", adjust each IPmodule's parameters using a pop-up menu, download the data to the chip and see the results on your oscilloscope.

Quick Test Drive – Simple Example Circuit

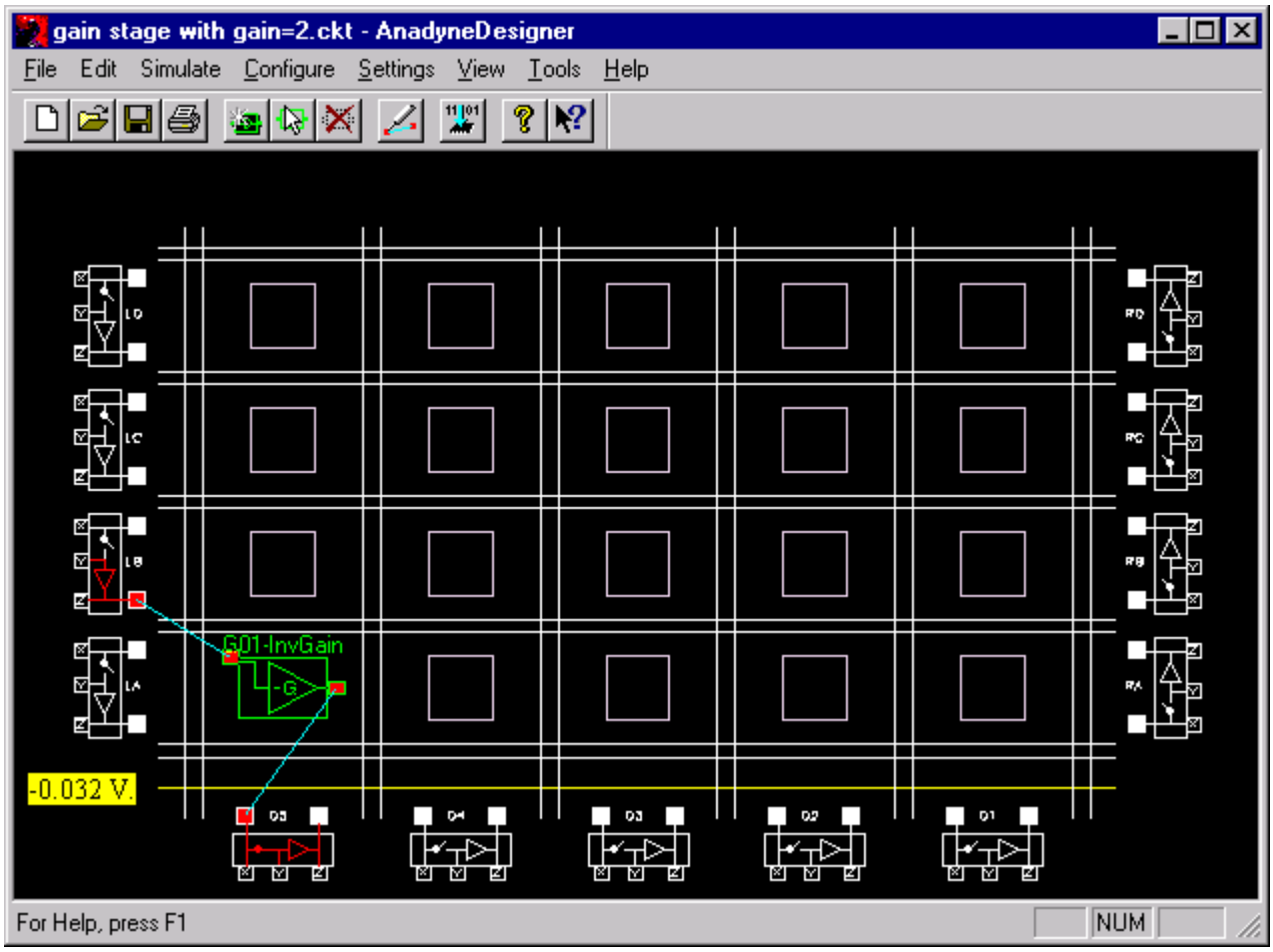
Chances are that once you've worked through this section, you'll probably abandon the manual in favor of simply "playing" with the design system on your own. It's that easy. Still though, this manual contains all the detailed information you may ever need to run AnadyneDesigner.

The quickest way to put a circuit up on the screen is to use one of the example circuits.

Lets try a simple *inverting gain stage*:

1. In the AnadyneDesigner software window, use the left mouse button and click on the "file" menu item. This brings up the "file" menu pull-down.

2. Click on the “Open . . .” menu item. This brings up a file selection dialog box.
3. You will see an “Examples” folder within the AnadyneDesigner installation folder in the window. Use the mouse to place the cursor over the “Examples” folder and double-click the left mouse button. This will display a list of example circuits in the window.
4. Locate the “gain stage with gain=2.ckt” entry, place the cursor over it, and double-click the left mouse button. The gain stage circuit will be loaded into AnadyneDesigner software and displayed in the lower left corner of the AnadyneDesigner software display screen as shown below.



Note that the green object labeled “G01-InvGain” is placed over one of the twenty chip zones (squares on the screen) indicating that the zone is being occupied. Also note that the InvGain IPmodule receives its input from the output terminal of the IO Cell labeled LB and sends its output to the input terminal of the IO Cell labeled D5.

In the LB IO Cell, the op-amp has been turned on so (colored red) that you can connect external stimulus to the Y terminal of the IO Cell. Using the Y terminal for your input buffers the input signal such that the FPAA does not unduly load it.

The voltage of the input signal should not exceed 5 volts peak-to-peak of course (the chip’s analog signal ground is at +2.5 volts). A signal generator can be used to provide this input.

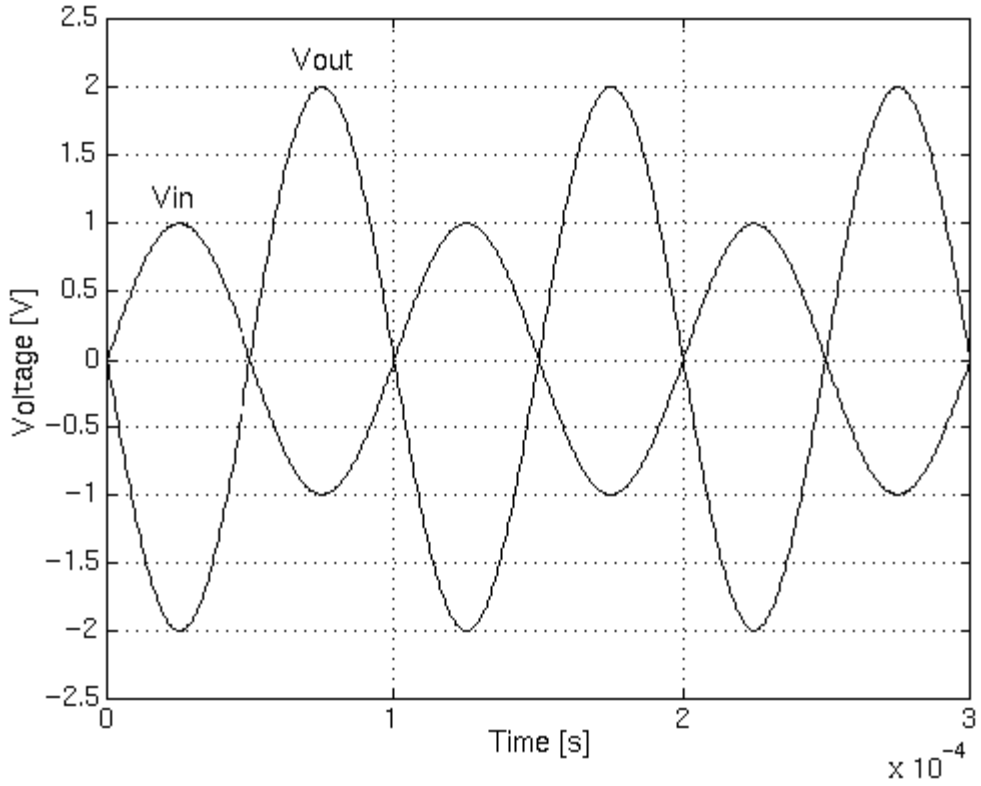
In the D5 IO Cell, the switch and the op-amp have both been turned on so that you can inspect the output by attaching an oscilloscope probe to any of the IO Cells pads, X,Y or Z. Using the Z pad as the output terminal will buffer the FPAA circuit and prevent the external world from unduly loading down the gain stage.

Yes, it really is that simple.

Download Data to the Serial Port

Now assuming you have some form of an FPAA evaluation board connected up to your PC's serial port, and further assuming that a signal generator and oscilloscope are attached to the proper terminals, we are now ready to download the configuration data to the chip. The gain setting for the InvGain IPmodule is "2" and the output signal will be inverted.

Downloading to an Anadyne FPAA is accomplished by selecting the menu item Configure → Write configuration data to Serial Port. There will be a bell signifying start of download. When you hear a second bell, the download is complete and the circuit should immediately begin working as an inverting gain stage. The download takes approximately 3 seconds. If you don't hear the second bell you will want to investigate possible serial port communications problems.



The gain of the InvGain IPmodule for this circuit is set to two. A right click over the InvGain IPmodule will pop-up the Set IPmodule Parameter dialog box. Adjust the gain to some new value then again download the data to the Serial Port to immediately see the effect of the new gain value on the amplitude of the output waveform. No trips to the little drawers full of resistors, no squinting to try and make out the infinitesimally small printing on the capacitors, no projectile component leads as you snip them to length, no molten hot solder flux sputtering up to your eyes, no acrid solder fumes burning your eyes and throat. Sorry we took all the "fun" out of analog design.

Brief Tutorial – Creating a New Circuit

If you are thinking that you already know most of what you need to drive this design system, then you're not far from wrong. Still though it will be instructive to go through at least one "from scratch" design just to make sure we cover all the bases. The following simple example is based on the popular AN10E40 array.

The design steps are straight forward and have a natural flow. For any design, you follow the same basic steps:

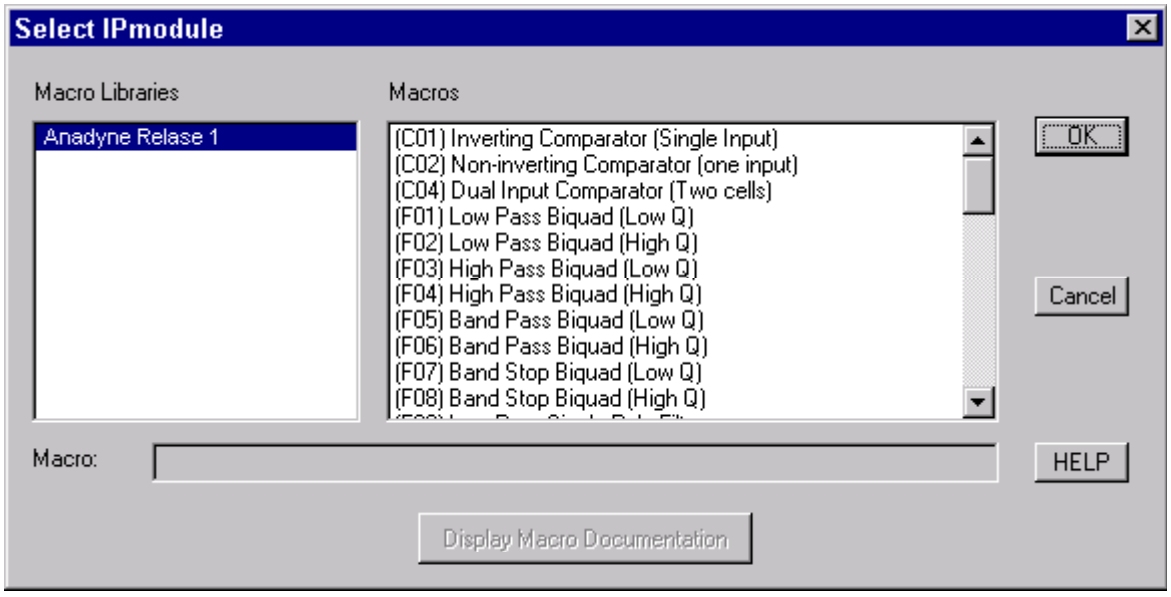
- Select and place IPmodules
- Set IPmodule parameters
- Connect the IPmodules and IO Cells with wires
- Power up the IO Cells
- Download the configuration data to the FPAA

Start with a Blank Design Window

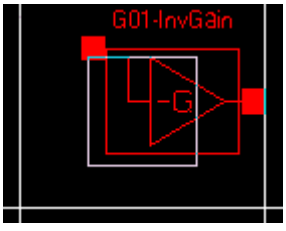
At any point, you can choose File → New Design and all contents of the main window will be cleared.

Select and Place IPmodules

Click on the  symbol in the tool bar just above the main window (or type the m keystroke shortcut) to bring up the Select IPmodule dialog box. Use the scroll bar on the right to scroll down to the (G01) Inverting Gain Stage. Place the mouse pointer over it and do a left double-click. (A single left click to select the IPmodule and another left click over the OK button (or hit your Enter key) will also work. This is all typical GUI interface behavior.)



The "Select IPmodule" pop-up will go away and a ghosted (red) version of the gain stage IPmodule symbol will be attached to your mouse cursor.



Place the image over the lower left zone marker in the design window. (You could place it on any of the 20 zones but, for this tutorial, we choose the lower left corner.) Click the left mouse button to drop a copy of the IPmodule down. The IPmodule will have been "placed" and hence changes to green.

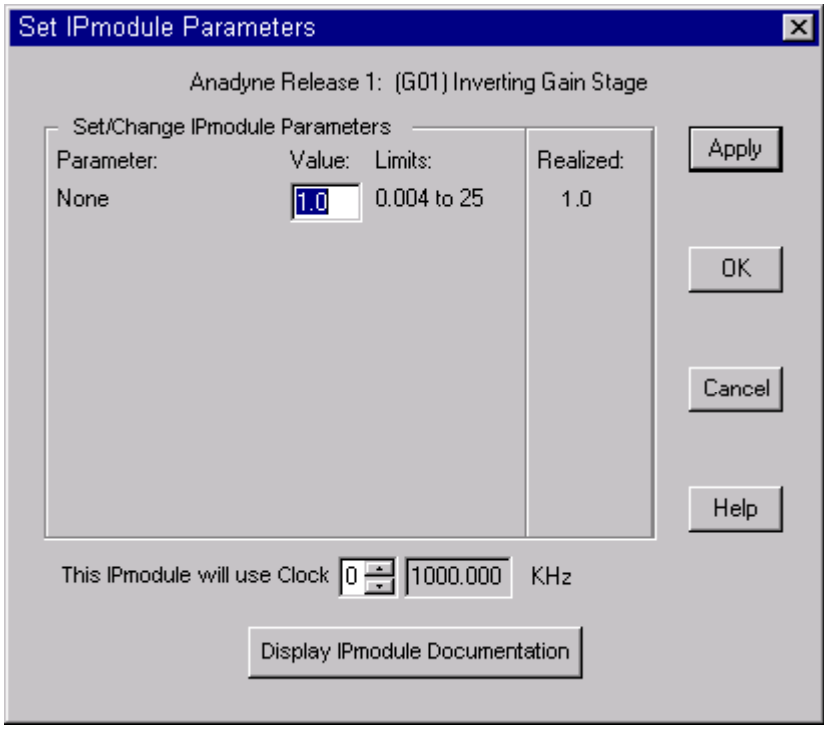
Set IPmodule Parameters

Right click over the IPmodule. The Set IPmodule Parameters dialog box will pop up. The contents of this box varies with the IPmodule selected, but in general contains all the user adjustable parameters for that particular sub-circuit.

In this particular instance, the only parameter to set for the gain stage is its gain. The "realized" column reflects what the FPAA will be able to actually do.

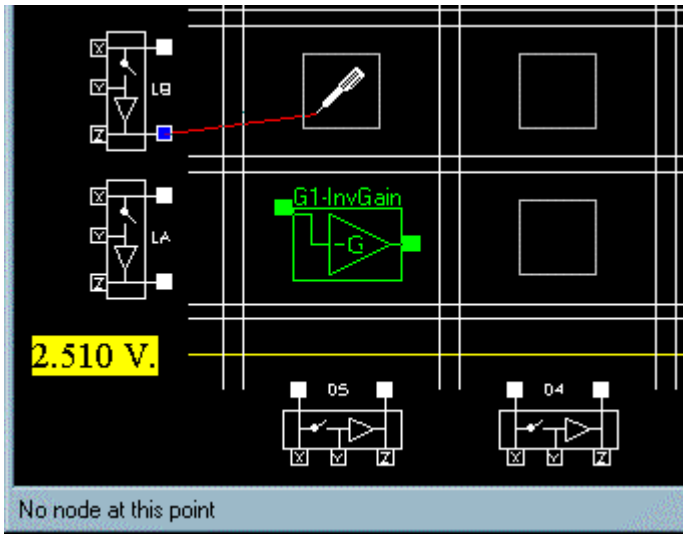
There is a control which enable you to select which of the 4 internal clocks will drive the IPmodule. There is also the "Display IPmodule Documentation" button which pops up a quick help window which full describes the features of the selected IPmodule.

Hit Cancel and enter the Wire mode of AnadyneDesigner.

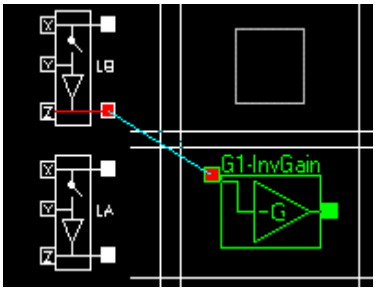


Connect the IPmodules and IO Cells with Wires

Clicking over the  symbol or type a w on the keyboard to enter the wire mode. The cursor image will change to a drawing pen symbol. As the name suggests, this wire mode is used to wire up connections within the array, and is also used for power up the IO cell op-amp and closing its switch. More on those uses later, for now, lets wire this circuit up.

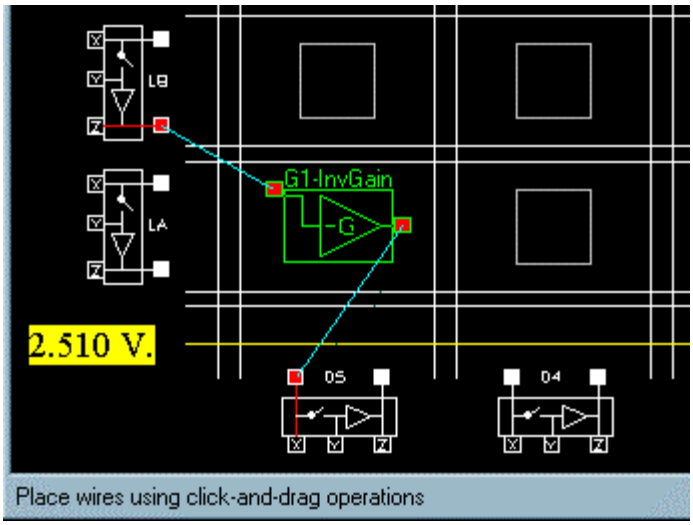


Place the tip of the cursor over the "output" (lower) terminal of the IO Cell labeled "LB". Press the left mouse button down and hold it down. The interior of the white output terminal should change to blue if the cursor was placed close enough for AnadyneDesigner to snap to the terminal. As you drag the mouse, you will see a "rubber-band" line stretch from the terminal to the tip of the cursor where ever you move it within the design window. As you move the cursor over the vertical and horizontal global wires and other terminals on the screen, note the highlighting of global wires and terminals that occurs. Also note the messages that appear in the lower left corner of the screen, i.e., in the "status bar".



Circuit connectivity in the FPAA array is accomplished by setting switches within the chip. Some nodes cannot be directly connected in the design window because no switch exists within the array that could directly connect them. The messages in the status bar tell you continuously whether you can or cannot connect to the site the cursor is over. These messages also provide a brief explanation as to why you cannot connect to some particular site. Place the cursor directly over the solid green square (input contact) on the left side of the gain stage. The interior of the green square will turn blue.

Release the mouse button. A blue wire will appear in place of the red rubber band line and the interiors of both contacts will turn red indicating that a connection has been made.



Using the same, click-drag-release method, please connect the output terminal of the right hand side of the gain stage to the input terminal of the IO Cell labeled “D5” as shown.

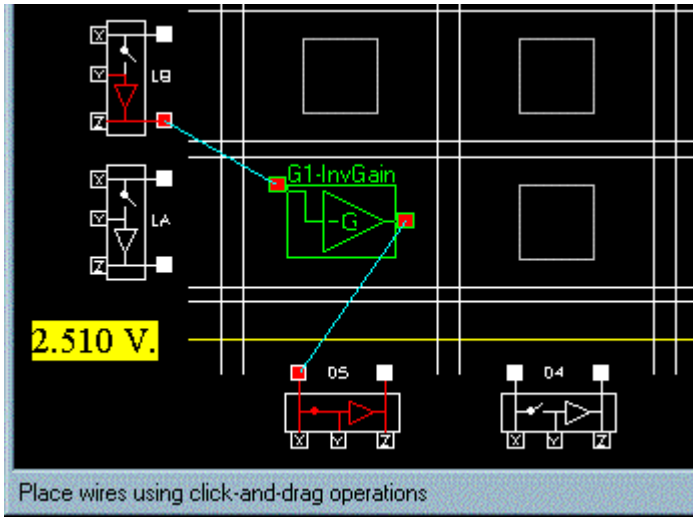
In this simple example, we have used only local routing resources. The pairs of vertical and horizontal lines represent global routing resources. These are explained more completely in the body of the manual.

Your first design is nearly complete, all that's left to do is power up the IO Cells. and configure the device.

Power up the IO Cells

Now turn on the appropriate op-amps and switches by placing the “pen” cursor directly over them and clicking the left mouse button. As the switches are close and the op-amps power up, the elements will turn red.

That completes construction of the circuit. To see this circuit in operation, we will need to download the configuration data to the FPAA. We will also need to input a signal such as a sine wave to the “Y” pin of the “LB” IO Cell and attach an oscilloscope probe to the “Z” pin of the “D5” IO Cell.



Download the Configuration Data

Using the Ctrl-w shortcut, download the configuration data to the array and look at the oscilloscope screen. The default gain of the inverting op-amp is “1”.

You are now free to change whatever you wish in the design. For example, right mouse click on the center of the green gain stage symbol to bring up the Set IPmodule Parameters dialog box to alter the value of the gain.

Click OK to store the new gain value then again download the configuration data, and look at the oscilloscope to see the effect of the new gain value.

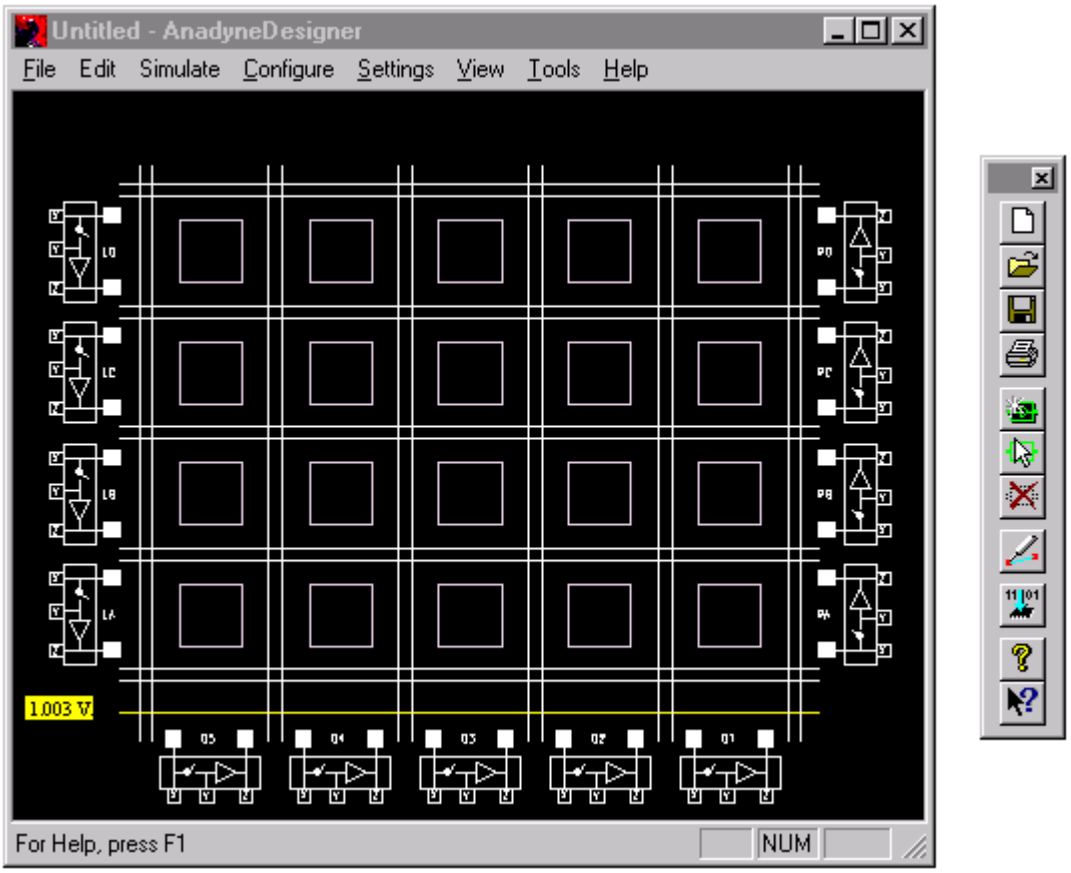
Insanely simple. Incredibly powerful.

AnadyneDesigner User Reference

The Main User Interface

AnadyneDesigner presents the user with a comfortable and intuitive interface. The entire program window is sizable to any practical size you feel most comfortable working in. Focus on ease of use continues with a complete, but not overburdened set of familiar and well organized pull down menus; each containing just the options you would expect. A few thoughtfully selected iconic push-button shortcuts are also provided in a tear away palette that can be floated anywhere on screen.

The window itself contains a functional “map” of the FPAA die. This depiction of the die shows the 13 available IO Cells, the 4 by 5 array of Configurable Analog Block (CAB) locations and the 10 by 12 grid of global routing channels. Local interconnects are not shown until used. As IPmodules are dropped onto the map, as wiring connections are made and as I/O cells are routed to, you complete a correct-by-construction graphical depiction of exactly how the FPAA will be configured at boot time.

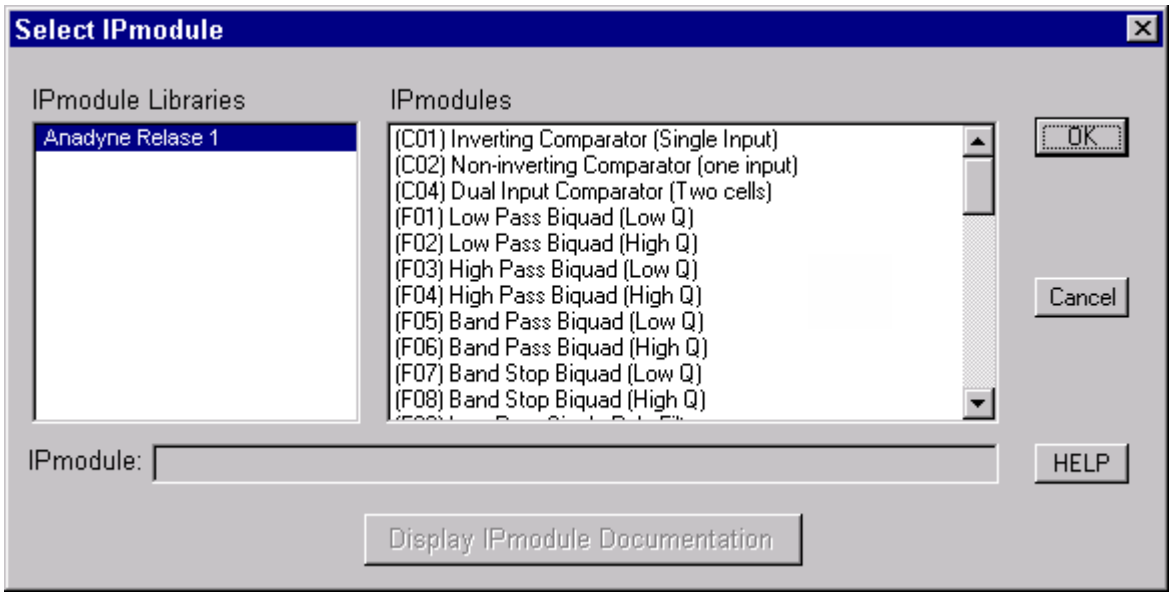


Notice in this particular screen shot, that the shortcut button palette has been undocked from its default position just under the pull down menus and floated to the right of the main window. It only takes a simple click and drag to tear it away and float it wherever on the display you like. You can also dock it to any of the other three sides of the main window just as easily.

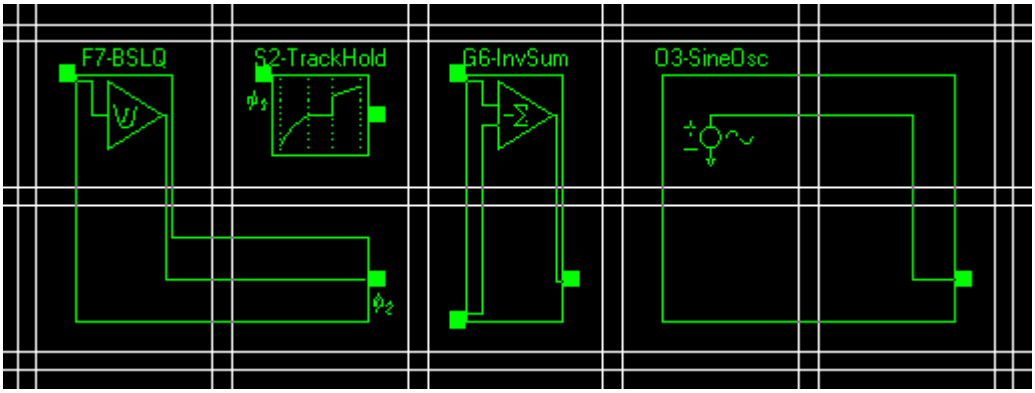
The programmable voltage reference displays its currently programmed value in the lower left of the design window.

Selecting and Placing an IPmodule

Selecting and placing an IPmodule begins with a pull down menu selection of Edit → Select IPmodule. The Select IPmodule window will pop up next.



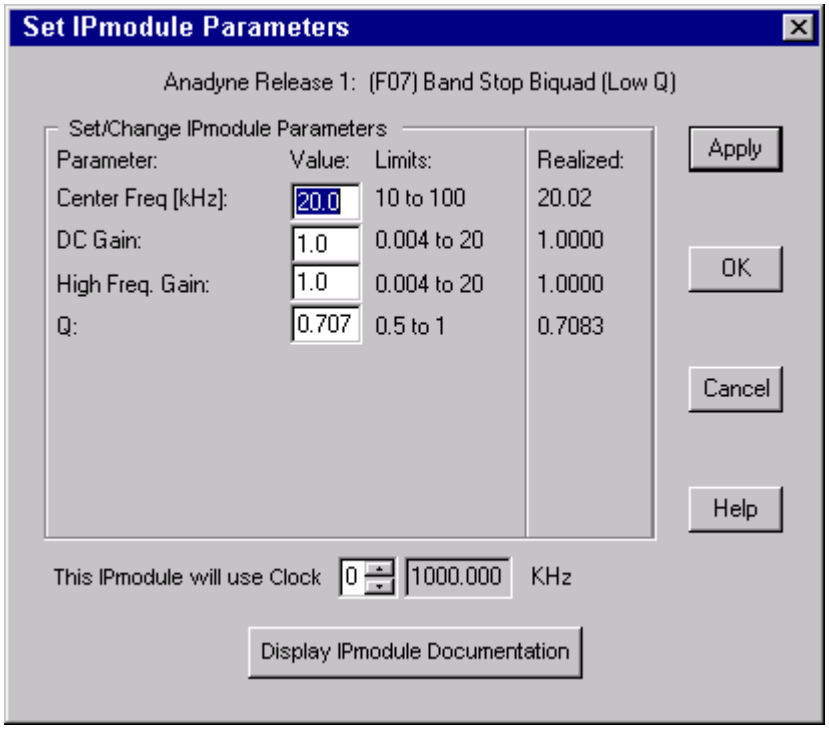
The available elements of the default selected IPmodule library (.lib file) are presented in the scrollable right half of the pop-up. As you first begin using AnadyneDesigner, you may want an IPmodule Manual close at hand, though extensive on-line context sensitive help is always available. Once an IPmodule is selected with a left mouse click and a tap of the OK button, the pop-up dismisses itself and a ghost image of the IPmodule is attached only to your mouse cursor. Another left click of the mouse, and it will snap down to the closest available empty configurable analog block (CAB) element (or collection of empty elements of the appropriate shape).



Most of the IPmodules consume only a single CAB, but some of the more complex circuits that have been characterized and placed into a library may consume two or more. In the above screen shot, you can see an odd collection of IPmodules that consume 1,2, 3 and 4 CAB locations.

Setting IPmodule Parameters

A right mouse click over any placed IPmodule will bring up its Set IPmodule Parameters pop-up.



It is in this window that all the pertinent parameters of this particular placement the IPmodule are established. AnadyneDesigner defaults with a reasonable set of default parameters but you are free to change any number field with a white background to any in-range value that suites your needs. As you do so, AnadyneDesigner immediately computes and displays “realized” parameters performance estimates.

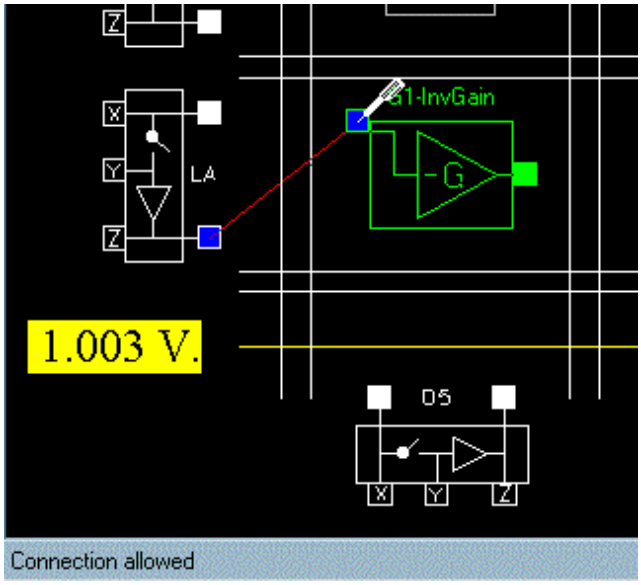
Because the feedback elements of a CAB are restricted to a limited set of discrete values, the realized numbers may be slightly off from your input numbers. This quantization error is demonstrated in the sample above. A center frequency of 20.0 kHz was desired, but the closest frequency AnadyneDesigner and the FPAA could match to was 20,020 Hertz. Likewise the realized filter’s Q is off by a few tenths of a percent.

Please note – Changing the clock frequencies within the array after an IPmodule has been placed and parameterized will of course affect its response. (More on clocks later.) If it is necessary for you to change a clock setting after your IPmodules are placed and parameterized, then you will want to go back and right click on all the IPmodules assigned to that clock and make the appropriate corrections.

Additional details on each of an IPmodule's parameters and performance values can be found in the IPmodule Manual.

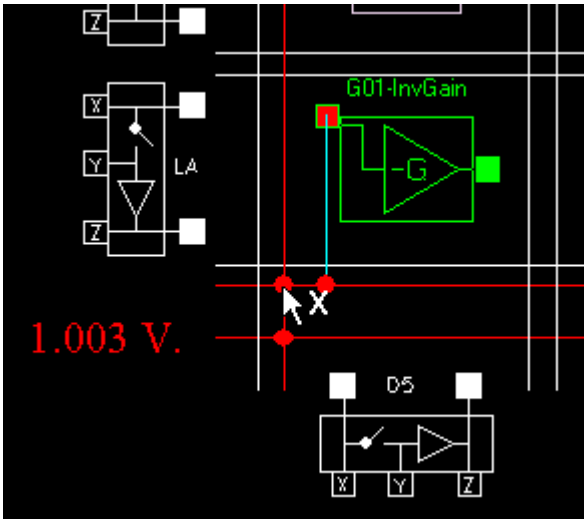
Using Local and Global Routing

The most expedient way to gain understanding of the routing resources available on an FPAA is to use just simply use this software and try a few things out on your own. Failing that, the following screen shots and paragraphs summarize the connections available within an AN10E40.



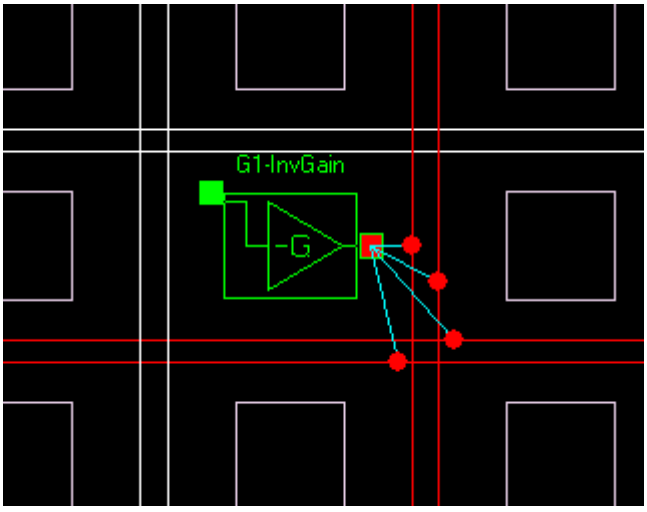
The Wire mode, turns the cursor into a little soldering iron (an item that you will soon no longer be using). Select the first node with a left click and hold of the mouse. The node (contact or global wire) will turn blue if the wiring cursor tip was close enough for the software to snap to a valid connection point. As you drag the cursor a rubber band line will appear from the selected node to the tip of the wiring cursor. As you move the mouse you will receive immediate feedback that lets you know if the mouse pointer is over a valid connection site. The contact or global wire will turn blue if it is valid and there will be a message in the lower left corner of the window. That message is updated continuously in real-time as you move the mouse pointer so you have feedback regarding whether a connection is possible.

With a left mouse click, the Wire mode is also used to power up the switch and the op-amp sections of an IO cell.



The Delete mode provides an effective tool for deleting unwanted connections or IPmodules. A quick left click over the wire, IPmodule or global route “solder dot”, deletes these items.

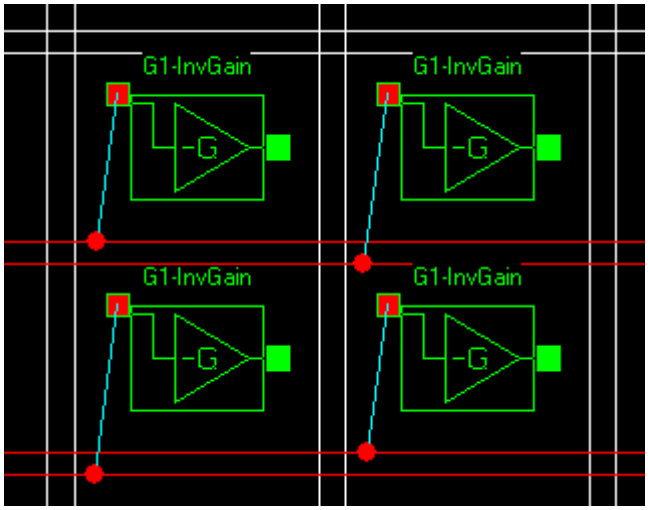
In an identical manner to the Wire mode, a left click over either the switch or op-amp halves of the IO cell toggles power on these components.



Global routing resources allow you to move signals to disparate locations on the die. There are a total of 10 horizontal global routes and 12 vertical global routes within the array. A IPmodule’s output can be connected to any of the two adjacent right or two adjacent down global routes.

The output drive of a IPmodule is limited, but is designed to handle the capacitance of the load presented by a single receiving IPmodule plus two global routes or plus a single local route.

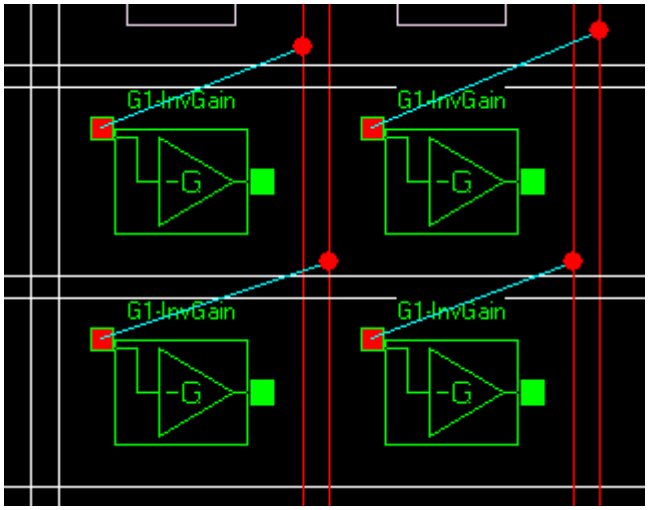
AnadyneDesigner does not prevent you from overloading a IPmodule output.



Inputs on the other hand are limited to be driven by a single source. In other words, you are not allowed to short outputs together.

In the case of global routing, inputs may be driven from one of the two adjacent bottom global routes. Just which of the two global routes alternates with row and column position within the array.

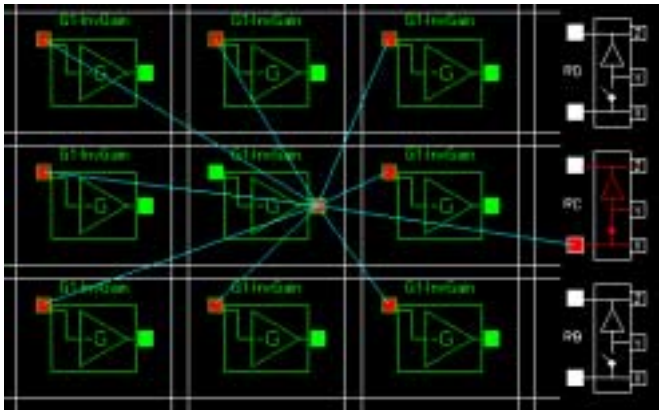
Here a quartet of IPmodules have been wired up to the only possible global routes below the cell.



Global routing from the right to an input has a similar connection characteristic as routing from below.

When routing from global channels form the right of the IPModule, inputs may be driven from one of the two adjacent right global routes. Just which of the two global routes alternates with row and column position within the array.

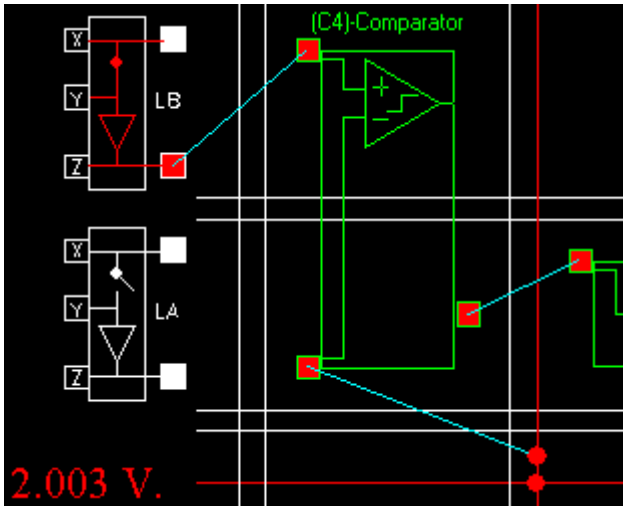
Here another quartet of IPmodules have been wired up to the only possible global routes to the right of the cell.



Local routing resources are only shown (as fly lines a.k.a. rubber band lines) in the AnadyneDesigner screen once they are used. An IPmodule output may be connected to an input in any of its 8 adjacent neighbors, and additionally to the IPmodule or I/O Cell in the same row and to the right two locations.

In the screen shot shown here, 'the same row and to the right two locations' happens to be an IO Cell.

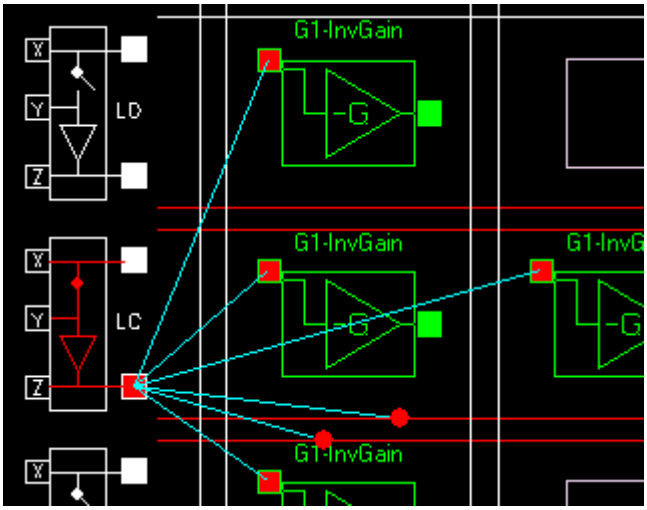
Again, AnadyneDesigner does not prevent you from overloading a IPmodule output. It is doubtful that the sample shown here would reliably operate within spec.



Connections to the programmable on chip voltage reference can only be made via global routing resources.

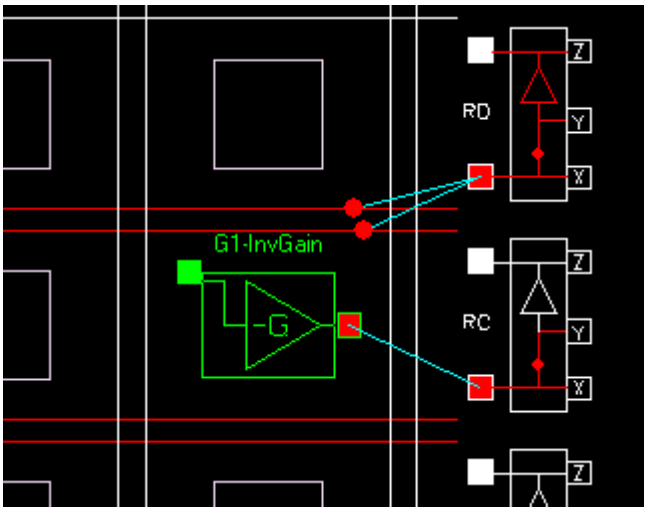
In this screen shot of the lower left portion of the design window, a two input comparator IPmodule has been placed. The lows side input is connected to an adjacent right global route, which in turn was shorted to the programmable voltage reference route.

The high side input of the comparator is connected to a buffered external input signal.



Local connections from and IO cell's output port are constrained in a manner consistent with IPmodule cell outputs. In the case of an IO cell however, there are not 8 adjacent neighbors. For IO cells along the left edge of the die, there are up 3 immediately adjacent neighbors and a neighbor on the same row and to the right two locations. For bottom edge IO cells, local connections can be made to the adjacent 3 CABs above. For the right side IOs, local connections can be made to the 3 CABs just to the left.

Connections to Global routing from left or right edge IO cell outputs are available on the two channels just below the IO cell. For the bottom edge IO cell outputs, global routing is available on the channels immediately to the right.



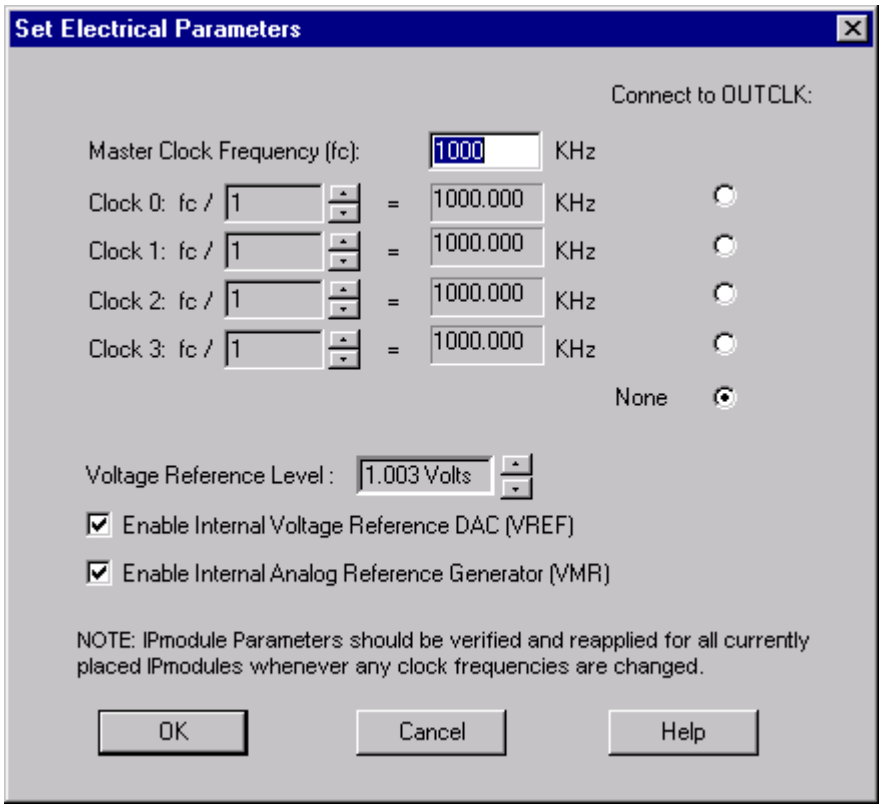
Connections to an IO cell's input port are available on the same global resources described above.

Local connections to an IO cell input again follow the same constraints as the conventional IPmodule input connections.

In this particular example, the topmost IO cell is completely powered up (all red) and its Z output is ready for external connection. The lower IO cell will only have an unbuffered signal available on its X or Y pads.

Generally, analog circuit processing functions are connected in a serial fashion. The routing architecture of Anadyne's FPAA take this into account and provide you with resources you need to implement your designs.

Setting Clocks, VREF Voltage and VMR



A right click over the Voltage Reference (VREF) indicator in the lower left hand portion of the design window brings up the Set Electrical Parameters pop-up box.

The AN10E40 has 4 programmable internal clocks that can be used to drive the placed IPmodules. The clocks Clock 0 through 3 can be divided down from the master from 2 to 62 times (in even steps) or not at all. The vertical set of selection buttons to the right select which if any of these clocks shall be presented on the OUTCLK pin.

The topmost entry box labeled Master Clock Frequency is where you tell AnadyneDesigner what clock frequency you will be applying to the array. AnadyneDesigner uses this clock frequency for all performance calculations when setting an IPmodule's parameters. If at any time in the design cycle you decide to change this master frequency (or the divide by ratio of any of the 4 internal clocks) then you should verify and reapply parameters for all placed IPmodules.

Up-Down arrow selectors for each of the 4 programmable clocks are used to set their frequency divisor. The resultant frequency is conveniently calculated and displayed just to the right.

There is an on board programmable Voltage Reference Level available for your use. It has a range just a little over –2.2V to + 2.2V. You have the option to disable the VREF if your application requires the most optimal power conservation.

The Internal Analog Reference Generator uses a precision source to generate 2.5V. This Voltage Mid-Rail (VMR) is the reference voltage for all analog processing within the array. If you elect to instead generate your own VMR external to the device and drive it in, you may do so, but of course it is recommended that you disable VMR within this pop-up during the design process.

The "File" Pull-Down Menu

New Device

Your selection of any of the available FPAAs from Anadyne is made using this menu selection.

New Design (Ctrl-n)

When you are ready to design a new circuit use this menu selection or the Ctrl-n keystroke short cut. If the design currently resident has been modified since its last save, then you will be given the opportunity to save it before New Design clears the design window.

Open (Ctrl-o)

The standard file selection dialog box will open on execution of this menu item. In the context of AnadyneDesigner, you will be browsing for a .ckt file containing a previously saved design. If the contents of the current design window have been modified since the last save, AnadyneDesigner will give you the opportunity to save prior to overwriting with the contents of the file to be opened.

Save (Ctrl-s)

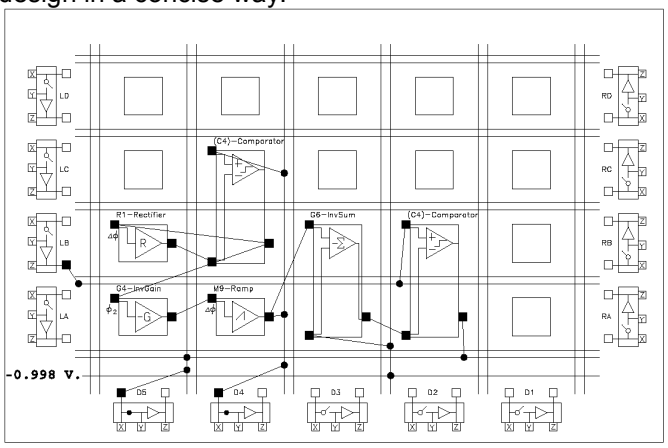
Selection of this menu item (or using its Ctrl-s keystroke shortcut) will save the current design state to its associated .ckt file. If there design window happens to be currently Untitled, then Ctrl-s will behave the same as the Save As menu item.

Save As

The Save As menu item allows you to save the current design as a new .ckt file. A typical application would be to open some reference design, make some modifications and Save As some new name, without affecting the contents of the reference design's .ckt file first opened.

Print (Ctrl-p)

The print command brings up a standard Print dialog box. Printing an open design is a great way to document your design in a concise way.



The first page of the printed report is a graphical representation of the design screen. All of the design's connections are shown along with the VREF setting.

The design file name is presented for easy design retrieval. This view is handy for the PCB designer. It clearly shows the input and output pads.

pulse—width modulator.ckt

```
Cell (B,5) - Anadyne Release 1: (R1) Full wave RECTIFIER (with low-pass filter)
     Clock Frequency:         1000.000 KHz
     Corner Freq [kHz]:       Desired:  159   Realized:   158.80
     Pass-Band Gain:          Desired:  0.8   Realized:   0.800
     Temperature [C]:         Desired:  27    Realized:   27.0

Cell (B,3) - Anadyne Release 1: (G6) Inverting SUM AMPLIFIER
     Clock Frequency:         1000.000 KHz
     Gain1 (top input):       Desired:  1.0   Realized:   1.000
     Gain2 (bottom inp.):     Desired:  1.0   Realized:   1.000
     Temperature [C]:         Desired:  27    Realized:   27.0

Cell (A,4) - Anadyne Release 1: (M9) RAMP
     Clock Frequency:         1000.000 KHz
     ClkCyc/1V (for 1V Vin): Desired:  255   Realized:   255.000
     Const Vin [V]:           Desired:  1.0   Realized:   1.000
     Temperature [C]:         Desired:  27    Realized:   27.0

Cell (B,2) - Anadyne Release 1: (C4) 2-input COMPARATOR (two cells)
     Clock Frequency:         1000.000 KHz
     Temperature [C]:         Desired:  27    Realized:   27.0

Cell (A,5) - Anadyne Release 1: (G4) Inverting GAIN STAGE (comp. in one phase)
     Clock Frequency: 1000.000 KHz
     Gain:                    Desired:  1.0   Realized:   1.000
     Temperature [C]:         Desired:  27    Realized:   27.0

Cell (C,4) - Anadyne Release 1: (C4) 2-input COMPARATOR (two cells)
     Clock Frequency:         1000.000 KHz
     Temperature [C]:         Desired:  27    Realized:   27.0
```

The following pages of the printed report document all IPmodule parameter settings as well as the calculated 'realized' values.

If in the course of design, you elect to change one or more clock frequencies, then these sheets are a handy reference to guide you back to those affected IPmodule cells.

These report pages also serve as a handy design review report, allowing others the ability to review your design with needing to be in front of a tube running AnadyneDesigner.

Print Preview

Nothing new to a computer user here. The normal Print Preview functions allow you to view one or two pages at a time of the report to be printed out. There are tool bar buttons available for zooming in and out, flipping through the pages, printing and dismissing the window.

Print Setup

This menu item brings up a standard print dialog box. From this pop-up, you can select paper size and orientation as well as a printer. You may also adjust print options specific to the selected printer.

Most Recently Used - MRU File List

The second to last section of the File pull-down menu is a short list of the Most Recently Used design files, sometimes referred to as an MRU list. From this convenient location, you can quickly left click over the desired design and AnadyneDesigner will re-load that design back in.

Exit

A left click over the Exit item will immediately close down AnadyneDesigner. If your design was modified since the most recent save, then AnadyneDesigner will give you the opportunity to save your changes away before dismissing itself.

The ”Edit” Pull-Down Menu

This is where the work gets down. Within the first few minutes of getting acquainted with AnadyneDesigner, most users will abandon this pull-down menu and its contents in favor of the more convenient short cut keys.

Undo (Ctrl-z)

The undo feature keeps track of all the drawing steps you’ve taken since the design last opened for editing. You can go back in time undoing the edits one at time.

Redo (Ctrl-Alt-z)

Did you get a little over exuberant with your Ctrl-z’s and wipe out a bit too much of your design? No problem. In the same way Undo keeps a record of items added to your design, Redo keeps track of things taken away, and allows you to move back forward in design steps, replacing accidentally “undone” items.

Select IPmodule (m)

This menu item or its M keystroke shortcut causes the Select IPmodule pop-up dialog box to appear. (Please see above, Selecting and Placing an IPmodule.) Scroll to and left click to select the desired IPmodule to be placed into your design. If you have questions about the IPmodule, on line help for the selected IPmodule is available with a second left click over the Display IPmodule Documentation button. A left click on the OK button returns you to the design window, with a ghosted image of the selected IPmodule attached to your cursor. Drop the IPmodule into any available CAB location(s). A ghosted version of the IPmodule remains attached for quick additional placements. The ghosted image of the IPmodule will disappear if you change edit modes or hit the Esc key.

Enter Wire Mode (w)

This menu item or its w keystroke shortcut changes the cursor to a small soldering iron. This icon is used to make local and global connections as well as power up the switch and op-amp halves of the IO cells.

Enter Buffers/Switch Set Mode (b)

This allows you to left-click on the buffer op-amps and switches in the IO Cells around the periphery of the chip and toggle them on or off. It also allows all of the Wire mode operations.

In fact, this mode is identical to wire mode except for the instructions that appear in the lower left corner of the display. This command was added primarily for user clarification regarding how to toggle the buffer op-amps and switches. Anadyne wants you to recapture the fun of design, without having to slog through yet another manual.

Enter Shift IPmodule Mode (s)

The Shift IPmodule Mode is the default mode of a design session. Left click and drag over a placed IPmodule in this mode and you can shift the IPmodule to another location on the array. (Any connections made to an IPmodule will be deleted as it is shifted to its new location.) This is a very convenient method of shuffling IPmodules around in a complex design to optimize signal flow.

Enter Delete Mode (d)

Use this menu item or its d shortcut to delete placed IPmodules or connections in a design. Once in the Delete Mode, the cursor changes to small skull. Just left click over the unwanted IPmodule or connection element and it disappears from your design. This deletion cursor also conveniently serves as a third editing mode that allows to you toggle the power on the switch and op-amp halves of the IO cells.

The ”Simulate” Pull-Down Menu

A simulation function is being worked on by the engineers at Anadyne. We thought it better to bring the design system to you now, then wait for complete development of a non-critical feature. The next major release of AnadyneDesigner will have a full featured simulation tool which will allow stimulate your design using virtual signal generators and monitor internal signals with virtual oscilloscopes. Pretty cool stuff.

The ”Configure” Pull-Down Menu

Detailed descriptions of the serial port data stream and configuration file formats are addressed later in this manual.

Write Configuration Data to a Serial Port (Ctrl-w)

This writes the configuration data, for the circuit being displayed, to your PC’s serial port. There are a variety of appliances that use this data port to move data to the FPAA. Many of the Anadyne evaluation products have the appropriate RS-232 circuitry on board for this function, obviating the need for programming Serial Boot PROMs or writing microcontroller hosting programs.

Write Configuration Data to a “.AHF” File

This writes the configuration data, for the circuit being displayed, to a file. The ".ahf" file contains the ASCII codes for the hexadecimal byte-stream that represents your circuit. The root filename will be the name you assigned to your circuit file. If the file you are working with is "circuit1.ckt" then the file that will be written will be named "circuit1.ahf". The file will be written into the same directory that your circuit file is in. The path name for this file will be displayed in the lower left corner of the window immediately after the file has been written in case there is any question regarding where the file was written.

The file may be used to program a parallel EPROM chip or used as a data file for microcontroller hosted FPAA designs.

Note that some of the older versions of EPROM programmer software packages are unable to handle file names greater than eight characters so you might wish to choose your circuit name with this in mind.

Write Configuration Data to a “Reversed .AHF” File

This menu item does basically the same as the item just described above. The only differences are that the bits of each byte are reversed to comply with the convention of programming serial PROM chips, and the root file name is appended with a “-r” to reflect this data reversal.

Write Configuration Data to a “Motorola S-Record Format” File

This writes the configuration data, for the circuit being displayed, to a file. The ".ms2" file contains the ASCII codes for the hexadecimal byte-stream that represents your circuit. The root filename will be the name you assigned to your circuit file. If the file you are working with is "circuit1.ckt" then the file that will be written will be named "circuit1.ms2". The file will be written into the same directory that your circuit file is in. The path name for this file will be displayed in the lower left corner of the window immediately after the file has been written in case there is any question regarding where the file was written.

The file may be used to program a parallel EPROM chip or used as a data file for microcontroller hosted FPAA designs.

Note that some of the older versions of EPROM programmer software packages are unable to handle file names greater than eight characters so you might wish to choose your circuit name with this in mind.

Write Configuration Data to a "Reversed Motorola S-Record Format" File

Here again, this menu item does basically the same as the item just described above. The only differences are that the bits of each byte are reversed to comply with the convention of programming serial PROM chips, and the root file name is appended with a "-r" to reflect this data reversal.

The "Settings" Pull-Down Menu

Chip Settings

This menu item brings up the same Set Electrical Parameters pop-up dialog box that you get by right clicking over the VREF indicator in the design window. Please see the section "Setting Clocks, VREF Voltage and VMR" for the complete description of all of this dialog's items.

Serial Port

Selecting this menu item brings forward the Serial Port for Chip Download Operations dialog box. It is within this dialog box that you inform AnadyneDesigner about your particular serial port connections.

Preferences

All AnadyneDesigner user preference options are set in this dialog box. As of release 1.0, the only option available in the sound effects on/off control.

The "View" Pull-Down Menu

Like the Edit pull-down menu, users even modestly acquainted with AnadyneDesigner will usually quickly abandon this menu in favor the intuitive short cuts.

Toolbar

AnadyneDesigner's tool bar can be torn away and floated anywhere on our PC's screen. If that doesn't solve your clutter problems, then selecting this menu item will toggle the check mark next to "Toolbar", hiding and unhiding the toolbar from the PC screen.

Status Bar

In a similar fashion to the Toolbar entry, the Status bar menu item will toggle the visibility of the status bar along the bottom of the design window.

Zoom In (I)

The entire design window is sizable to suite your personal preferences. AnadyneDesigner launches with a design window size and placement comfortable for most users on most computer screens. If you elect to resize the design window (dragging the familiar double headed diagonal arrow cursor) you may wish to zoom in or out on your design.

The Zoom In menu item or its i keystroke shortcut quickly zooms in on your design without resizing the window. Anytime you are zoomed in, horizontal and vertical scroll bars show up to allow easy panning.

Zoom Out (o)

Selecting the Zoom Out menu item or its o keystroke shortcut zooms the design back out. Repeated o's will continue to zoom the design out until the complete array diagram fills the design window.

Zoom Fit (f)

A quick press of the f key resets the current zoom settings to default and brings the entire array back into full view.

Refresh (r)

The graphic windowing systems within operating systems are imperfect creations, even for as long as they have been around. Through no fault of its own, design features within the AnadyneDesigner window may mysteriously disappear on a zoom, pan or related windowing operation. A quick swipe of the r shortcut key refreshes the graphics in the design window and quickly dispenses with the rare annoyance.

The ”Tools” Pull-Down Menu

There are typically no contents in the Tools pull-down menu. As we and our customers continue to innovate, we sometimes build experimental versions of AnadyneDesigner and this is where access to custom features is usually provided. Don’t feel left out! We welcome your comments and suggestions on our unique programmable analog array technology.

The ”Help” Pull-Down Menu

Help Topics

Though AnadyneDesigner and the Anadyne FPAAs are designed to be intuitive, with little need of a manual for successful use, we want to be sure that you have all the answers to keep you moving ever forward. The on line help is extensive.

About AnadyneDesigner

Selecting this menu item brings up a small pop-up that gives you information about the build of AnadyneDesigner that you are currently using.

Configuration File Formats

The Serial Port Data Stream

Selecting the Configure -> Write Configuration Data to Serial Port pull down menu item (or using the Ctrl-w shortcut), causes AnadyneDesigner to assert RTS on the selected serial port (see the Settings menu description). On receipt of the RS-232 CTS signal, AnadyneDesigner will commence to move configuration data which represents the currently loaded design out to the serial port at 9600 baud. The complete transmission is bracketed with STX and ETX characters. RTS/CTS handshaking is used to control the flow of data. There are no parity bits sent. There are no stop bits.

Motorola S-Record Format

A second industry standard format for transferring programming information between tools is the Motorola S-Record format. The file is easy to understand once you have been introduced to it. The first and last couple of lines of a S-Record format file for an AN10E40 are shown below.

```
S224000000138502B70000000000000000000000000000000000000000000000000000000000000026
S2240000200000000000000000000000000000000000000000000000000000000000000000000000BB
. . .
S20E000360080000080000080000 1462
S9030000FC
```

A field by field dissection of the first and last S-Records within an AN10E40 configuration file is given below:

```
S224000000138502B70000000000000000000000000000000000000000000000000000000000000026
```

S2 → tells downstream tools that this record's address field is 24 bits in length.

24 → tells downstream tools that 36 (hex 24) bytes follow.

000000 → tells downstream tools that the starting address for this data is 0x000000.

138502B7 → Not part of the S-Record spec, but this is first of the device specific data.

138502B7 → For Anadyne FPAAs, these 8 bytes represent a unique

138502B7 → device type identifier.

26

This is the end of S-Record check byte ← 26

```
S9030000FC
```

S9 → tells downstream tools that this is the termination record for the file.

03 → byte count for remainder of record

0000 → dummy data

FC→ checkbyte

ASCII Hex File Format

ASCII Hex File Format is nothing more than raw configuration data bytes represented as ASCII Hex pairs, with a CR-LF pair suffixing each byte.

```
13
85
02
B7
00
00
00
. . .
```

Here again, you can see that the first 4 bytes of a configuration file contain the 32 bit device type code for an AN10E40.

Why Reversed?

Below are the first lines of two S-Record configuration files for the same design. The first line is from a "normal" S-Record file, the second from a reversed. The device configuration data is bolded.

```
S224000000138502B70000000000000000000000E00100000000000000000000000E0010064
S224000000C8A140ED0000000000000000000000078000000000000000000000000078000AC
```

The binary representations of the first data bytes "13" and "C8" are:

13 = 00010011
C8 = 11001000

You can see that the bits within each data byte of the second (reversed) file are ordered opposite the first. The reason this is done is that data comes out of a serial EPROM in the opposite order in which it was programmed in. This quirky behavior of serial EPROMs has been around since their market introduction and has simply stuck.

If you intend to use serial EPROMs for booting an Anadyne FPAA, and your PROM programmer does not take this "first in last out" behavior into account (most do not), then you will likely want to use the "reversed" version of either of .ahf or .ms2 configuration file formats.

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