
# Internship position description

## Modeling and design of hybrid CMOS/magnetic circuits based on newly discovered spintronics phenomena

Keywords
Spin electronics ; compact models ; CADENCE ; circuits design ; spin orbit

Summary
Spin electronics is a merging of microelectronics and magnetism which aims at taking advantage of the best of the two worlds. Magnetism is very appropriate for memory functions since it allows encoding information in a nonvolatile way via the direction of magnetization of magnetic nanostructures. Magnetic memories called MRAM (Magnetic Random Access Memories) are about to be launched in volume production at several major microelectronics companies. For readout, these memories use the magnetoresistance of magnetic tunnel junctions while the writing is performed by using the magnetic torque that a spin-polarized current exerts on the magnetization of a magnetic nanostructure (spin transfer torque). But spinelectronics keeps on progressing and new phenomena have been discovered since then on which our laboratory is actively working. These new phenomena rely on spin-orbit interactions and on the control of the magnetic properties of magnetic nanostructures by electric field rather than magnetic field or spin transfer torque. They enable the conception of memories and non-volatile logic circuits working at multiGHz frequency and exhibiting extremely low power consumption. The purpose of this internship will first consist in developing compact models of devices based on these new phenomena, for electrical simulation using the standard design suites of microelectronics. The models will be confronted to experimental results obtained in our laboratory and others available from literature. Once validated simple circuits will be designed based on these phenomena such as non-volatile standard cells for digital design, small memory matrix or radiofrequency spintronics oscillators, for which these new devices seem particularly promising. These circuits' performances will be benchmarked with those of equivalent circuits.

### Full description of the subject

The internship will be made at Spintec laboratory, jointly operated by CEA, CNRS (French research organisms) and the University of Grenoble. Spintec aims at making the bridge between upstream research in magnetism and microelectronics applications. It covers activities from fundamental research (theory, simulation, materials, processing…) to the design of hybrid CMOS/magnetic logic circuits. The candidate will join the "Spintronics IC design staff" of spintec, in charge of the design, fabrication and test of spintronic circuits. Spintronics consists in using magnetic devices in addition to standard microelectronics devices to push forward the physical barriers that limit integrated circuits scaling. These devices are the basic blocs of an emerging memory technology, called MRAM for Magnetic Random Access Memory. These memories are part of resistive non-volatile memories. They combine several advantages for logic circuits, that are not gathered by any other memory technology: intrinsically non-volatile, the have an operation speed close to the one of SRAM, a density close to the one of DRAM and a quasi-infinite endurance.

A lot of academic studies have shown the advantages in terms of performance, power consumption and new functionalities that can be expected in computations systems for various applications. The biggest actors of microelectronics are investigating this technology in its standard version, with Spin Transfer Torque (STT) writing scheme. However, while STT becomes more and more mature and close to industrialization, new generations are studied in laboratories and in particular at Spintec, like electric field assisted writing scheme of spin/charge current interconversion by spin orbit effect. These new technologies promise still better performance but are actually at the stage of theoretical studies, from fundamental understanding to materials developments.

The aim of the internship is a preliminary evaluation of the advantages that can be expected from memory and logic circuits using these new concepts. It will be necessary to develop compact models of the devices and integrate them in the standard tools of microelectronics for electrical simulations. These models will then be used to design elementary circuits which will allow in the long term an evaluation of the gains for more complex circuits. The internship could address the following tasks :

- Compact model development for electrical simulations using the design suite CADENCE.
- Validation of these models by comparison with experimental results obtained in the lab or from the literature.
- The design of elementary circuits like non-volatile logic gates (NOR, NAND …), small memory blocks or spintronics RF oscillators.
- Evaluation of the performance of these circuits compared to the equivalent state of the art.
- Writing of scientific articles an internship report.

## Requested skills

The candidate should have a master degree or equivalent, from university or engineer school. His skills should cover microelectronics full-custom/circuit level design preferably using Cadence. VerlilogA language programing notions would be an asset. The level of English should allow the candidate to read and write scientific articles, as well as attending technical discussions which could be made in English. An attraction for research and multidisciplinary are very important for this internship.

## Possibility to follow with a PhD Yes

## Contact

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