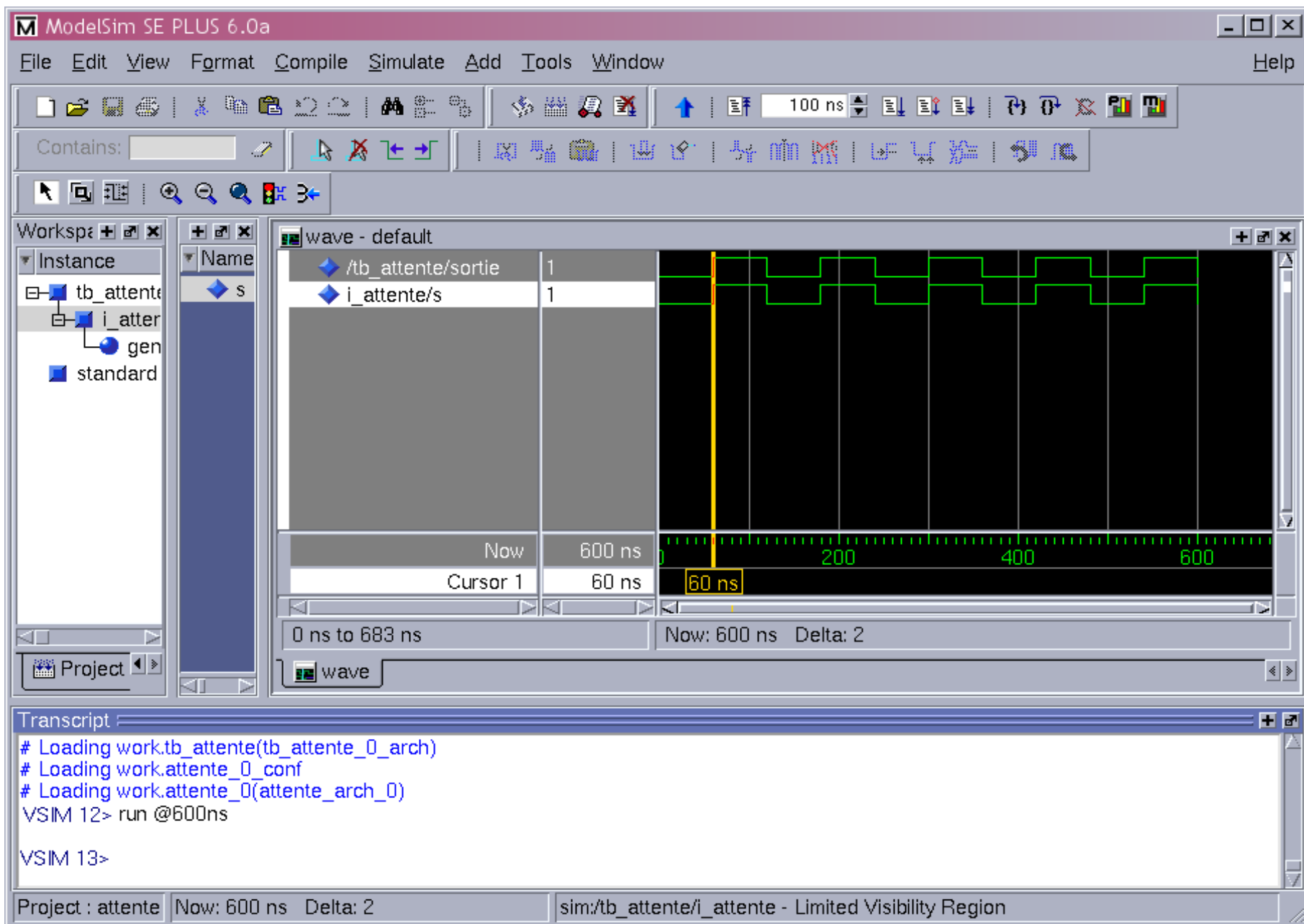


Variations autour du Wait...

**D'un code simulable vers un code générique
synthétisable...**

TB0 / attente 0



The screenshot shows the ModelSim SE PLUS 6.0a interface. The main window displays a waveform for two signals: `/tb_attente/sortie` and `i_attente/s`. The time scale is set to 100 ns. A cursor is positioned at 60 ns, and the time range is from 0 ns to 683 ns. The waveform shows a series of pulses with a period of 60 ns. The status bar at the bottom indicates the current time is 600 ns with a delta of 2 ns.

Workspace:

- Instance: `tb_attente`
 - `i_attente`
 - `gen`
 - `standard`

Waveform:

Name	Value
<code>/tb_attente/sortie</code>	1
<code>i_attente/s</code>	1

Transcript:

```
# Loading work.tb_attente(tb_attente_0_arch)
# Loading work.attente_0_conf
# Loading work.attente_0(attente_arch_0)
VSIM 12> run @600ns
VSIM 13>
```

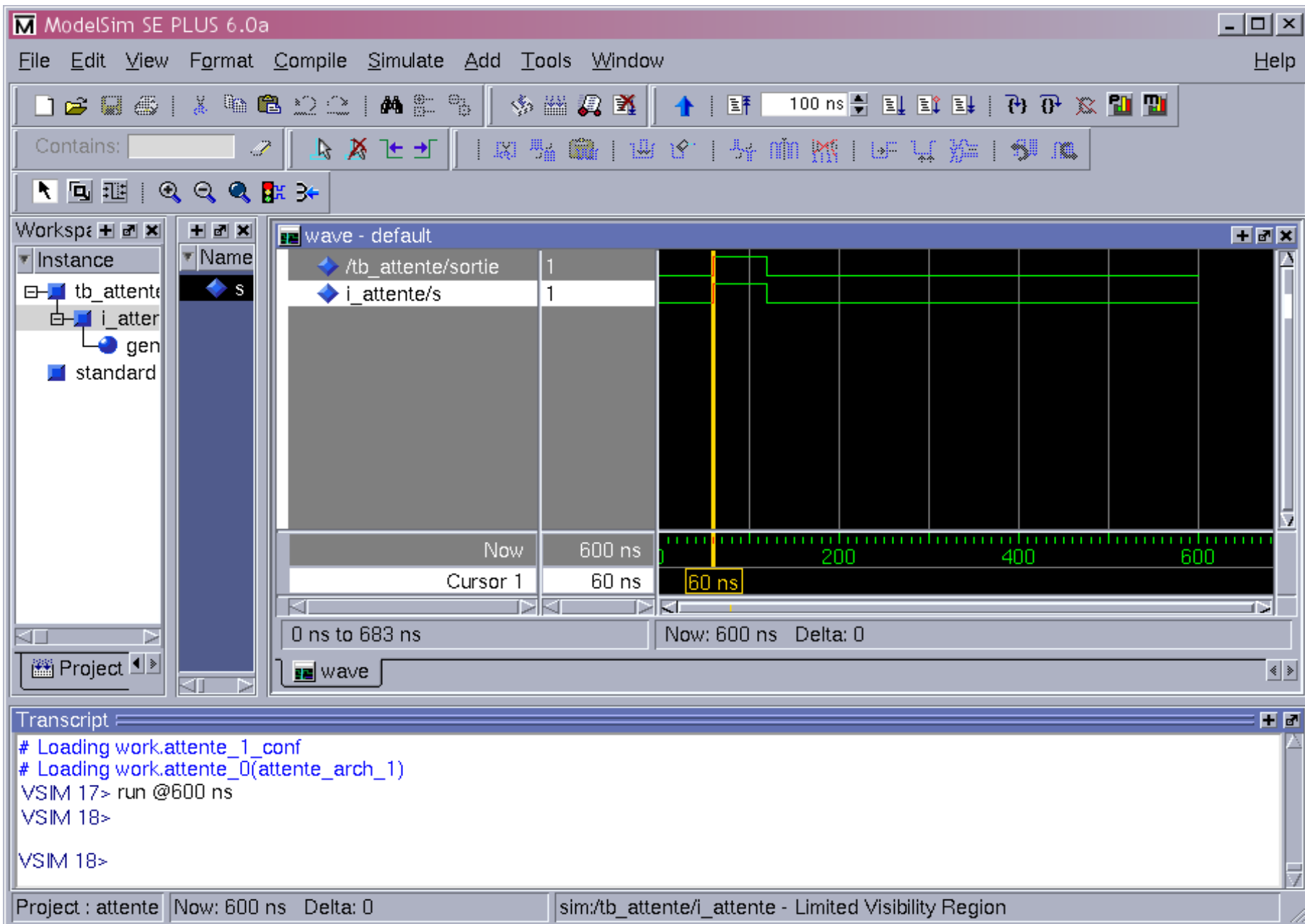
Project : attente | Now: 600 ns Delta: 2 | sim:/tb_attente/i_attente - Limited Visibility Region

Tentative de synthèse

```
Cadence Physically Knowledgeable Synthesis
File Edit View Commands PKS Reports Window Help
[Icons] cadence

<TECHLIB-305>.
CORE9GPLL
pks_shell[7]>set_global target_technology {CORE9GPLL }
pks_shell[8]>read_vhdl ../VHDL/attente_0.vhd
Info: Current VHDL working library is 'TEMP' (mapped to '/tmp/hpt7awmYq/vhdl/TEMP') <VHDL-229>.
==> ERROR: Multiple 'wait' statements in a VHDL process are unsupported (File ../VHDL/attente_0.vhd, Line
24)
<VHDL-669>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File
../VHDL/attente_0.vhd,
Line 24) <VHDL-607>.
--> WARNING: Timeout clauses in wait statements are ignored for synthesis. This may cause mismatches between
simulation
and synthesis (File ../VHDL/attente_0.vhd, Line 24) <VHDL-618>.
==> ERROR: Multiple 'wait' statements in a VHDL process are unsupported (File ../VHDL/attente_0.vhd, Line
26)
<VHDL-669>.
--> WARNING: A 'wait' statement that is not the first statement of the process may result in simulation
mismatches (File
../VHDL/attente_0.vhd, Line 26) <VHDL-668>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File
../VHDL/attente_0.vhd,
Line 26) <VHDL-607>.
--> WARNING: Timeout clauses in wait statements are ignored for synthesis. This may cause mismatches between
simulation
and synthesis (File ../VHDL/attente_0.vhd, Line 26) <VHDL-618>.
for attente_arch_0
|
==> ERROR: No architecture attente_arch_0 for configured entity attente_0 (File ../VHDL/attente_0.vhd, Line
36)
<VHDLPT-683>.
==> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell[9]>
```

TB1 / attente 1



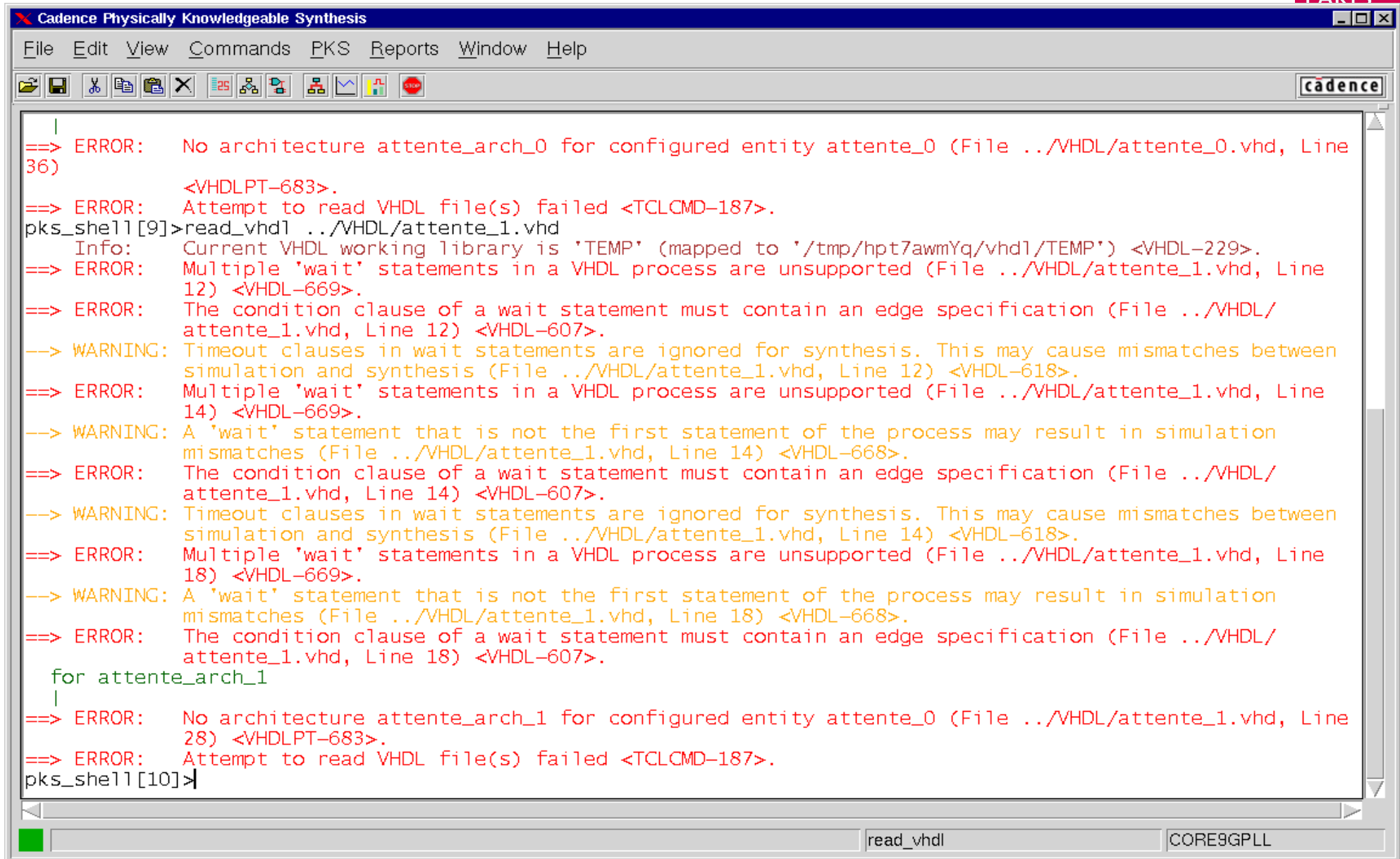
The image shows the ModelSim SE PLUS 6.0a interface. The main window displays a waveform titled "wave - default" with two signals: "/tb_attente/sortie" and "i_attente/s". The waveform shows a step function for "i_attente/s" that transitions from 0 to 1 at approximately 60 ns. The "sortie" signal remains at 0. A yellow cursor is positioned at 60 ns, and a measurement box indicates a duration of 60 ns. The time axis is marked at 0, 200, 400, and 600 ns. The status bar at the bottom indicates "Now: 600 ns Delta: 0".

The Transcript window shows the following text:

```
# Loading work.attente_1_conf
# Loading work.attente_0(attente_arch_1)
VSIM 17> run @600 ns
VSIM 18>
VSIM 18>
```

The Project window shows the project name "attente". The status bar at the bottom indicates "Project : attente Now: 600 ns Delta: 0" and "sim:/tb_attente/i_attente - Limited Visibility Region".

Tentative de synthèse



```
File Edit View Commands PKS Reports Window Help
cadence

=> ERROR: No architecture attente_arch_0 for configured entity attente_0 (File ../VHDL/attente_0.vhd, Line 36)
      <VHDLPT-683>.
=> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell [9]>read_vhdl ../VHDL/attente_1.vhd
Info: Current VHDL working library is 'TEMP' (mapped to '/tmp/hpt7awmYq/vhdl/TEMP') <VHDL-229>.
=> ERROR: Multiple 'wait' statements in a VHDL process are unsupported (File ../VHDL/attente_1.vhd, Line 12) <VHDL-669>.
=> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/attente_1.vhd, Line 12) <VHDL-607>.
--> WARNING: Timeout clauses in wait statements are ignored for synthesis. This may cause mismatches between simulation and synthesis (File ../VHDL/attente_1.vhd, Line 12) <VHDL-618>.
=> ERROR: Multiple 'wait' statements in a VHDL process are unsupported (File ../VHDL/attente_1.vhd, Line 14) <VHDL-669>.
--> WARNING: A 'wait' statement that is not the first statement of the process may result in simulation mismatches (File ../VHDL/attente_1.vhd, Line 14) <VHDL-668>.
=> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/attente_1.vhd, Line 14) <VHDL-607>.
--> WARNING: Timeout clauses in wait statements are ignored for synthesis. This may cause mismatches between simulation and synthesis (File ../VHDL/attente_1.vhd, Line 14) <VHDL-618>.
=> ERROR: Multiple 'wait' statements in a VHDL process are unsupported (File ../VHDL/attente_1.vhd, Line 18) <VHDL-669>.
--> WARNING: A 'wait' statement that is not the first statement of the process may result in simulation mismatches (File ../VHDL/attente_1.vhd, Line 18) <VHDL-668>.
=> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/attente_1.vhd, Line 18) <VHDL-607>.
  for attente_arch_1
  |
=> ERROR: No architecture attente_arch_1 for configured entity attente_0 (File ../VHDL/attente_1.vhd, Line 28) <VHDLPT-683>.
=> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell [10]>
```

read_vhdl CORE9GPLL

TB2 / attente 2

The screenshot displays the ModelSim SE PLUS 6.0a interface. The main window shows a waveform titled 'wave - default' with two signals: '/tb_attente/sortie' (output) and '/tb_attente/clock' (clock). The clock signal is a square wave with a period of 100 ns. The output signal is a square wave that is high for the first half of each clock cycle and low for the second half. A yellow cursor is positioned at 50 ns, with a '50 ns' label below it. The time scale is set to 100 ns. The transcript window at the bottom shows the following text:

```
# Loading work.tb_attente(tb_attente_2_arch)
# Loading work.attente_2_conf
# Loading work.attente_1(attente_arch_2)
VSIM 19> run @600 ns
VSIM 20>
```

The status bar at the bottom indicates 'Project : attente', 'Now: 600 ns Delta: 2', and 'sim:/tb_attente - Limited Visibility Region'.

Tentative de synthèse

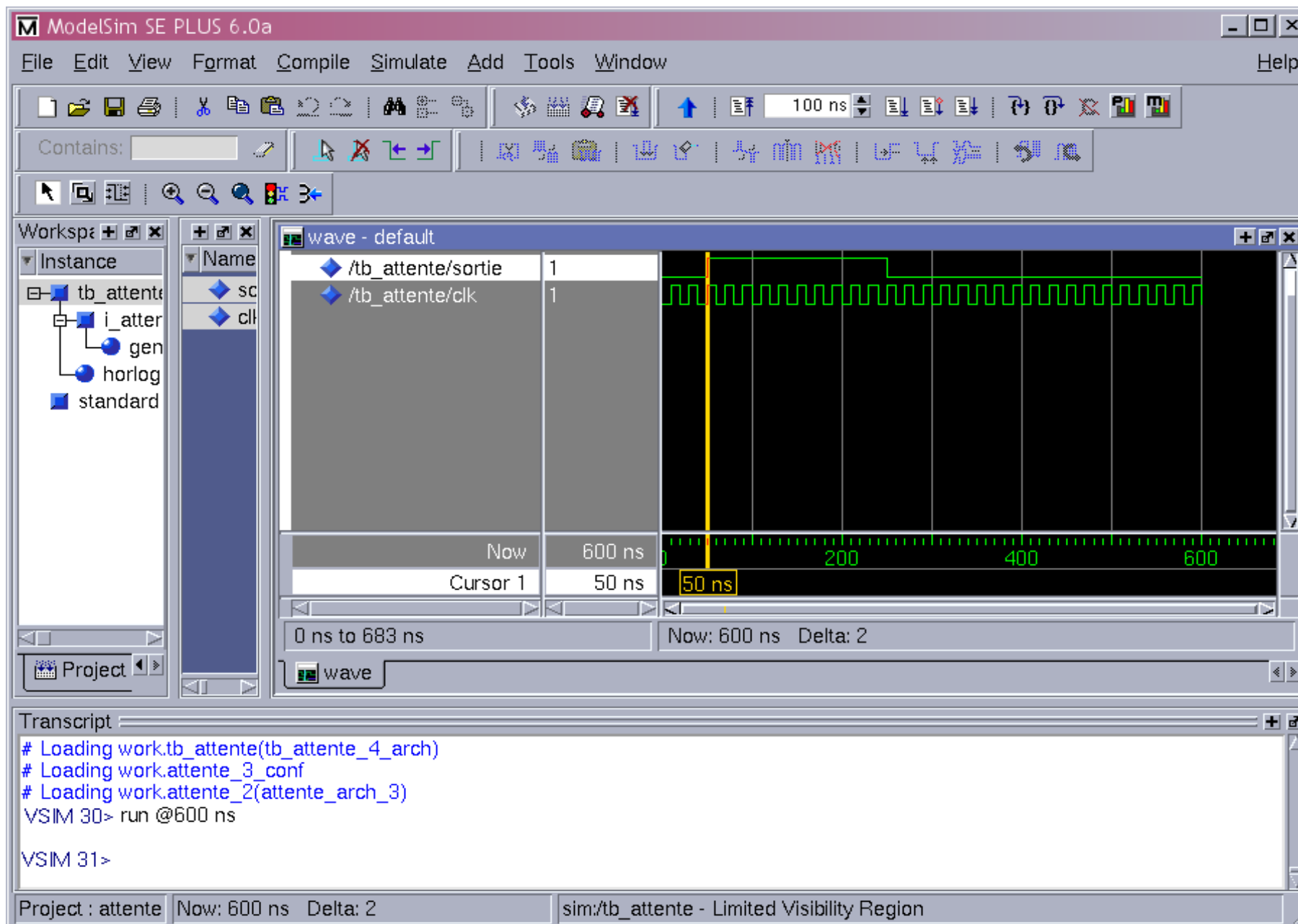


```
Cadence Physically Knowledgeable Synthesis
File Edit View Commands PKS Reports Window Help
[Icons] cadence

pks_shell [10]>read_vhdl ../VHDL/attente_2.vhd
Info: Current VHDL working library is 'TEMP' (mapped to '/tmp/hpt7awmYq/vhdl/TEMP') <VHDL-229>.
==> ERROR: Multiple 'wait' statements in a VHDL process are unsupported (File ../VHDL/attente_2.vhd, Line
25) <VHDL-669>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_2.vhd, Line 25) <VHDL-607>.
==> ERROR: Multiple 'wait' statements in a VHDL process are unsupported (File ../VHDL/attente_2.vhd, Line
27) <VHDL-669>.
--> WARNING: A 'wait' statement that is not the first statement of the process may result in simulation
mismatches (File ../VHDL/attente_2.vhd, Line 27) <VHDL-668>.
==> ERROR: Multiple 'wait' statements in a VHDL process are unsupported (File ../VHDL/attente_2.vhd, Line
31) <VHDL-669>.
--> WARNING: A 'wait' statement that is not the first statement of the process may result in simulation
mismatches (File ../VHDL/attente_2.vhd, Line 31) <VHDL-668>.
==> ERROR: A wait must be the first statement of the process (File ../VHDL/attente_2.vhd, Line 37)
<VHDL-606>.
==> ERROR: Clock-edge is supported only in process statements. See 'help VHDL-656' for more details (File
..
../VHDL/attente_2.vhd, Line 37) <VHDL-656>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_2.vhd, Line 37) <VHDL-607>.
==> ERROR: Multiple 'wait' statements in a VHDL process are unsupported (File ../VHDL/attente_2.vhd, Line
42) <VHDL-669>.
--> WARNING: A 'wait' statement that is not the first statement of the process may result in simulation
mismatches (File ../VHDL/attente_2.vhd, Line 42) <VHDL-668>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_2.vhd, Line 42) <VHDL-607>.
for attente_arch_2
|
==> ERROR: No architecture attente_arch_2 for configured entity attente_1 (File ../VHDL/attente_2.vhd, Line
51) <VHDLPT-683>.
==> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell [11]>|

read_vhdl CORE9GPLL
```

TB4 / attente 3



The screenshot shows the ModelSim SE PLUS 6.0a interface. The main window displays a waveform titled "wave - default" with two signals: `/tb_attente/sortie` and `/tb_attente/clk`. The `clk` signal is a periodic square wave, and the `sortie` signal is a square wave that changes state at each clock edge. A yellow cursor is positioned at 50 ns on the `sortie` signal. The time scale is set to 100 ns. The transcript window shows the following text:

```
# Loading work.tb_attente(tb_attente_4_arch)
# Loading work.attente_3_conf
# Loading work.attente_2(attente_arch_3)
VSIM 30> run @600 ns

VSIM 31>
```

The status bar at the bottom indicates "Project : attente", "Now: 600 ns Delta: 2", and "sim:/tb_attente - Limited Visibility Region".

Tentative de synthèse

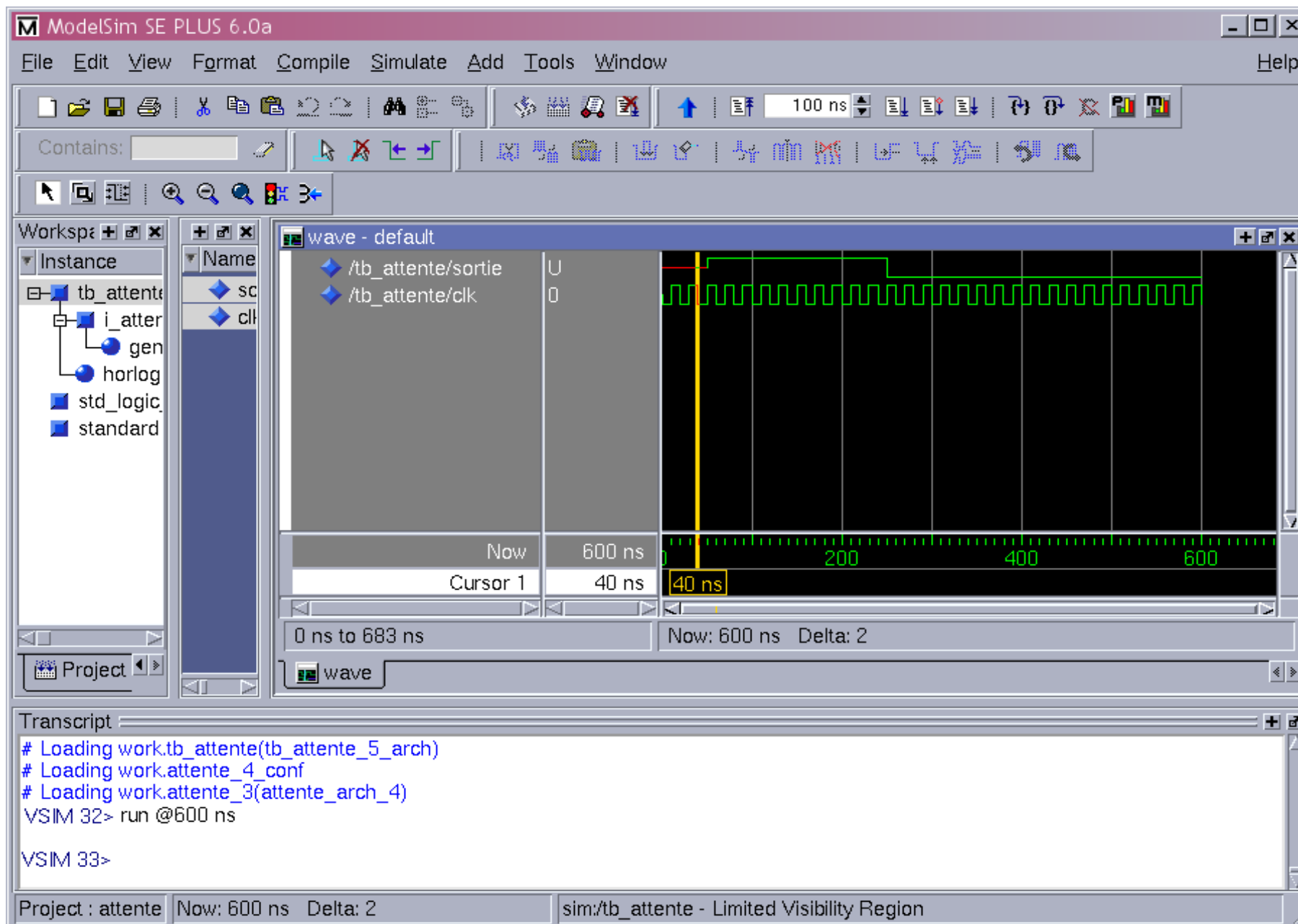


```
Cadence Physically Knowledgeable Synthesis
File Edit View Commands PKS Reports Window Help
[Icons] cadence

for attente_arch_2
|
==> ERROR: No architecture attente_arch_2 for configured entity attente_1 (File ../VHDL/attente_2.vhd, Line
51) <VHDLPT-683>.
==> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell[11]>read_vhdl ../VHDL/attente_3.vhd
Info: Current VHDL working library is 'TEMP' (mapped to '/tmp/hpt7awmYq/vhd1/TEMP') <VHDL-229>.
==> ERROR: A wait must be the first statement of the process (File ../VHDL/attente_3.vhd, Line 28)
<VHDL-606>.
==> ERROR: Clock-edge is supported only in process statements. See 'help VHDL-656' for more details (File
..
../VHDL/attente_3.vhd, Line 28) <VHDL-656>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_3.vhd, Line 28) <VHDL-607>.
==> ERROR: A wait must be the first statement of the process (File ../VHDL/attente_3.vhd, Line 36)
<VHDL-606>.
==> ERROR: Clock-edge is supported only in process statements. See 'help VHDL-656' for more details (File
..
../VHDL/attente_3.vhd, Line 36) <VHDL-656>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_3.vhd, Line 36) <VHDL-607>.
==> ERROR: Multiple 'wait' statements in a VHDL process are unsupported (File ../VHDL/attente_3.vhd, Line
42) <VHDL-669>.
--> WARNING: A 'wait' statement that is not the first statement of the process may result in simulation
mismatches (File ../VHDL/attente_3.vhd, Line 42) <VHDL-668>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_3.vhd, Line 42) <VHDL-607>.
for attente_arch_3
|
==> ERROR: No architecture attente_arch_3 for configured entity attente_2 (File ../VHDL/attente_3.vhd, Line
51) <VHDLPT-683>.
==> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell[12]>

[Progress bar] read_vhdl CORE9GPLL
```

TB5 / attente 4



The screenshot shows the ModelSim SE PLUS 6.0a simulation environment. The main window displays a timing diagram for a testbench named 'tb_attente'. The diagram shows two signals: '/tb_attente/sortie' (output) and '/tb_attente/clock' (clk). The clock signal is a periodic square wave with a period of 40 ns. The output signal is a square wave that is high during the first half of each clock cycle and low during the second half. A yellow cursor is positioned at the 40 ns mark on the time axis, indicating the current simulation time. The time axis ranges from 0 ns to 683 ns, with major ticks every 200 ns. The simulation is currently at 600 ns, with a delta of 2 ns. The transcript window at the bottom shows the following commands and output:

```
# Loading work.tb_attente(tb_attente_5_arch)
# Loading work.attente_4_conf
# Loading work.attente_3(attente_arch_4)
VSIM 32> run @600 ns
VSIM 33>
```

The status bar at the bottom of the window displays: Project : attente, Now: 600 ns Delta: 2, and sim:/tb_attente - Limited Visibility Region.

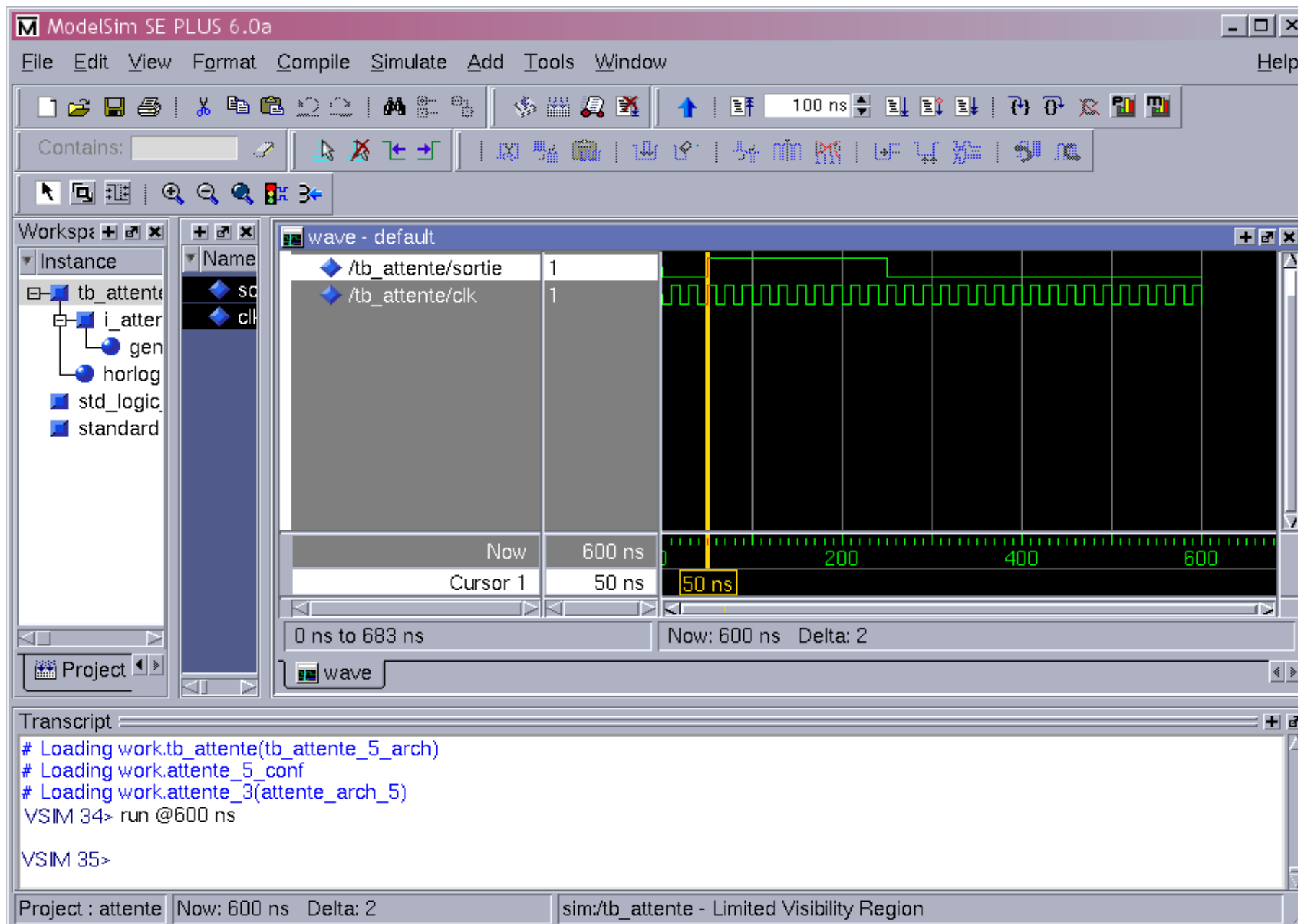
Tentative de synthèse

```
Cadence Physically Knowledgeable Synthesis
File Edit View Commands PKS Reports Window Help
cadence

for attente_arch_3
|
==> ERROR: No architecture attente_arch_3 for configured entity attente_2 (File ../VHDL/attente_3.vhd, Line
51) <VHDLPT-683>.
==> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.|
pks_shell[12]>read_vhdl ../VHDL/attente_4.vhd
Info: Current VHDL working library is 'TEMP' (mapped to '/tmp/hpt7awmYq/vhd1/TEMP') <VHDL-229>.
==> ERROR: A wait must be the first statement of the process (File ../VHDL/attente_4.vhd, Line 30)
<VHDL-606>.
==> ERROR: Clock-edge is supported only in process statements. See 'help VHDL-656' for more details (File
..
../VHDL/attente_4.vhd, Line 30) <VHDL-656>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_4.vhd, Line 30) <VHDL-607>.
==> ERROR: A wait must be the first statement of the process (File ../VHDL/attente_4.vhd, Line 38)
<VHDL-606>.
==> ERROR: Clock-edge is supported only in process statements. See 'help VHDL-656' for more details (File
..
../VHDL/attente_4.vhd, Line 38) <VHDL-656>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_4.vhd, Line 38) <VHDL-607>.
==> ERROR: Multiple 'wait' statements in a VHDL process are unsupported (File ../VHDL/attente_4.vhd, Line
44) <VHDL-669>.
--> WARNING: A 'wait' statement that is not the first statement of the process may result in simulation
mismatches (File ../VHDL/attente_4.vhd, Line 44) <VHDL-668>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_4.vhd, Line 44) <VHDL-607>.
for attente_arch_4
|
==> ERROR: No architecture attente_arch_4 for configured entity attente_3 (File ../VHDL/attente_4.vhd, Line
53) <VHDLPT-683>.
==> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell[13]>

read_vhdl CORE9GPLL
```

TB6 / attente 5

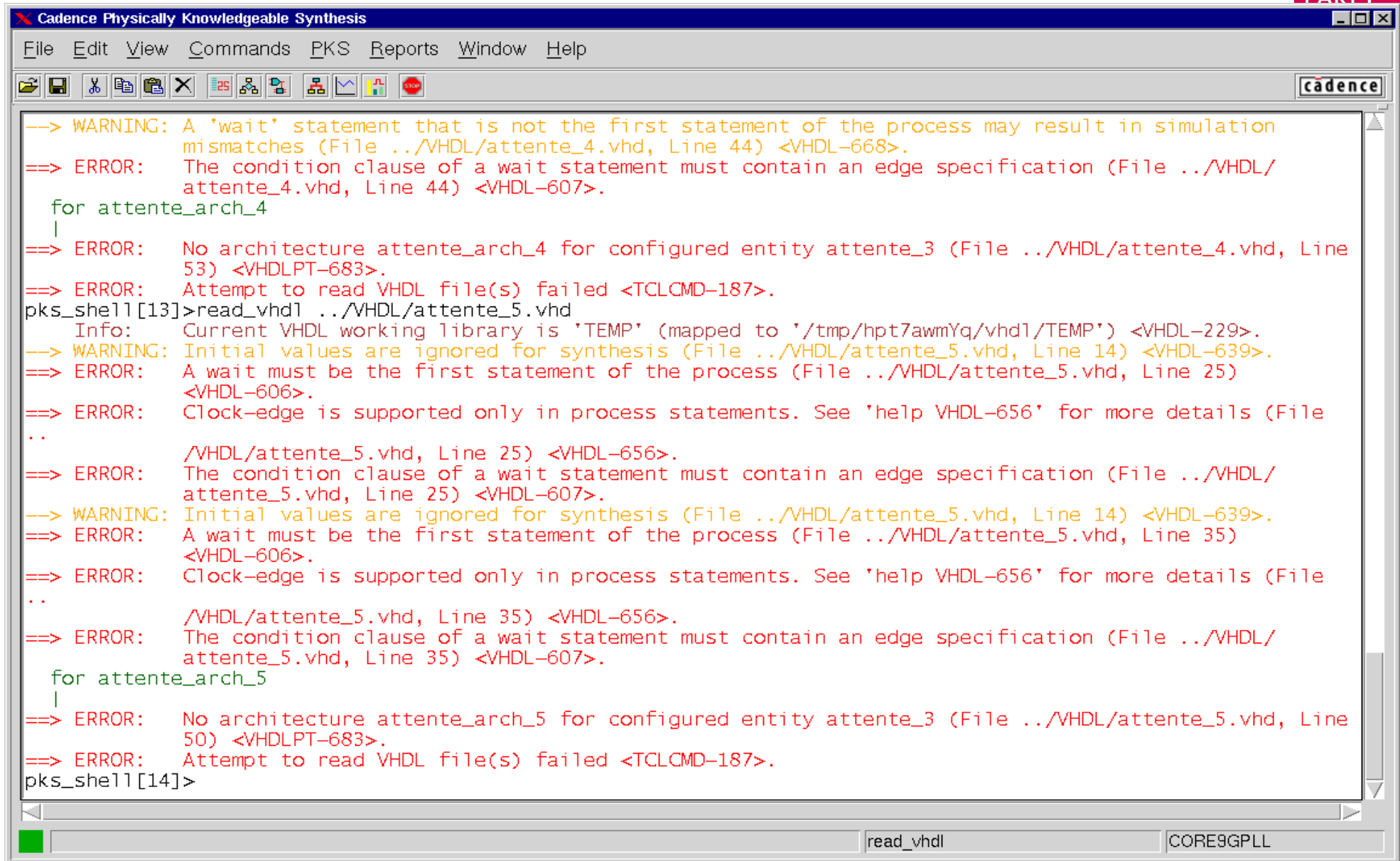


The screenshot shows the ModelSim SE PLUS 6.0a interface. The main window displays a waveform titled 'wave - default' with two signals: '/tb_attente/sortie' and '/tb_attente/clk'. The 'sortie' signal is a square wave that transitions from low to high at approximately 100 ns and remains high. The 'clk' signal is a periodic square wave. A yellow cursor is positioned at 50 ns on the 'sortie' signal. The time scale is set to 100 ns. The transcript window at the bottom shows the following text:

```
# Loading work.tb_attente(tb_attente_5_arch)
# Loading work.attente_5_conf
# Loading work.attente_3(attente_arch_5)
VSIM 34> run @600 ns
VSIM 35>
```

The status bar at the bottom indicates 'Project : attente', 'Now: 600 ns Delta: 2', and 'sim:/tb_attente - Limited Visibility Region'.

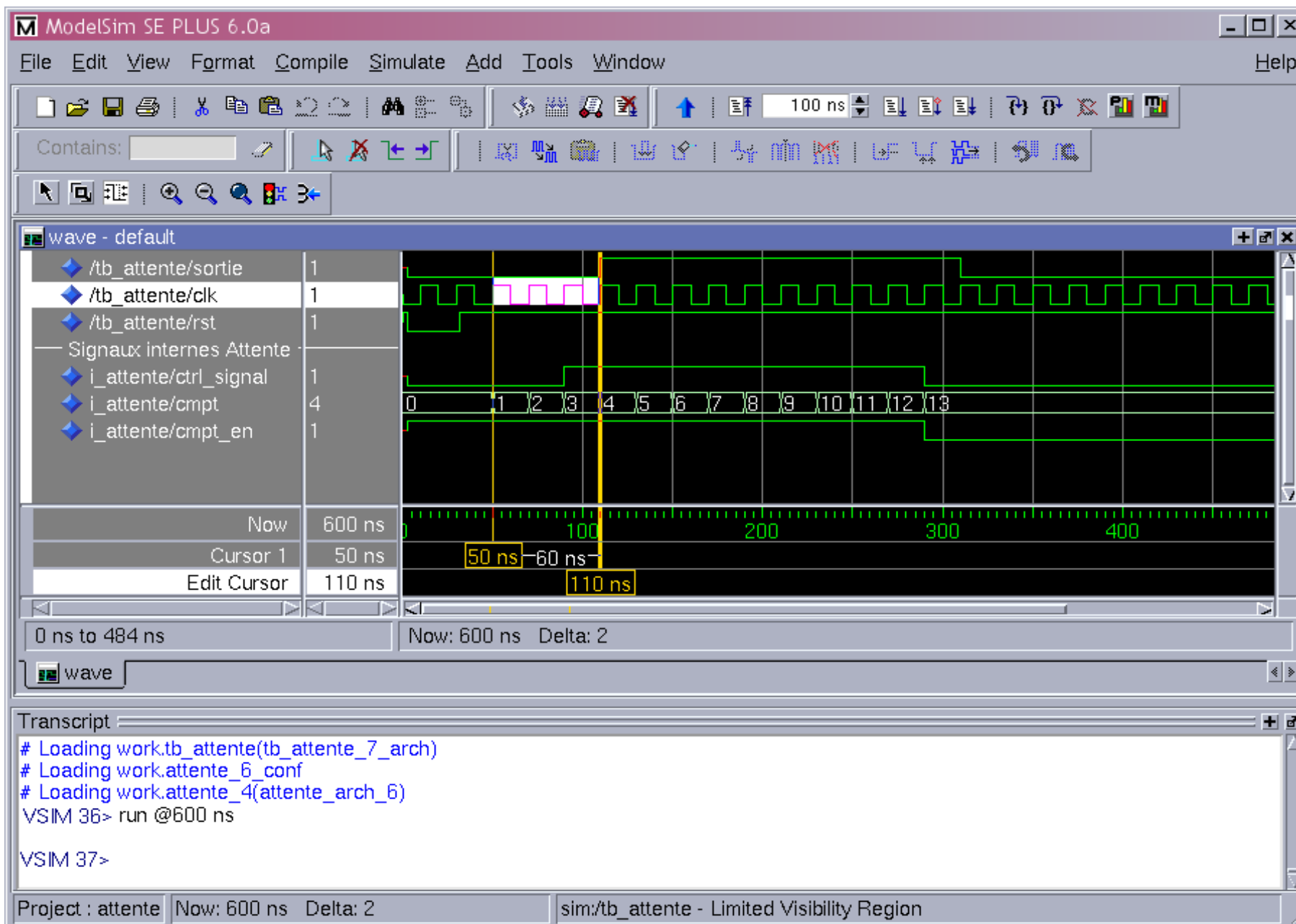
Tentative de synthèse



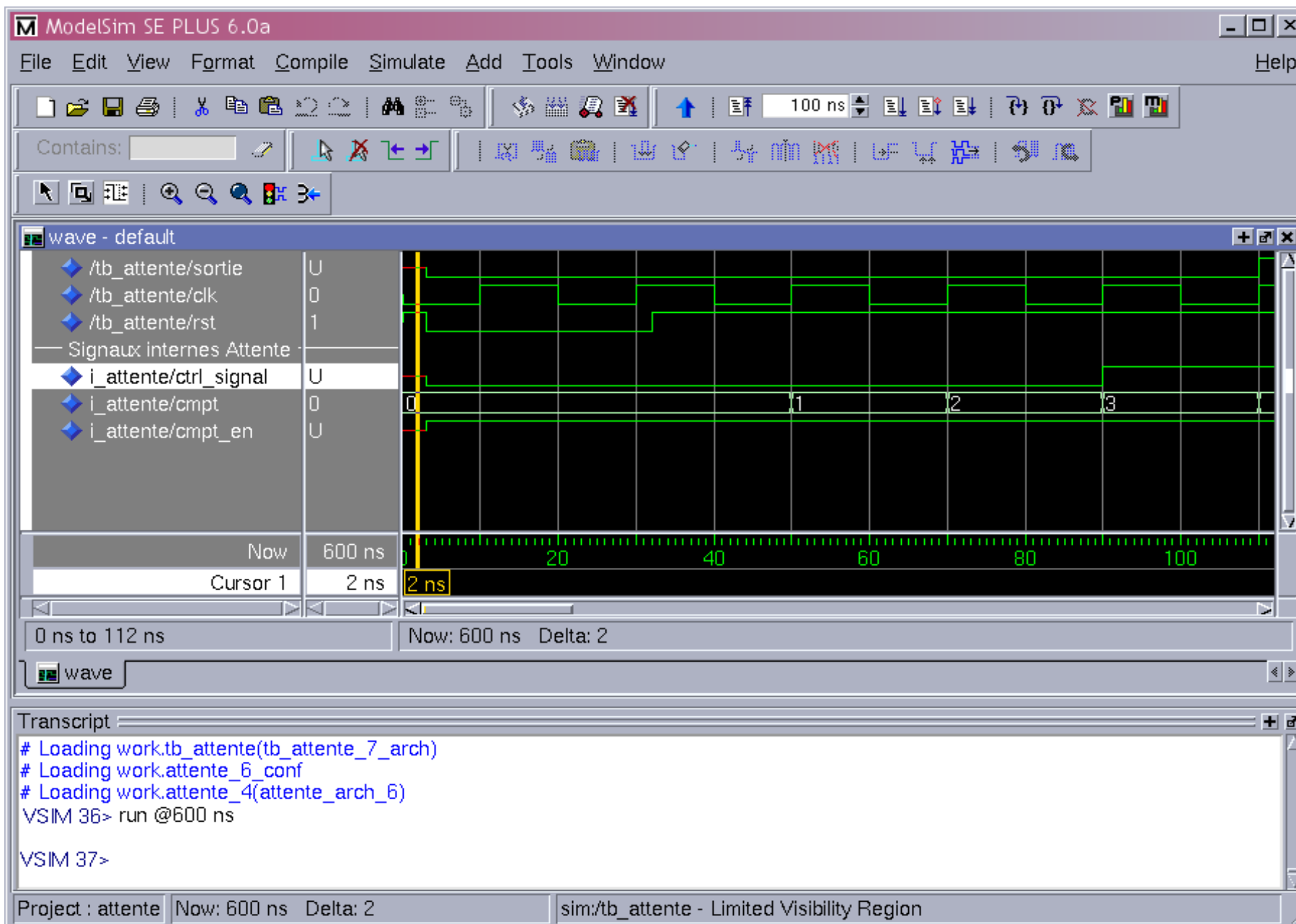
```
File Edit View Commands PKS Reports Window Help
--> WARNING: A 'wait' statement that is not the first statement of the process may result in simulation
mismatches (File ../VHDL/attente_4.vhd, Line 44) <VHDL-668>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_4.vhd, Line 44) <VHDL-607>.
for attente_arch_4
|
==> ERROR: No architecture attente_arch_4 for configured entity attente_3 (File ../VHDL/attente_4.vhd, Line
53) <VHDLPT-683>.
==> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell[13]>read_vhdl ../VHDL/attente_5.vhd
Info: Current VHDL working library is 'TEMP' (mapped to '/tmp/hpt7awmYq/vhdl/TEMP') <VHDL-229>.
--> WARNING: Initial values are ignored for synthesis (File ../VHDL/attente_5.vhd, Line 14) <VHDL-639>.
==> ERROR: A wait must be the first statement of the process (File ../VHDL/attente_5.vhd, Line 25)
<VHDL-606>.
==> ERROR: Clock-edge is supported only in process statements. See 'help VHDL-656' for more details (File
..
/VHDL/attente_5.vhd, Line 25) <VHDL-656>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_5.vhd, Line 25) <VHDL-607>.
--> WARNING: Initial values are ignored for synthesis (File ../VHDL/attente_5.vhd, Line 14) <VHDL-639>.
==> ERROR: A wait must be the first statement of the process (File ../VHDL/attente_5.vhd, Line 35)
<VHDL-606>.
==> ERROR: Clock-edge is supported only in process statements. See 'help VHDL-656' for more details (File
..
/VHDL/attente_5.vhd, Line 35) <VHDL-656>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_5.vhd, Line 35) <VHDL-607>.
for attente_arch_5
|
==> ERROR: No architecture attente_arch_5 for configured entity attente_3 (File ../VHDL/attente_5.vhd, Line
50) <VHDLPT-683>.
==> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell[14]>
```

read_vhdl CORE9GPLL

TB 7 / attente 6



TB7-Bis /attente_6 détail du reset



Tentative de synthèse

```
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cadence

==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_4.vhd, Line 44) <VHDL-607>.
for attente_arch_4
|
==> ERROR: No architecture attente_arch_4 for configured entity attente_3 (File ../VHDL/attente_4.vhd, Line
53) <VHDLPT-683>.
==> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell[13]>read_vhdl ../VHDL/attente_5.vhd
Info: Current VHDL working library is 'TEMP' (mapped to '/tmp/hpt7awmYq/vhdl/TEMP') <VHDL-229>.
--> WARNING: Initial values are ignored for synthesis (File ../VHDL/attente_5.vhd, Line 14) <VHDL-639>.
==> ERROR: A wait must be the first statement of the process (File ../VHDL/attente_5.vhd, Line 25)
<VHDL-606>.
==> ERROR: Clock-edge is supported only in process statements. See 'help VHDL-656' for more details (File
..
/VHDL/attente_5.vhd, Line 25) <VHDL-656>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_5.vhd, Line 25) <VHDL-607>.
--> WARNING: Initial values are ignored for synthesis (File ../VHDL/attente_5.vhd, Line 14) <VHDL-639>.
==> ERROR: A wait must be the first statement of the process (File ../VHDL/attente_5.vhd, Line 35)
<VHDL-606>.
==> ERROR: Clock-edge is supported only in process statements. See 'help VHDL-656' for more details (File
..
/VHDL/attente_5.vhd, Line 35) <VHDL-656>.
==> ERROR: The condition clause of a wait statement must contain an edge specification (File ../VHDL/
attente_5.vhd, Line 35) <VHDL-607>.
for attente_arch_5
|
==> ERROR: No architecture attente_arch_5 for configured entity attente_3 (File ../VHDL/attente_5.vhd, Line
50) <VHDLPT-683>.
==> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell[14]>read_vhdl ../VHDL/attente_6.vhd
Info: Current VHDL working library is 'TEMP' (mapped to '/tmp/hpt7awmYq/vhdl/TEMP') <VHDL-229>.
pks_shell[15]>
```


Pas d'erreur, on lance la synthèse



Cadence Physically Knowledgeable Synthesis

File Edit View Commands PKS Reports Window Help

Logical Physical Variables

HDL Editor Tcl Editor Constraints Schematic PKS

Verilog

```

==> ERROR: Attempt to read VHDL file(s) failed <TCLCMD-187>.
pks_shell[14]>read_vhdl ../VHDL/attente_6.vhd
Info: Current VHDL working library is 'TEMP' (mapped to '/tmp/hpt7awmYq/vhdl/TEMP') <VHDL-229>.

do_build_clock_tree do_build_generic do_build_physical_tree
pks_shell[15]>do_build_generic
Info: Processing design 'attente_4' <CDFG-303>.

```

Sequential Elements										
Module	File	Line	Name	Type	Width	AS	AR	SS	SR	
attente_4	../VHDL/attente_6.vhd	32	cmpt_en_reg	FF	1	Y	N	N	N	
attente_4	../VHDL/attente_6.vhd	32	cmpt_reg	FF	31	N	Y	N	N	
attente_4	../VHDL/attente_6.vhd	32	ctrl_signal_reg	FF	1	N	Y	N	N	
attente_4	../VHDL/attente_6.vhd	32	s_reg	FF	1	N	Y	N	N	

```

Finished processing module: 'attente_4' <MODGEN-110>.
Info: Setting 'attente_4' as the top of the design hierarchy <FNP-704>.
Info: Setting 'attente_4' as the default top timing module <FNP-705>.
pks_shell[16]>

```

set_global CORE9GPLL

Schéma « RTL » de attente

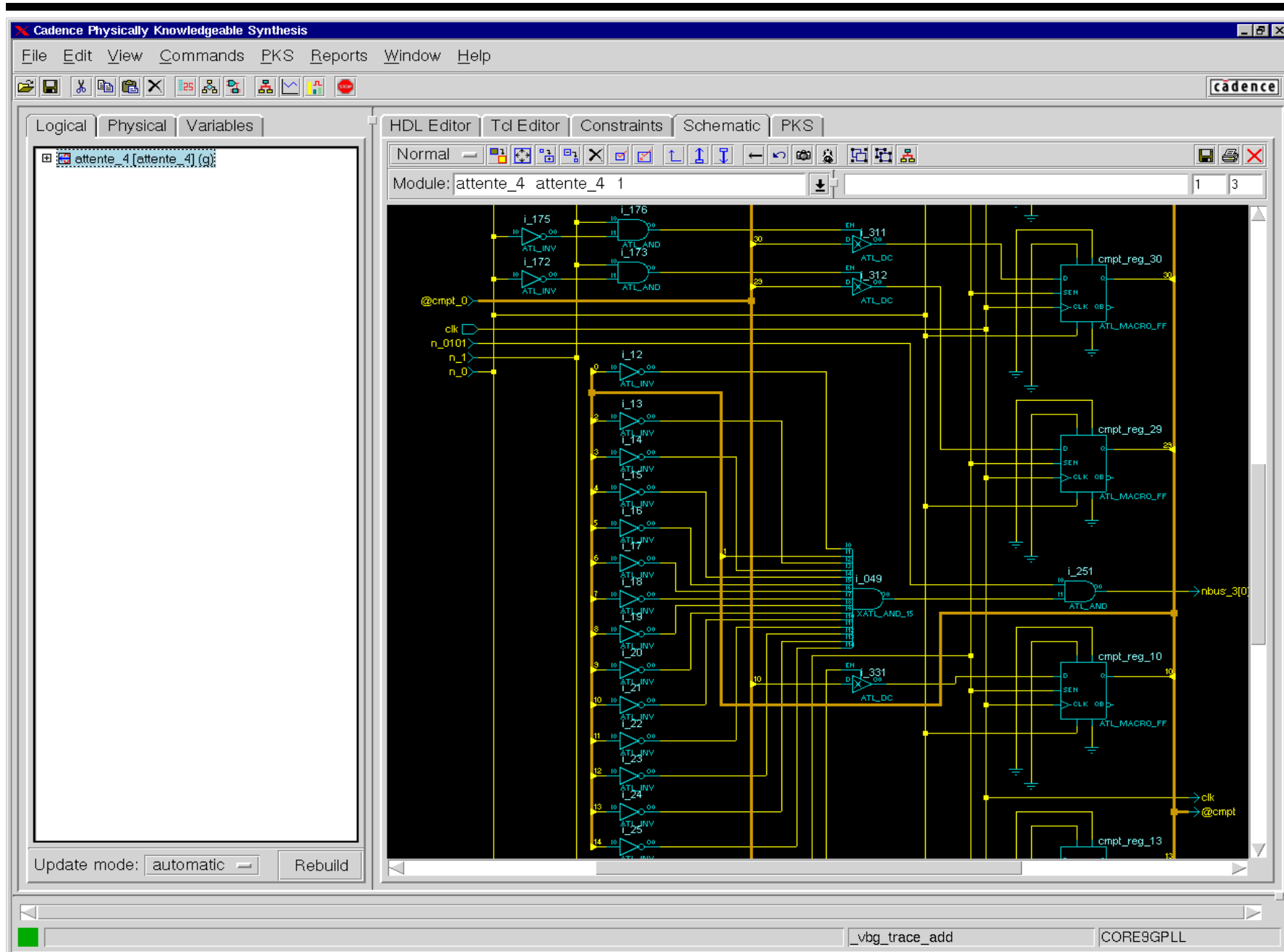


Schéma après optimisation avec la bibliothèque physique

