

Reverse-Engineering of Hardware Circuits

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SR2I301

Presentation Outline

- 1 Introduction
- 2 Invasive techniques
 - Delaying / Tomography
 - Chip edition
- 3 Semi-invasive techniques
 - Preparation
 - Active / passive probing
 - FIRE
- 4 Non-invasive techniques
 - Temporal / spatial localization of the algorithm
- 5 Countermeasures against RE
 - White-box cryptography
 - Active shield against probing
 - Countermeasure against probing attacks
 - Hardware and software camouflage [GMN⁺13]

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Definition of reverse-engineering

Definition

- When the algorithm to attack is unknown, the system is a “black-box”.
- This means that the only way to attack is to analyze the input/output relationships $\Rightarrow$ hard in general (but for cube attacks [DS09, DS10])
- Therefore, the first step is to recover the algorithm.

Hardware versus Software reverse-engineering

- **Software:** The compiled code can be read-out from memories, and disassembled. Typically A5/1, A5/2, Hitag2 and Keeloq have been retrieved like that.
- **Hardware:** The functionality is buried into an ASIC.

Goal of reverse-engineering

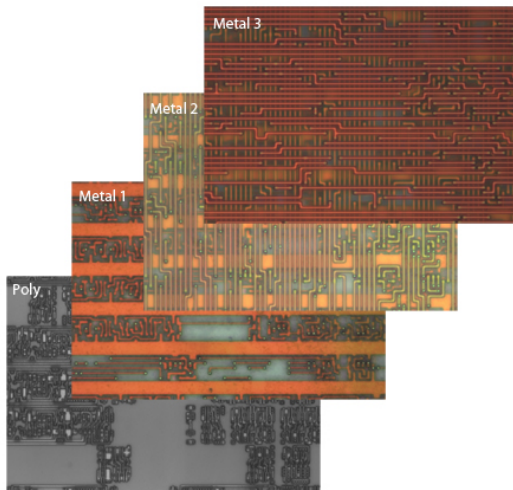
Goals

- ① Retrieving an algorithm and then cryptanalyse it:
 - This was the case of CRYPTO1 (MyFare) or DSC (DECT).
 - Indeed, the confidential algorithm is most often weak.
- ② Breaking a protection:
 - Understand how memories are encrypted by a secure microcontroller [Mah97].
 - Afterwards, all the code is exposed.
 - It thus becomes easy to identify bugs, that can be exploited at the software-level.
 - Thanks to buffer overflows, take the control of the application.
- ③ Intellectual property matters:
 - Accessing the design of a competitor, so as to steal it.
 - Checking that the competitor does not infringe my patents.

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Principle of Circuit Reverse-Engineering: Delaying

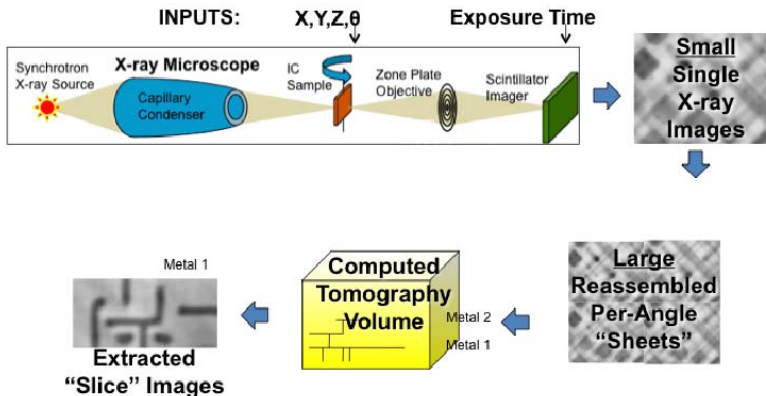


Principle of Circuit Reverse-Engineering:

Tomography [BBT⁺11]

(see also [Zei13])

X-ray Inspection Flowchart



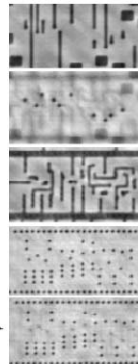
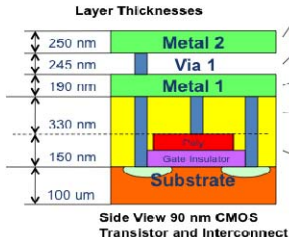
Principle of Circuit Reverse-Engineering:

Tomography [BBT⁺11]

(see also [Zei13])

Imaging Capability: Fine Feature Differentiation on Wiring Layers

Can differentiate finest scale features on smallest layers. E.g. Metal 1 is 190 nm thick with 120 nm feature size. "Lower contact" layer is 150 nm thick with 120 nm feature size.



Metal 2 (140 nm features)

Via 1 (140 nm features)

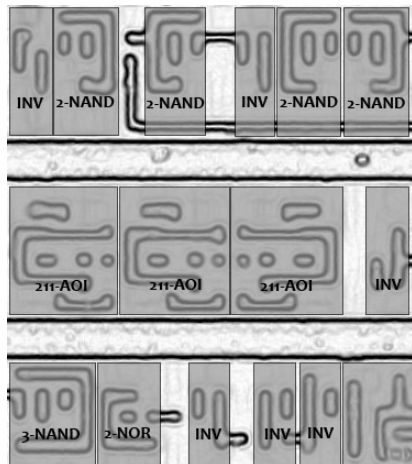
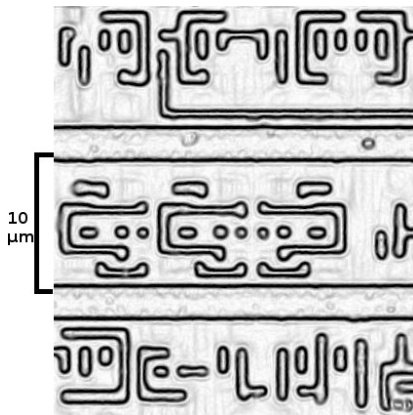
Metal 1 (120 nm features)

"Upper Contact"
 Layer (120 nm features)
 (above transistors)

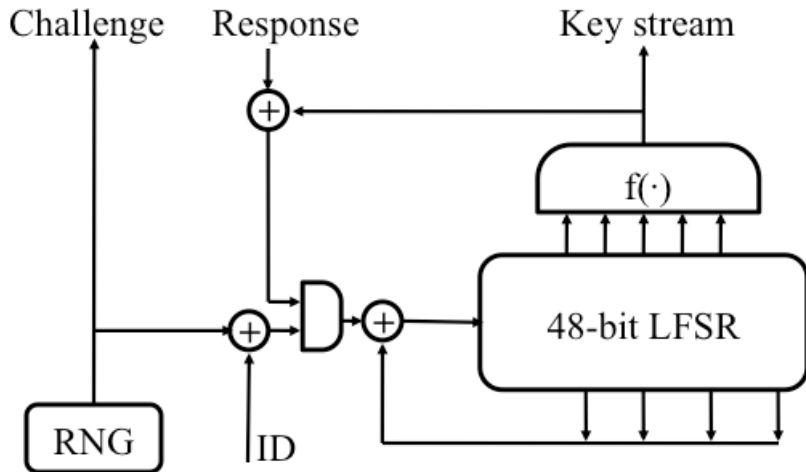
"Lower Contact"
 Layer (120 nm features)
 (below transistors)

6 um x 3.6 um "raw slices"
 of standard cell area

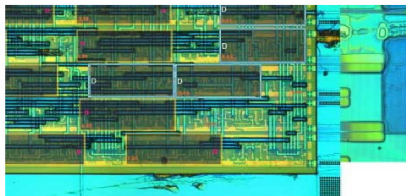
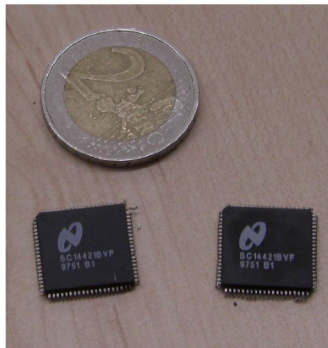
Example of MyFare (NXP) [NSP08]



Example of MyFare (NXP) – CRYPTO1 exposed [NSP08]

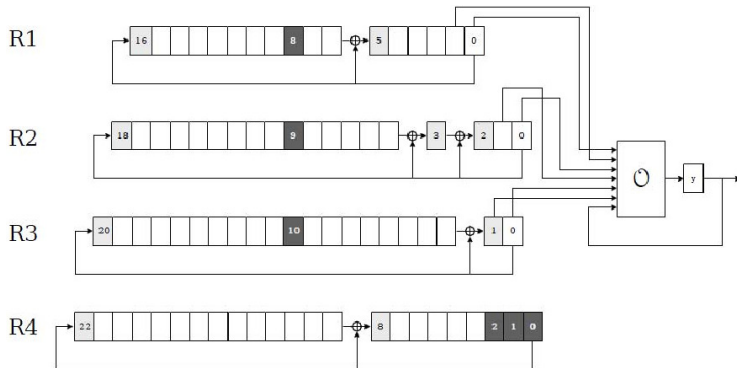


Example of DECT (Alcatel) [NTW10]



See also: <https://deDECTed.org/>.

Example of DECT (Alcatel) – DSC exposed [NTW10]

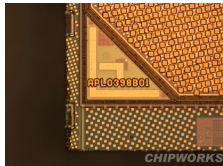


DSC = DECT Standard Cipher.

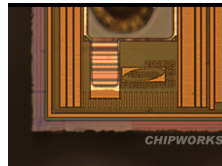
Professional techniques

Example of <http://www.chipworks.com/> [TJ09] iPad tear-down (see also <http://www.ltecusa.com/> and many others).

Apple / Microprocessor (with DRAM)



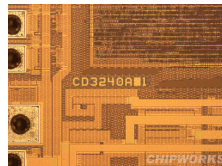
Samsung / 1 Gb mobile DDR SDRAM (x2)



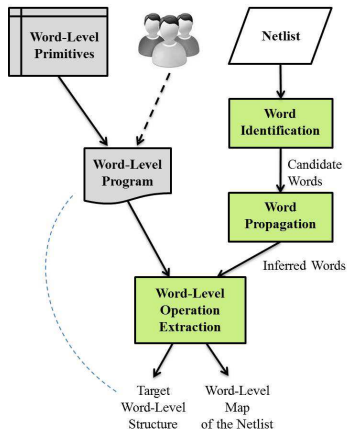
Broadcom / Microcontroller with NVM (used for touchscreen)



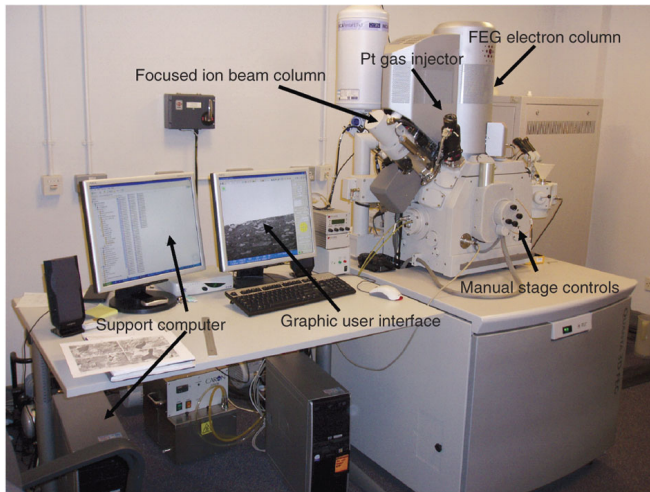
TI / Touchscreen line driver



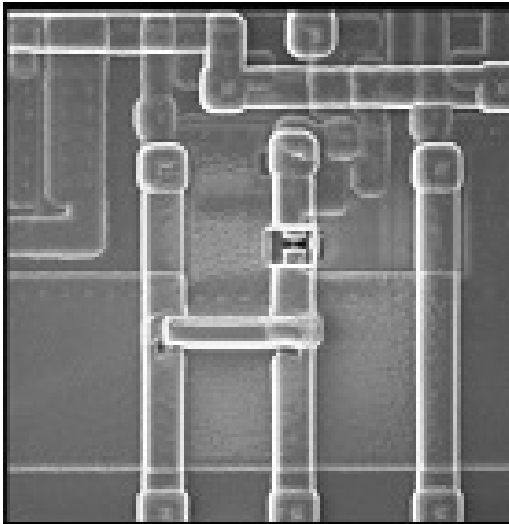
WordRev: Finding word-level structures in a sea of bit-level gates [LGS⁺13]



Focused Ion Beam (FIB)

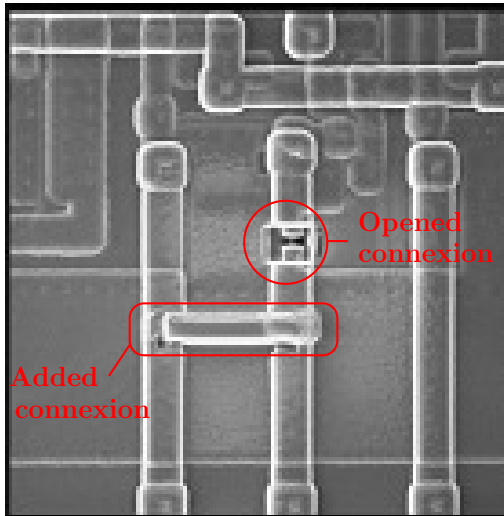


Edition of a circuit thanks to a FIB (Focused Ion Beam)



Can be used for
instance to unlock
memories [Gir07].

Edition of a circuit thanks to a FIB (Focused Ion Beam)

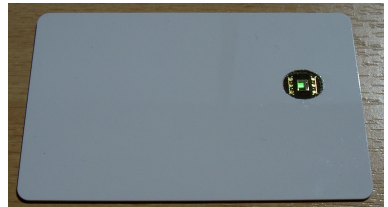
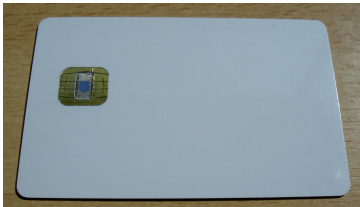
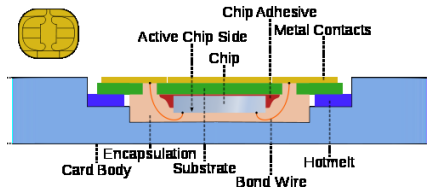


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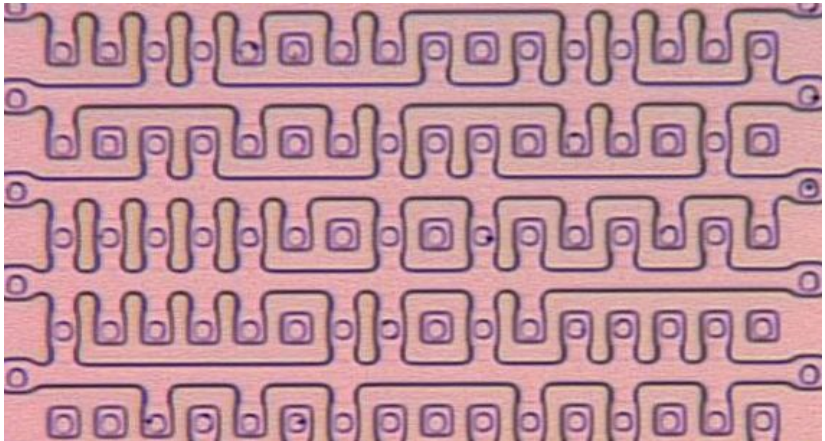
Preparation of a smartcard front- and rear-side



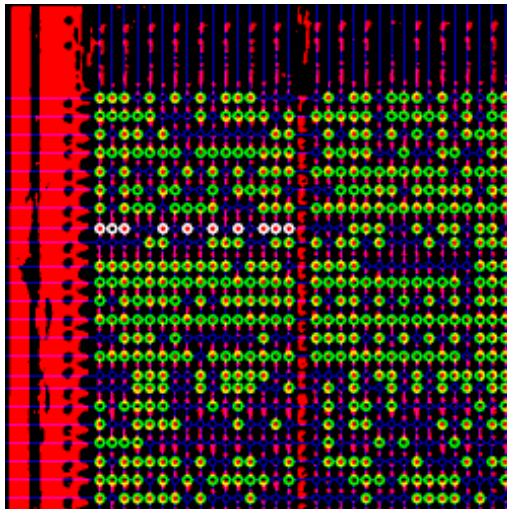
This chemical preparation enables probing and fault injection attacks.

Reading ROMs [KK99]

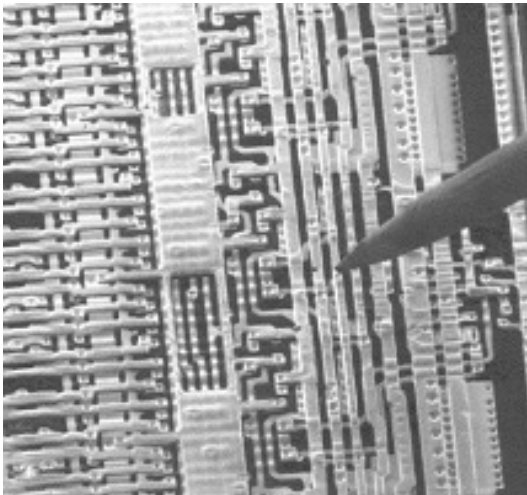
The image shows 16×10 bits in an ST16xyz. Every bit is represented by either a present or missing diffusion layer connection.



Semi-automatic extraction of ROM data (**rompar**)



Needles can be used to actively / passively probe signals



- Can be used for instance to read keys as they circulate into the circuit.
- This technique gives the attacker a considerable power.
- However, probing stations allow to simultaneously read only a couple of bits [**HPS99**]... and only those that are on top of the circuit.

Faults Injection Reverse-Engineering

FIRE on DES / AES

- Already illustrated by Biham & Shamir (reconstructing unknown ciphers [BS97]) on Feistel schemes.
- Works on DES, because the attacker sees *inputs and outputs* differentials (improvement in [LBGRT13]).
- With secret encodings, it still works on DES, because the sbox is non-injective [Cla07].
- FIRE on SPNs (such as AES) is an emerging topic [PMG11].

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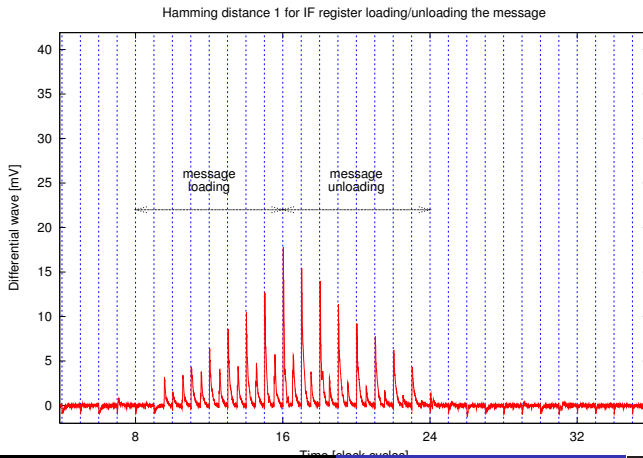
Principle of temporal localization

Use **specific inputs** and **monitor the differences** via one side-channel. For instance, imagine that the key is known.

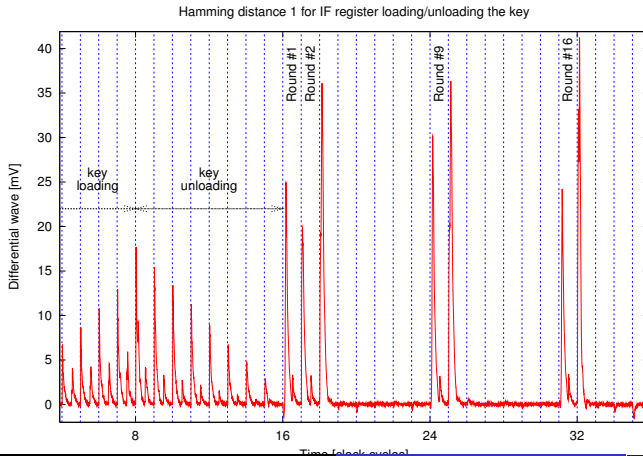
In the next three slides, we suggest to locate:

- 1 the plaintext loading,
- 2 the key loading,
- 3 the key schedule (diversification of the root key for each round).

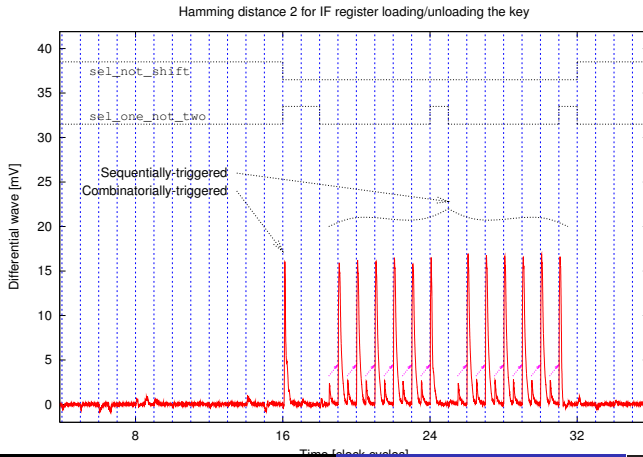
Signature of message loading / unloading in IF (Reminder: IF is the InterFace register)



Signature of key loading / unloading in IF, plus the CD activity

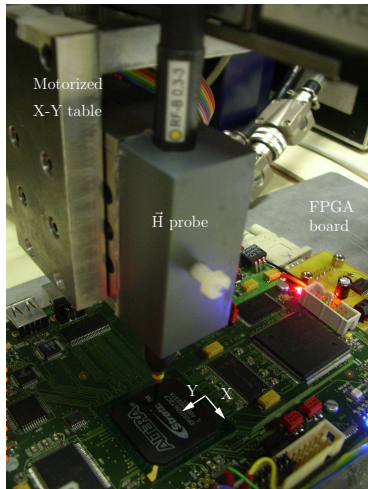


Signature of distance-2 key loading / unloading in IF and of LS^2 in CD



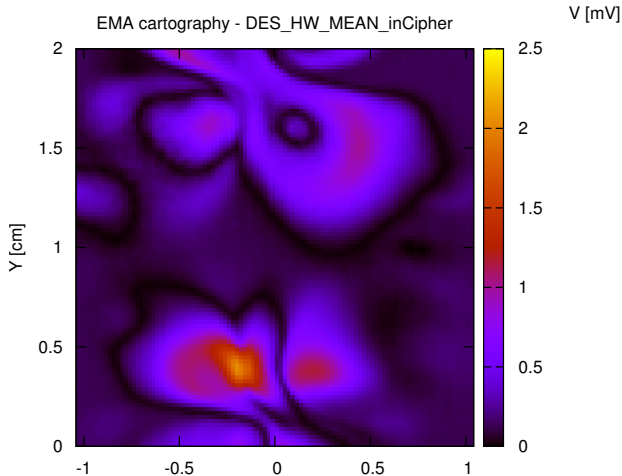
Principle of spacial localization

Using an (X, Y) cartography tool



- Extension: (X, Y, Z, θ) table.
- Helps identify zones that leak a lot; they do not necessarily correspond to the location of the modules! *Id est* they can maybe guide an attack by EMI but not by laser.

Cartography results



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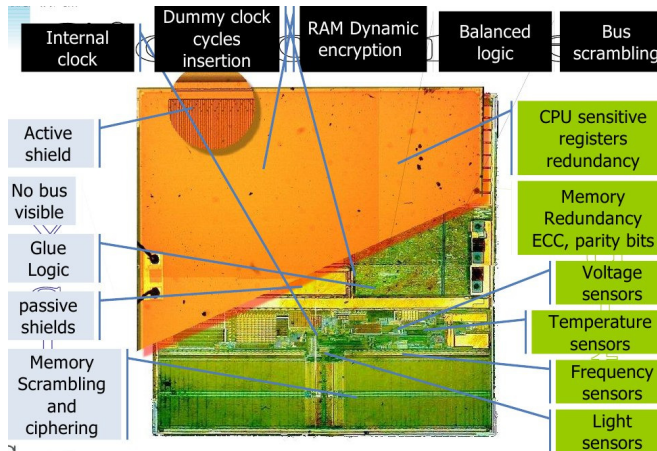
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Example of the white-box cryptography

White-box cryptography [BCD09, CFD⁺10]

- **Principle:** provide everything (*i.e.* the compiled or the source code of the software) of an algorithm embedding a secret key.
- **Goal:** deny to the attacker the power of retrieving the couple (algorithm + key).

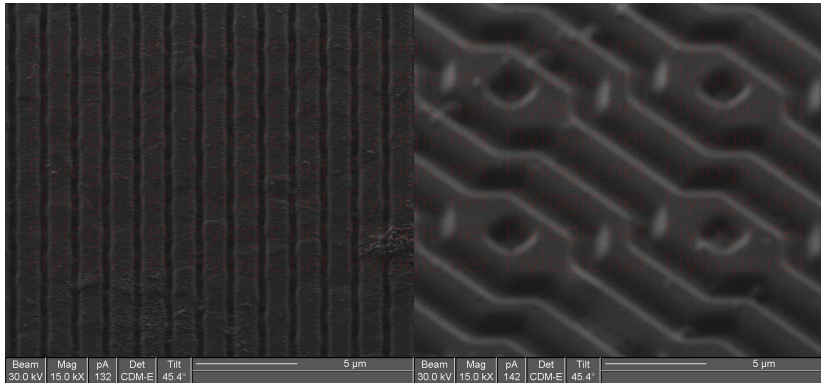
A summary of the countermeasures embedded in a smartcard



Courtesy of Assia Tria, CEA/LETI.

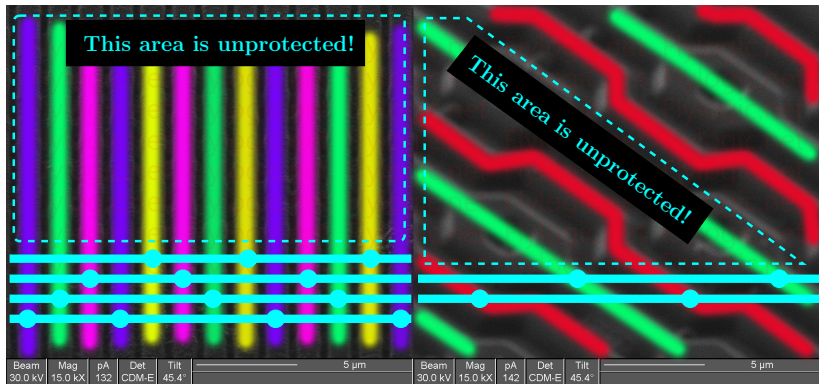
Active shield

1/2



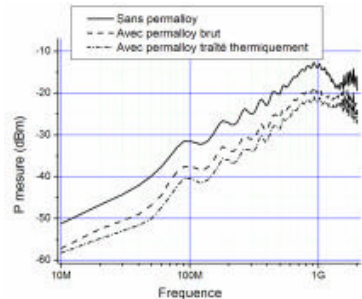
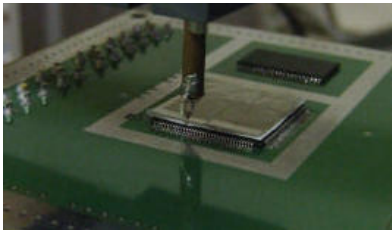
Active shield

2/2



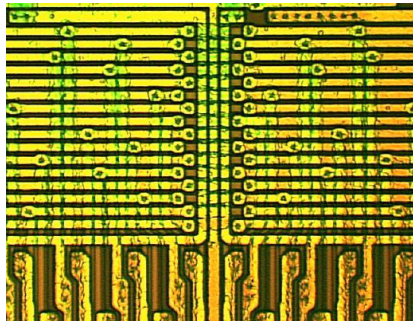
Radiation suppression with a ferromagnetic film

Ferromagnetic material $\text{Ni}_{80}\text{Fe}_{20}$, aka Permalloy.
Experiment with a layer of $20\text{ }\mu\text{m}$ depth [BBD⁺07].



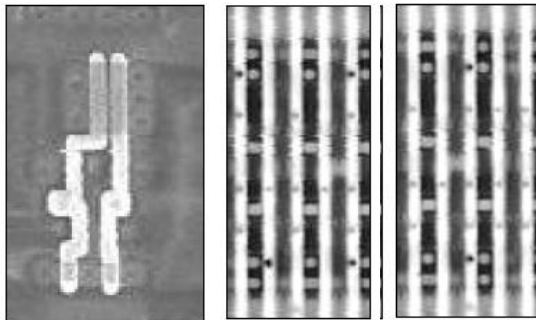
Bus scrambling

- Scrambling can be static or dynamic.
- Static scrambling can also be a feature
 - The mixing comes from a problem of routability of the data/address bus to the memory.
 - Possible because permutations affect equally the write and read operations.



Beware of attacks [FLM10] on scrambled EEPROMs!

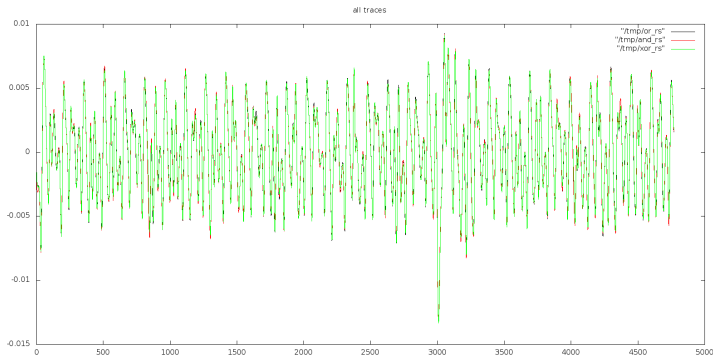
Hardware Camo



Hardware-level camouflage of gates. Left: an unprotected gate, whose function is easy to identify. Center, right: *almost* indistinguishable AND/OR camouflaged gates. [courtesy of SMI / SypherMedia Library]

Software Camo

ARM7 Native Machine Code



Traces of the electromagnetic leakage of the AND, XOR and OR

- [BBD⁺07] L. Bouhouch, A. Boyer, S. Ben Dhia, É. Sicard, and M. Fadel.
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Evaluation of White-Box and Grey-Box Noekeon Implementations in FPGA.
In Viktor K. Prasanna, Jürgen Becker, and René Cumplido, editors, *ReConFig*, pages 310–315. IEEE Computer Society, 2010.

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Memory Address Scrambling Revealed Using Fault Attacks.
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Attaques de cryptosystèmes embarqués et contre-mesures associées.
PhD thesis, Université de Versailles Saint-Quentin-en-Yvelines, 26 octobre 2007.
<http://www.prism.uvsq.fr/fileadmin/CRYPTO/TheseCG-new.pdf>.
- [GMN⁺13] Sylvain Guilley, Damien Marion, Zakaria Najm, Youssef Souissi, and Antoine Wurcker.
Software Camouflage.
In *FPS*, volume 8352 of *LNCS*. Springer, October, 21–22 2013.
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