Dr. Sumanta Chaudhuri

Education

2004- 2009 • `PhD.Thesis "Asynchronous FPGA Architectures for Cryptographic Applications".`
Ecole Nationale Supérieure des Télécommunications(ENST), Paris, FRANCE

1996- 2000 • `Bachelor of Technology in Electronics and communication Engineering`
National Institute of Technology(NIT), Warangal, INDIA

Employment

2014- Present • `Lecturer`
Institut Mines-Telecom, FRANCE

2012- 2014 • `Leading Design Engineer`
Imagination Technologies, UK
- Performance Analysis of SoC Interconnect & DDR Intreface.
- Transaction Level Modelling & verification of performance for two Multimedia SoCs.

2010- 2012 • `Research Associate`
Imperial College, London, UK
- Process Variation Aware Design for FPGAs.
- Variation-Aware P&R & Retiming Algorithm Development (11; 10; 8; 9; 6; 7)
- Benchmarking and Architecture Exploration using HPC grid.

2008- 2010 • `Research Associate`
Université Paris Sud, FRANCE
- Project NANO2012 in collaboration with ST-Microelectronics
- Development of Embedded MRAM Macros for Memory-in-Logic Application
- 3D integration of MRAM and CMOS(130nm) Designs.

2006- 2008 • `Research Assistant`
CNRS, Paris, FRANCE
- Project SAFE in Collaboration with TIMA, Greonble.
- Software development for FPGA P/R, layout generation, synthesis(C/C++) (13)
- VLSI & SoC Design(Simulation,P&R,DRC,LVS Timing Analysis with Cadence/Mentor tools)
- Automatic layout generation for FPGAs (17), Asynchronous FPGA Architectures for Secure Applications , Future Interconnect Strategies (15), FPGA Architectures for Run-Time Reconfigurability (14), Theory of Interconnects.

2000- 2004 • `Hardware Engineer`
Center for Development of Telematics(CDOT), Bangalore, INDIA
Software Development on TMS320 DSP Processors(C/Assembly) & Firmware Development (ALTERA) for a controller of 3G feedforward Amplifiers.
Hardware Development of Digital-RF Boards using Mentor Graphics BoardStation.

R&D Record

- One patent, Four journal Publications and Eight Peer Reviewed Conference Publications in FPL,FPGA,FPT,DAC.
- Two Completed Tape-Outs of FPGA Prototypes in 130nm, 65nm.
- One completed Tape-out of embedded MRAM in MTJ-CMOS hybrid technology.
- Reviewer of Microelectronics Journal(Elsevier), ACM TRETS, FPGA Conferences.
- Open source Software Development VPR. (8; 13; 17)
- Open source Hardware Development Opencores.

List of Tape-Outs

[1] Sumanta Chaudhuri,Jacques-Olivier Klein, Claude Chappert, "CILIOMAG-IEF(CMOS 130 nm, MTJ 120nm), Z80 Processor with Embedded MRAM," September 2009, CMP(Circuits Multi-Projets) S13C09_4 with ST Microelectronics and SPINTEC, France.

[2] Sumanta Chaudhuri, Taha Beyrouthy, and Sylvain Guilley, "**SAFE(65 nm), A Prototype Asynchronous FPGA for Secure Applications**," February 2008, CMP(Circuits Multi-Projets) S65C8_1 with ST Microelectronics, France.

[3] Sumanta Chaudhuri, Florent Flament, Sylvain Guilley, "**SECMAT V3(130 nm), An RTR FPGA embedded in a SoC for Cryptographic Applications**," January 2007, CMP(Circuits Multi-Projets) SI2C7_1 with ST Microelectronics, France.

Selected Publications

Journal

[4] W. Zhao, S. Chaudhuri, C. Accoto, J.-O. Klein, C. Chappert, and P. Mazoyer, "Cross-point architecture for spin-transfer torque magnetic random access memory," *Nanotechnology, IEEE Transactions on*, vol. 11, no. 5, pp. 907–917, 2012.

[5] S. Guilley, S. Chaudhuri, L. Sauvage, P. Hoogvorst, R. Pacalet, and G. M. Bertoni, "Security Evaluation of WDDL and SecLib Countermeasures against Power Attacks," in *IEEE Transactions on Computers*, vol. 57, no. 11, Nov. 2008.

[6] Z. Guan, J. S. Wong, S. Chaudhuri, G. A. Constantinides, and P. Y. K. Cheung, "Classification on variation maps : a new placement strategy to alleviate process variation on FPGA," *IEICE Electronic Express*, vol. 11, no. 3, p. 20130912, 2014. [Online]. Available : http://dx.doi.org/10.1587/elex.10.20130912

[7] ——, "Mitigation of process variation effect in fpgas with partial rerouting method," *IEICE Electronic Express*, vol. 11, no. 3, p. 20140011, 2014. [Online]. Available : http://dx.doi.org/10.1587/elex.11.20140011

Conferences

[8] Z. Guan, J. S. Wong, S. Chaudhuri, G. A. Constantinides, and P. Y. K. Cheung, "**A two-stage variation-aware placement method for FPGAS exploiting variation maps classification**," in *FPL*, 2012, pp. 519–522.

[9] S. Chaudhuri, J. S. J. Wong, and P. Y. K. Cheung, "**Timing Speculation in FPGAs : Probabilistic Inference of Data Dependent Failure Rates**," in *ICFPT*, Dec 2011, New Delhi, India.

[10] Z. Guan, J. S. Wong, S. Chaudhuri, G. A. Constantinides, and P. Y. K. Cheung, "**A Variation-adaptive Retiming Method Exploiting Reconfigurability**," in *FPL*, 2013.

[11] ——, "**Exploiting Stochastic Delay Variability on FPGAs with Adaptive Partial Rerouting**," in *ICFPT*, 2013.

[12] S. Chaudhuri, W. Zhao, J.-O. Klein, C. Chappert, and P. Mazoyer, "**High-Density Asynchronous LUT based on Non-Volatile MRAM Technology**," in *FPL*, Sept 2010, Milan, Italy.

[13] S. Chaudhuri, "**Diagonal Tracks in FPGAs : A Performance Evaluation**," in *FPGA*, USA, Feb 2009.

[14] S. Chaudhuri, S. guilley, F. Flament, P. Hoogvorst, and J.-L. Danger, "**An 8x8 Run-Time Reconfigurable FPGA Embedded in a SoC**," in *DAC*, Anaheim, California USA, June 2008.

[15] S. Chaudhuri, J.-L. Danger, P. Hoogvorst, and S. Guilley, "**Efficient Tiling Patterns for Reconfigurable Gate Arrays (Extended Abstract in FPGA 2008)**," in *SLIP*, Newcastle,UK, April 2008, pp. 11–18.

[16] S. Chaudhuri, S. Guilley, P. Hoogvorst, J.-L. Danger, T. Beyrouthy, A. Razafindraibe, L. Fesquet, and M. Renaudin, "Physical Design of FPGA Interconnect to Prevent Information Leakage," in *ARC*, March 2008, london,UK.

[17] S. Chaudhuri, J.-L. Danger, and S. Guilley, "**Efficient Modeling and Floorplanning of Embedded-FPGA Fabric**," in *FPL*, Aug 2007, pp. 665–669, Amsterdam, Netherlands.

[18] T. Beyrouthy, A. Razafindraibe, L. Fesquet, M. Renaudin, S. Chaudhuri, S. Guilley, P. Hoogvorst, and J.-L. Danger, "A Novel Asynchronous e-FPGA Architecture for Security Applications," in *ICFPT*, 2007, pp. 15–22, kokurakita, Kitakyushu, JAPAN.

Patents

[19] S. Chaudhuri, W. Zhao, J.-O. Klein, C. Chappert, and P. Mazoyer, "(WO2012168591) Logical Memory Architecture, in particular for MRAM, PCRAM, or RRAM," Pub. No. :WO/2012/16859, International Application No. :PCT/FR2012/050617, Publication Date :13.12.2012, http://patentscope.wipo.int/search/en/WO2012168591.