Analysis of timing anomalies in multi-core real-time systems

Topic	formal methods, micro-architecture, critical systems
Duration	2×1 year
Cities and country	Palaiseau (LTCI) & Nantes (LS2N), France
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General presentation of the topic This position is part of the CAOTIC collaborative project. It is funded by the French National Research Agency (ANR). CAOTIC brings together a number of research groups working in the area of timing analysis and verification of critical embedded systems. The aim of the project is to develop new techniques for the verification of real-time constraints in multi-core and heterogeneous embedded architectures.

Timing analysis of multi-core platforms is more difficult than that of single core platforms due to the presence of timing interference. Timing interference occurs when two activities conflict to access a shared hardware resource (cache, interconnect, memory banks, etc.) resulting in a delay for one of the activities. To verify the timing behavior of a program on a multi-core architecture, it is necessary to exhaustively identify the interference channels present at the hardware architecture level. It is then necessary to determine the effect of the interference passing through these channels on the timing behavior of the program of interest. In some systems, this problem is made more difficult by the possible presence of timing anomalies: either counter-intuitive behaviors (a local acceleration leads to a global slowdown), or amplification (a local slowdown leads to a much larger global slowdown).

The context of this position is the timing verification of programs in the presence of timing interference and timing anomalies.

Scope of the work The person recruited will work on two topics. In the first year, the work will focus on the study of the memory hierarchy of heterogeneous multi-core embedded architectures. The aim of this study will be to identify the channels, explicit or implicit, through which a system activity can interfere with the execution of a program on one of the cores, typically by delaying a memory access. A memory hierarchy representative of the target systems includes parallelism and non-preemptive activities, two elements that are known to lead to the appearance of timing anomalies. Thus, the study will also investigate the existence of timing anomalies in the memory hierarchy. Finally, the two phenomena, interference and timing anomalies, will have to be characterized. Ideally, an operational procedure for detecting their occurrence will be formalized and applied to realistic system models.

In the second year, work will focus on developing analysis techniques to compute a safe upper bound on the maximum duration of an execution trace in the presence of interference, when the micro-architecture is likely to produce timing anomalies. The presence of timing anomalies invalidates approaches based on adding a constant interference cost equal to the induced delay. It is then necessary to consider a set of scenarios that are sufficiently complete to ensure that the worst case is included. The work will involve identifying this set of scenarios and proposing a symbolic enumeration technique that can be scaled up to compute the upper bound.

Job Profile This position is aimed at young researchers with a PhD in Computer Science or Computer Engineering and experience in some of the following areas

- Timing analysis of computer systems: WCET, cache analysis, etc;

- Formal methods, in particular model checking;
- Hardware architecture, especially micro-architecture.

Application Applications are welcome online via a job advertisement of Télécom Paris:
`https://institutminestelecom.recruitee.com/o/post-doctorante-ou-post-doctorant-in-timing-anomalies-in-multicore-systems.`

Relevant candidates will be interviewed by several project partners. The contract will be limited to one year initially, with a possibility for a renewal for a second year. The project partners are located in Palaiseau (Paris region) and Nantes. Candidates may thus chose to work either in Palaiseau or Nantes.