

# FLORIAN BRANDNER

## PERSONAL DATA

*born* 23 - 09 - 1980, Erlenbach am Main, Germany  
*www* <https://perso.telecom-paris.fr/brandner/>  
*email* [florian.brandner@telecom-paris.fr](mailto:florian.brandner@telecom-paris.fr)  
*phone* +33 (0)1 75 31 97 74

## WORK EXPERIENCE

*Télécom Paris* **Current** Associate Professor, Paris, FR  
Associate Professor (maître de conférences) in the ACES team (formally S3) of the LTCI laboratory at Télécom Paris (formally Télécom ParisTech), which is part of the Institut Polytechnique de Paris (IP Paris) and the Institut Mines-Télécom (IMT).

*ENSTA ParisTech* 09/2013 Assistant Professor, Palaiseau, FR  
08/2015 Assistant Professor (enseignant-chercheur) at the Computer Science and Systems Engineering Department of ENSTA ParisTech (École Nationale Supérieure de Techniques Avancées).

*DTU Compute* 11/2011 Post-doctoral Researcher, Copenhagen, DK  
09/2013 Post-doctoral researcher at the Embedded Systems Engineering Section of DTU Compute (Danmarks Tekniske Universitet). Funded by the European project T-CREST.

*INRIA Grenoble* 10/2009 Post-doctoral Researcher, Lyon, France  
10/2011 Post-doctoral researcher at the Laboratoire de l'Informatique du Parallélisme (LIP) at the École Normale Supérieure de Lyon (ENS de Lyon) Funded by INRIA and the Mediacom project as part of Nano2012.

*MSR Redmond* 04/2009 Microsoft Research, Redmond, WA, USA  
07/2009 Research Internship at Microsoft Research on just-in-time code generation for the fast JavaScript engine *SPUR*.

*CD-Laboratory  
Phd* 10/2005 Research Assistant, Vienna, Austria  
02/2009 Research on retargetable compiler components, compiler optimizations and processor description languages in the Christian Doppler Laboratory – Compilation Techniques for Embedded Processors. In part funded by ONDEMAND Microelectronics and the Christian Doppler Forschungsgesellschaft.

- 03/2004  
10/2004  
*StarCore LLC.* Compiler-Developer, Vienna, Austria  
In 2004 *StarCore* (now *LSI LOGIC*) established a branch in Vienna. I joined *StarCore* to develop high-level and low-level optimizations for a new compiler targeting the *StarCore SC1x00* family DSPs.
- 01/2004  
02/2004  
*Atair GmbH.* Software-Developer, Vienna, Austria  
Development of a processor description language for the Open Compiler Environment (OCE) by *Atair*.
- 2002  
2005  
*Vienna University of Technology* Teaching Assistant, Vienna, Austria  
Teaching Assistant at the Languages Group of the Institute of Computer Languages, the Distributed Systems Laboratory of the Institute of Information Systems, and the Database and Artificial Intelligence Group of the Institute of Information Systems.

## EDUCATION

- 10/2005  
12/2009  
*PhD* Vienna University of Technology, Austria  
*PhD* PhD student of Computer Science at the Vienna University of Technology. The final Rigorosum (defense) was held in Vienna on December 18th, 2009.  
Thesis: Compiler Backend Generation from Structural Processor Models  
Jury members: Jens Knoop, Andreas Krall, Tomáš Hruška  
Adviser: Andreas Krall
- 09/1999  
10/2004  
*Dipl. Ing. Master* Vienna University of Technology, Austria  
*Dipl. Ing. Master* Student of Computer Science at the Vienna University of Technology. Graduated with honors in 2004.  
Thesis: Instruction set simulation  
Adviser: Andreas Krall
- 06/2003  
01/2004  
*Exchange* Technical University of Denmark, Lyngby  
*Exchange* Exchange student at the DTU in Lyngby close to Copenhagen, Denmark.
- 09/1991  
06/1999  
*School* BG/BRG Bruck an der Mur, Austria  
*School* Secondary School.

## ADDITIONAL INFORMATION

- Languages* ENGLISH · Fluent  
FRENCH · Fluent  
GERMAN · Mother Tongue  
DANISH · Reading

## BOOK CHAPTERS

## DSP Instruction Set Simulation

**Florian Brandner**, Nigel Horspool, and Andreas Krall  
 Handbook of Signal Processing Systems (2nd Edition)  
 S.S. Bhattacharyya, E.F. Deprettere, R. Leupers, and J. Takala (Editors)  
 2013, Springer

## DSP Instruction Set Simulation

**Florian Brandner**, Nigel Horspool, and Andreas Krall  
 Handbook of Signal Processing Systems  
 S.S. Bhattacharyya, E.F. Deprettere, R. Leupers, and J. Takala (Editors)  
 2010, Springer

## PROCEEDINGS

 Proceedings of the 18th International Workshop on Worst-Case  
 Execution Time Analysis

**Florian Brandner**  
 Barcelona, Spain, 2018  
 OASiCs Dagstuhl

 Proceedings of the 11th Workshop on Optimizations for DSP and  
 Embedded Systems

**Florian Brandner** and Tom Vander Aa (Editors)  
 Orlando, FL, USA, 2014  
 ACM ICPS

 Proceedings of the 10th Workshop on Optimizations for DSP and  
 Embedded Systems

**Florian Brandner** and Tom Vander Aa (Editors)  
 Shenzhen, China, 2013  
 ACM ICPS

## JOURNAL PUBLICATIONS

## Precise, Efficient, and Context-Sensitive Cache Analysis

**Florian Brandner**  
 Real-Time Systems (TIME)  
 to appear, 2021, Springer

 Work-Conserving Dynamic Time-Division Multiplexing for  
 Multi-Criticality Systems

Farouk Hebbache, **Florian Brandner**, Mathieu Jan, and Laurent Pautet  
 Real-Time Systems (TIME)  
 Volume 56(2): 124–170 (2020), Springer

## Analysis of Preemption Costs for the Stack Cache

Amine Naji, Sahar Abbaspour, **Florian Brandner**, and Mathieu Jan  
 Real-Time Systems (TIME)  
 Volume 54(3): 700–744 (2018), Springer

## Studying Optimal Spilling in the Light of SSA

**Florian Brandner**, **Florian Brandner**, and Alain Darté  
 ACM Transactions on Architecture and Code Optimization (TACO)  
 Volume 11(4): (2015), ACM

## Refinement of Worst-Case Execution Time Bounds by Graph Pruning

**Florian Brandner** and Alexander Jordan  
 Computer Languages, Systems & Structures (COMLAN)  
 Volume 40(3-4): 155–170 (2014), Elsevier

### Criticality: Static Profiling for Real-Time Programs

**Florian Brandner**, Stefan Hepp, and Alexander Jordan

Real-Time Systems (TIME)

Volume 50(3): 377-410 (2014), Springer

### Elimination of Parallel Copies using Code Motion on Data Dependence Graphs

**Florian Brandner** and Quentin Colombet

Computer Languages, Systems & Structures (COMLAN)

Volume 39(1): 25-47 (2013), Elsevier

### Automatic Generation of Compiler Backends

**Florian Brandner**, Viktor Pavlu, and Andreas Krall

Software: Practice and Experience (SPE)

Volume 43(2): 207-240 (2013), Wiley

## CONFERENCE PUBLICATIONS

### Is This Still Normal? Putting Definitions of Timing Anomalies to the Test

Benjamin Binder, Mihail Asavoae, Belgacem Ben Hedia, **Florian Brandner**, and Mathieu Jan

International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)

to appear, online, IEEE

### Scalable Detection of Amplification Timing Anomalies for the Superscalar TriCore Architecture

Benjamin Binder, Mihail Asavoae, **Florian Brandner**, Belgacem Ben Hedia, and Mathieu Jan

International Conference on Formal Methods for Industrial Critical Systems (FMICS)

Vienna, Austria, 2020, Springer

### Precise and Efficient Analysis of Context-Sensitive Cache Conflict Sets

**Florian Brandner**

28th International Conference on Real-Time and Network Systems (RTNS)

Paris, France, 2020, ACM ICPS

*Best Paper Award*

### Arbitration-Induced Preemption Delays

Farouk Hebbache, **Florian Brandner**, Mathieu Jan, and Laurent Pautet

Euromicro Conference on Real-Time Systems (ECRTS)

Stuttgart, Germany, 2019, LIPIcs Dagstuhl

### Shedding the Shackles of Time-Division Multiplexing

Farouk Hebbache, Mathieu Jan, **Florian Brandner**, and Laurent Pautet

Real-Time Systems Symposium (RTSS)

Nashville, USA, 2018, IEEE

*Outstanding  
Paper Award*

### Experimental Energy Profiling of Energy-Critical Embedded Applications

Kameswar Rao Vaddina, **Florian Brandner**, Gerard Memmi, and Pierre Jouvelot

Symposium on Green Networking and Computing (SGNC) part of SoftCOM 2017

Split, Croatia, 2017, IEEE

*Best Paper Award*

### Efficient Context Switching for the Stack Cache: Implementation and Analysis

Sahar Abbaspour, **Florian Brandner**, Amine Naji, and Mathieu Jan

23th International Conference on Real-Time and Network Systems (RTNS)

Lille, France, 2015, ACM ICPS

*Outstanding  
Paper Award*

### Splitting Functions into Single-Entry Regions

Stefan Hepp and **Florian Brandner**

International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)

New Delhi, India, 2014, ACM

## A Loosely Synchronizing Asynchronous Router for TDM-Scheduled NOCs

Ioannis Kotleas, Dean Humphreys, Rasmus Bo Sørensen, Evangelia Kasapaki, **Florian Brandner**, and Jens Sparsø  
International Symposium on Networks-on-Chip (NOCS)  
Ferrara, Italy, 2014, IEEE

## Static Analysis of Worst-Case Stack Cache Behavior

Alexander Jordan, **Florian Brandner**, and Martin Schoeberl  
International Conference on Real-Time and Network Systems (RTNS)  
2013, Sophia-Antipolis, France, ACM ICPS

*Best Paper Award*

## Static Profiling of the Worst-Case in Real-Time Programs

**Florian Brandner**, Stefan Hepp, and Alexander Jordan  
International Conference on Real-Time and Network Systems (RTNS)  
2012, Pont à Mousson, France, ACM ICPS

## Static Routing in Symmetric Real-Time Network-on-Chips

**Florian Brandner** and Martin Schoeberl  
International Conference on Real-Time and Network Systems (RTNS)  
2012, Pont à Mousson, France, ACM ICPS

## A Statically-Scheduled Time-Division-Multiplexed Network-on-Chip for Real-Time Systems

Martin Schoeberl, **Florian Brandner**, Evangelia Kasapaki, and Jens Sparsø  
Symposium on Networks-on-Chip (NOCS)  
2012, Kongens Lyngby, Denmark, ACM/IEEE

## Copy Elimination on Data Dependence Graphs

**Florian Brandner** and Quentin Colombet  
Symposium On Applied Computing (SAC-PL)  
2012, Riva del Garda, Italy, ACM

## A Non-Iterative Data-Flow Algorithm for Computing Liveness Sets in Strict SSA Programs

Benoît Boissinot, **Florian Brandner**, Alain Darte, Benoît Dupont de Dinechin, and Fabrice Rastello  
Symposium on Programming Languages and Systems (APLAS)  
2011, Kenting, Taiwan, Springer

## Studying Optimal Spilling in the Light of SSA

Quentin Colombet, **Florian Brandner**, and Alain Darte  
Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)  
2011, Taipei, Taiwan, ACM

## Execution Models for Processors and Instructions

**Florian Brandner**, Viktor Pavlu, and Andreas Krall  
28th Norchip Conference  
2010, Tampere, Finland, IEEE

## SPUR: A Trace-Based JIT Compiler for CIL

Michael Bebenita, **Florian Brandner**, Manuel Fahndrich, Francesco Logozzo, Wolfram Schulte, Nikolai Tillmann, and Herman Venter  
International Conference on Object Oriented Programming Systems Languages and Applications (OOPSLA)  
2010, Reno, USA, ACM

## Completeness of Automatically Generated Instruction Selectors

**Florian Brandner**  
21st International Conference on Application-specific Systems, Architectures and Processors (ASAP)  
2010, Rennes, France, IEEE

### RTTM: Real-Time Transactional Memory

Martin Schoeberl, **Florian Brandner**, and Jan Vitek

25th Symposium On Applied Computing, Real Time Systems Track, (SAC)

2010, Sierre, Switzerland, ACM

### Stack Allocation of Objects in the Cacao Virtual Machine

Peter Molnar, Andreas Krall, and **Florian Brandner**

7th International Conference on the Principles and Practice of Programming in Java (PPPJ)

2009, Calgary, Canada, ACM

### Embedded JIT Compilation with CACAO on YARI

**Florian Brandner**, Martin Schoeberl, and Tommy Thorn

12th IEEE International Symposium on Object/component/service-oriented Real-time distributed Computing (ISORC)

2009, Tokyo, Japan, IEEE

### Generalized Instruction Selection using SSA-Graphs

Dietmar Ebner, **Florian Brandner**, Bernhard Scholz, Andreas Krall, Peter Wiedermann, and Albrecht Kadlec

ACM Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)

2008, Tucson, USA, ACM

### Compiler Generation from Structural Architecture Descriptions

**Florian Brandner**, Dietmar Ebner, and Andreas Krall

International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)

2007, Salzburg, Austria, ACM

### Effective Compiler Generation by Architecture Description

Stefan Farfeleder, Andreas Krall, Edwin Steiner, and **Florian Brandner**

ACM Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)

2006, Ottawa, Canada, ACM

## WORKSHOP PUBLICATIONS

### Dynamic Arbitration of Memory Requests with TDM-like Guarantees

Farouk Hebbache, Mathieu Jan, **Florian Brandner**, and Laurent Pautet

Workshop on Compositional Theory and Technology for Real-Time Embedded Systems (CRTS)

Paris, France, 2017

### Worst-Case Execution Time Analysis of Predicated Architectures

**Florian Brandner** and Amine Naji

Workshop on Worst-Case Execution Time Analysis (WCET)

Dubrovnik, Croatia, 2017, OASICs Dagstuhl

### Eager Stack Cache Memory Transfers

Amine Naji and **Florian Brandner**

Workshop on Worst-Case Execution Time Analysis (WCET)

Toulouse, France, 2016, OASICs Dagstuhl

### A Comparative Study of the Precision of Stack Cache Occupancy Analyses

Amine Naji and **Florian Brandner**

Junior Researcher Workshop on Real-Time Computing (JRWRTC)

Lille, France, 2015

### Alignment of Memory Transfers of a Time-Predictable Stack Cache

Sahar Abbaspour and **Florian Brandner**

Junior Researcher Workshop on Real-Time Computing (JRWRTC)

Versailles, France, 2014

## Lazy Spilling for a Time-Predictable Stack Cache: Implementation and Analysis

Sahar Abbaspour, Alexander Jordan, and **Florian Brandner**  
Workshop on Worst-Case Execution Time Analysis (WCET)  
Madrid, Spain, 2014, OASIS Dagstuhl

## A Time-predictable Stack Cache

Sahar Abbaspour, **Florian Brandner**, and Martin Schoeberl  
Workshop on Software Technologies for Embedded and Ubiquitous Systems (SEUS)  
2013, Paderborn, Germany

## Studying Spilling in the Light of SSA

Quentin Colombet, **Florian Brandner**, and Alain Darté  
Workshop on Compilers for Parallel Computing (CPC)  
2012, Padua, Italy

## Modeling Application-Specific Processors for Cyber-Physical Systems

**Florian Brandner**, Viktor Pavlu, and Andreas Krall  
Workshop on Software Language Engineering for Cyber-physical Systems (WS4C)  
2011, Berlin, Germany (LNI)

## Compiler-driven Optimization of the Worst-Case Execution Time

**Florian Brandner** and Alain Darté  
Workshop Analyse to Compile, Compile to Analyse (ACCA)  
2011, Chamonix, France

## Towards a Time-predictable Dual-Issue Microprocessor: The Patmos Approach

Martin Schoeberl, Pascal Schleuniger, Wolfgang Puffitsch, **Florian Brandner**,  
Christian W. Probst, Sven Karlsson, and Tommy Thorn  
Workshop on Practice, Predictability and Performance in Embedded Systems (PPES)  
2011, Grenoble, France

## Automatic Tool Generation from Structural Processor Descriptions

**Florian Brandner**  
15th Biennial Workshop on Programmiersprachen und Grundlagen der  
Programmierung (KPS)  
2009, Maria Taferl, Austria

## Precise Simulation of Interrupts using a Rollback Mechanism

**Florian Brandner**  
12th International Workshop on Software and Compilers for Embedded Systems  
(SCOPES)  
2009, Nice, France

## Completeness of Instruction Selector Specifications with Dynamic Checks

**Florian Brandner**  
8th International Workshop on Compiler Optimization Meets Compiler Verification  
(COCV)  
2009, York, England

## Fast and Accurate Simulation using the LLVM Compiler Framework

**Florian Brandner**, Andreas Fellnhöfer, Andreas Krall, and David Riegler  
1st Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools  
(RAPIDO)  
2009, Paphos, Cyprus

## Leveraging Predicated Execution for Multimedia Processing

Dietmar Ebner, **Florian Brandner**, and Andreas Krall  
Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia)  
2007, Salzburg, Austria

Static Verification of Global Heap References in Java Native Libraries  
 Andreas Krall, Christian Thalinger, Dietmar Ebner, and **Florian Brandner**  
 Workshop on Semantics, Program Analysis, and Computing Environments for  
 Memory Management (SPACE)  
 2006, Charleston, USA

#### TECHNICAL REPORTS

Subgraph-Based Refinement of Worst-Case Execution Time Bounds  
**Florian Brandner** and Alexander Jordan  
 ENSTA Technical Report, hal-00978015  
 Palaiseau, France, April 2014

Parallel Copy Elimination on Data Dependence Graphs  
**Florian Brandner**, Quentin Colombet  
 INRIA Technical Report RR-7535  
 Lyon, France, September 2011

Computing Liveness Sets for SSA-Form Programs  
**Florian Brandner**, Benoit Boissinot, Alain Darte, Benoît Dupont de Dinechin, Fabrice Rastello  
 INRIA Technical Report RR-7503  
 Lyon, France, January 2011

SPUR: A Trace-Based JIT Compiler for CIL  
 Michael Bebenita, **Florian Brandner**, Manuel Fahndrich, Francesco Logozzo,  
 Wolfram Schulte, Nikolai Tillmann, and Herman Venter  
 Technical Report MSR-TR-2010-27  
 Microsoft Research  
 Redmond, USA, March 2010

Embedded JIT Compilation with CACAO on YARI  
**Florian Brandner**, Tommy Thorn, and Martin Schoeberl  
 Technical Report RR 35/2008  
 Institute of Computer Engineering  
 Vienna University of Technology  
 Vienna, Austria, June 2008

#### PROJECT REPORTS

D2.1 Software Simulator of Patmos  
**Florian Brandner**  
 T-CREST project report  
 Kongens Lyngby, Denmark, March, 2012

D5.2 Initial Compiler Version  
**Florian Brandner**, Stefan Hepp, and Daniel Prokesch  
 T-CREST project report  
 Vienna, Austria, September, 2012

#### THESES

Compiler Backend Generation from Structural Processor Models  
**Florian Brandner**  
 PhD Thesis  
 2009, Vienna University of Technology, Vienna, Austria

Instruction Set Simulation  
**Florian Brandner**  
 Diploma/Masters Thesis  
 2004, Vienna University of Technology, Vienna, Austria

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