Cycle-Accurate Virtual Prototyping with Multiplicity

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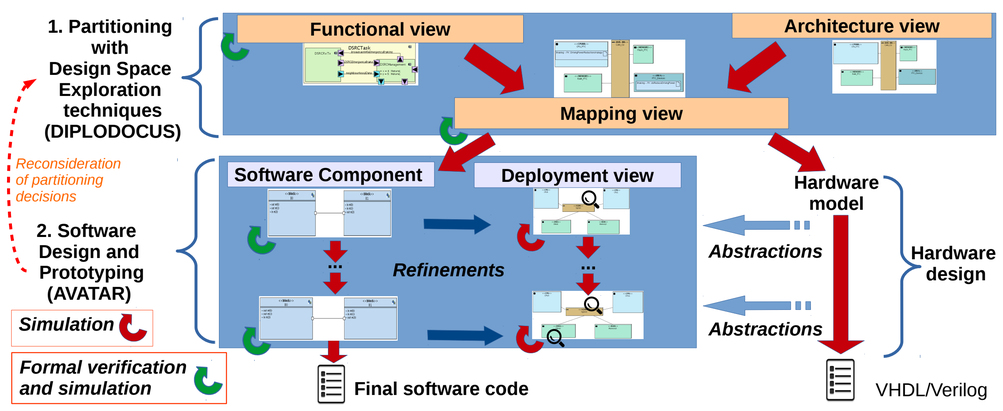
Aims

- Efficiently represent applications with many tasks and channels within SysML block diagrams
- Efficient allocation of these tasks and channels to multi-processor embedded hardware
  Non Uniform Memory Access (NUMA) architecture
- Hardware + tasks → cycle-accurate virtual prototype
- Explore diverse alternatives for optimal task deployment:
  Design Space Exploration

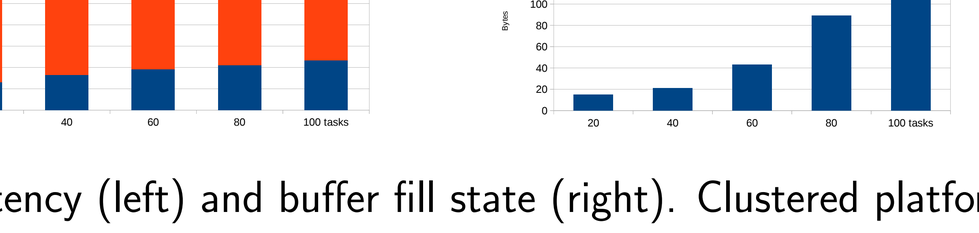
Methodology



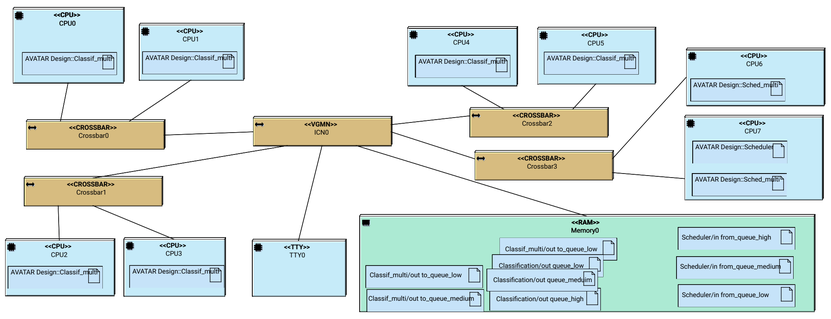
- Partitioning: SysML like model, allocation decisions
- Software Design: block diagrams, state machine diagrams
- Deployment on virtual prototype, simulation and cycle precise performance evaluation using TTool [1]

Case Study: Network Classification Application

- Classification tasks: read descriptors, retrieve first chunk of corresponding packet from memory, determine priority
- Scheduling tasks: read descriptors from priority queuesn reconstitute packets and write them to output queue



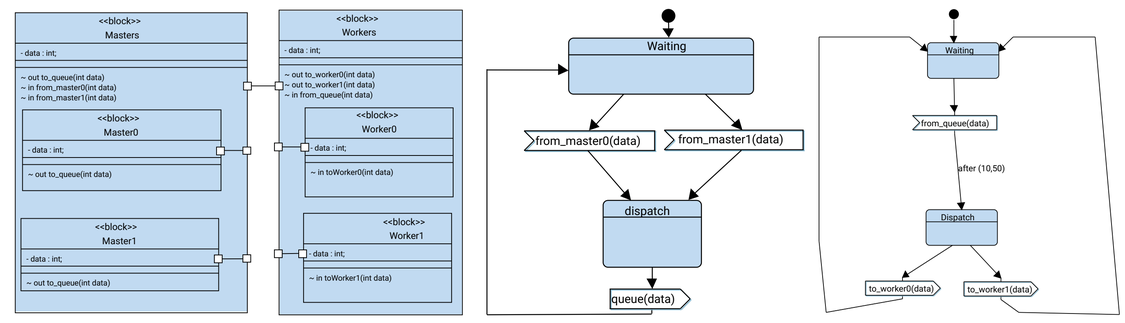
Mapping on Clustered Platform



Experimental Results

- Latency (left) and buffer fill state (right). Clustered platform, 8 MIPS32 processors, 6 classification and 2 scheduling tasks

Master-Worker Paradigm

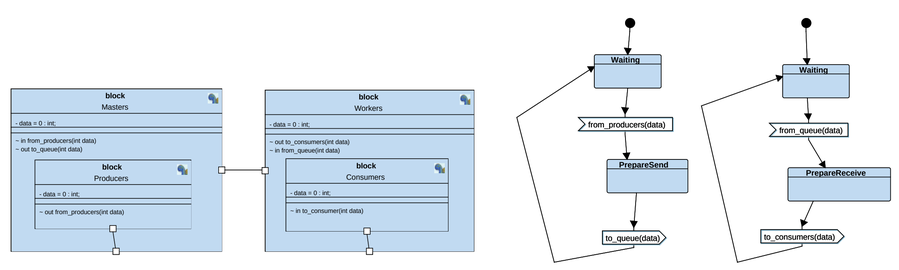


- Typical embedded applications: one-to-one communications
- High-performance streaming applications: massive task parallelism with many-to-many communications

Extensions to SysML Block Diagrams

- Introduce a new parameter to duplicate tasks instances
- Communication semantics: shared, point to point, multicast

Master-Worker Paradigm with Multiplicity



- One block to model multiple masters, multiple workers

Conclusions

- Design space exploration for task farm type applications on NUMA architectures is significantly facilitated
- Detailed virtual prototype is generated, making it particularly well adapted for fine grain performance analysis and tuning
- Task farm applications fully exploit the potential of multi writer multi reader channels [2]

Perspectives

- Specification of individual state machines for multiple blocks is still time-consuming: develop communications schemes similar to the Psi-Chart [3]
- Integration of transaction-level and QEMU-based virtual platforms for faster simulation
- Extension to analog/mixed signal systems [4]

Bibliography

[1] Apvrille, L. TTool, an open-source toolkit for the modeling and verification of embedded systems. http://ttool.telecom-paris.fr

[2] Genius, D., Apvrille, L., and Li, L. W. High-level modeling of communication-centric applications: Extensions to a system-level design and virtual prototyping tool. Microprocessors and Microsystems, vol 67:117–130, 2019

[3] Enrici, A., Apvrille, L., and Pacalet, R. A model-driven engineering methodology to design parallel and distributed embedded systems. ACM Trans. Design Automation of Electronic Syst., 22(2):34:1–34:25, 2017

[4] Cortés Porto, R. et al., Handling causality and schedulability when designing and prototyping cyber-physical systems. Software and Systems Modeling, Springer, 2021