PhD Proposal
Digital and analog twin for complex CPS

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1 Context

Model-based design methods have proven successful for both embedded and cyber-physical systems (CPS) [SG13, FE98]. Designing such systems usually starts with a hardware-independent model that can be verified against its specifications to ensure that functional requirements are met. However, non-functional requirements such as performance, power consumption, and security cannot yet be addressed at this level, since these properties depend on the implementation and in particular on the hardware/software partitioning. Moreover, it is usually necessary to use mechanisms specialized for the different requirements, of instance security mechanisms have to be used to handle used to handle security requirements. Yet, introducing such mechanisms my also fulfill other requirements (e.g. safety requirements), but may also negatively impact other requirements, such as performance requirements.

Within the *Modeling and Verification for Secure and Performant CPS* (MoVe4SPS) ANR project which finances the thesis, we intend to address the inter-relations between security and performance aspects during the life cycle of CPS. To do so, we intend to rely on **digital twins**, allowing continuous feedback and system adaptation, representing a high-level view and allowing formal verification on the one hand, and of **runtime monitors** which are expected to log data related to performance aspects on the other.

Once system has been designed, it can be verified, e.g. using formal verification or simulation, for instance using a virtual prototype. Then, the system is put into operation. When runtime errors are detected thanks to probes, the execution traces can be fed back to design models, and a patch is subsequently produced and deployed. Figure 1 presents the project's approach, featuring this digital twin paradigm.

TTool [Apv23] is a a SysML-based, free and open-source tool for modeling and formally verifying embedded systems. Models and verification are performed at multiple levels of abstraction, from system-level to cycle-accurate. TTool can generate cycle-accurate virtual prototypes based on SystemC components available in the SoCLib library [con03]. This library contains bit and cycle accurate model of these hardware components, for instance latencies, cache misses, power consumption, etc.. In a recent extension named TTool-AMS, digital virtual prototypes are combined with analog virtual prototypes by generating SystemC-AMS [BEG+16] code, which is simulated together with the SystemC code of the digital part; handling scheduling and causality between the digital and analog part is a challenge we successfully tackled in [CGA21]: this opens the door to defining digital/analog twins.

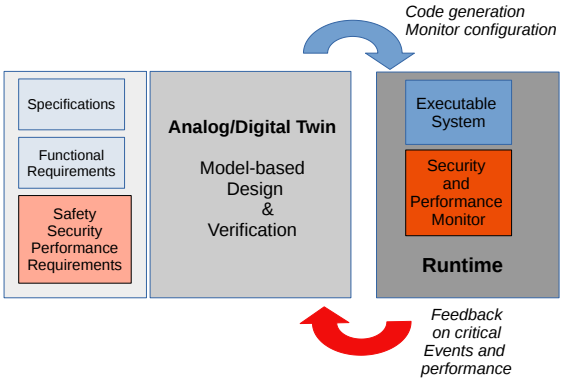

Figure 1: MoVe4SPS Approach

2 Problematic and objectives

As explained before, using digital twins is a common practice to design and monitor systems in a continuous way, in order to quickly investigate problems and accordingly produce patches. Yet, in digital twins, analog aspects are often left aside. Moreover, they are usually primarily interested in the safety of systems, while we expect to also handle the cyber-security and performance of CPS.

The objective of the thesis will be to define the notion of **digital-analog twins**, and to show how this new paradigm can help to better design complex CPS. The thesis will address this new paradigm for systems with hard security and performance constraints. Moreover, we expect the definition of a new development method for CPS based on digital/analog twins. This method shall in particular define how to efficiently combine formal techniques, simulation techniques, and prototyping techniques in order to produce a CPS respecting its requirements. This method shall also consider input feedbacks resulting from system execution.

3 Expected work

The select student will handle the following tasks:

1. Understand the current state of our support tools: TTool and SystemC-AMS

2. Establish a state-of-the art on digital twins and related contributions, especially in the scope of performance and cyber-security. A state-of-the-art will also be done for modeling techniques for analog aspects.

3. Propose a new paradigm: a digital/analog twin based on the definitions of new models and verification techniques.

4. Evaluate your contribution in the scope of the case study defined by one of the German partners of the project (Rheinland-Pfälzische Technische Universität-RPTU). This use case extends the smart grid model from the Vicinity European project.

4 Candidate Profile

Master 2 degree or equivalent including at least one the following field: embedded systems, cyber-physical systems, computer engineering, hardware/software co-design, cyber-security.

- Experience in System-level modeling and formal methods.
- Solid programming skills (C, Java).
- Ideally some experience in virtual prototyping and simulation.

5 How to apply?

Please send the following documents **in a unique pdf file** by email to ludovic.apvrille@telecom-paris.fr and daniela.genius@lip6.fr Incomplete applications won't be considered. Selected candidates will be evaluated on their technical abilities and on their ability to carry on research work (for instance by reviewing a research paper).

- Detailed CV
- Motivation letter clearly explaining why they would like to work on the topic of the Ph.D
- Recommendation letters
- Academic Transcripts (including ranking)
- List of publications (if any)

The thesis will be located within Lip6 in Paris Sorbonne University. Travel to RPTU (Germany) and to the Telecom Paris and ISAE research groups, andparticipation in dissemination events (workshops and conferences) will be financed by the project. Participation in the preparation of a project workshop organized by Lip6 is expected.

References

[Apv23] Ludovic Apvrille. *TTool, an open-source toolkit for the modeling and verification of embedded systems, https://ttool.telecom-paris.fr*, (accessed 2023).

[BEG+16] Martin Barnasconi, Karsten Einwich, Christoph Grimm, Torsten Maehne, and Alain Vachoux. *SystemC AMS Extensions 2.0 Language Reference Manual.* Accellera systems initiative, January 2016.

[CGA21] Rodrigo Cortés Porto, Daniela Genius, and Ludovic Apvrille. Handling causality and schedulability when designing and prototyping cyber-physical systems. *Software and Systems Modeling*, pages 1–17, 2021.

[con03] SoCLib consortium. The SoCLib project: An integrated system-on-chip modelling and simulation platform. Technical report, CNRS, 2003. www.soclib.fr.

[FE98] Peter Fritzson and Vadim Engelson. Modelica—a unified object-oriented language for system modeling and simulation. In *European Conf. on Object-Oriented Programming*, pages 67–90. Springer, 1998.

[SG13] Bran Selic and Sébastien Gérard. *Modeling and Analysis of Real-Time and Embedded Systems with UML and MARTE: Developing Cyber-Physical Systems.* Elsevier, 2013.