Hw/Sw Co-Design of Data-Dominated Systems-on-Chip
- The $\Psi$-chart Approach in TTool/DIPLODOCUS -

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System Level Modeling with the $\Psi$-chart: Application, Communications, Architecture and Mapping

Application (what): Dataflow graph with data and functional abstractions, where algorithms are described using abstract cost operators

Communications (how): Behavioral model of generic communication protocols that are described independently of the application and architecture models

Architecture (who): Set of interconnected generic hardware nodes, decorated with parameters, e.g., bus width, arbitration policy

Mapping (where): The workload of an application and the behavior of communication models are associated to the architecture units

Design Space Exploration: Simulation and Formal Verification at the push of a button

Automatic Generation of Executable Code from High Level Models

- Chart: Application, Communications, Architecture and Mapping

- Chart Approach in TTool/DIPLODOCUS -

$\Psi$-chart of the application is automatically generated for rapid prototyping on the real hardware: only memory allocation and data-blocks addresses must be manually encoded

- Model-checking of system properties (e.g., safety, schedulability, performance) with LOTOS and UPPAAL
- Functional simulation interactively, with graphical interface and debug facilities (e.g., breakpoints, simulation traces)

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