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A Coverage Driven Verification Environment for UML Models of Systems-on-Chip

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DIPLODOCUS: A 3-step Methodology Environment based on UML
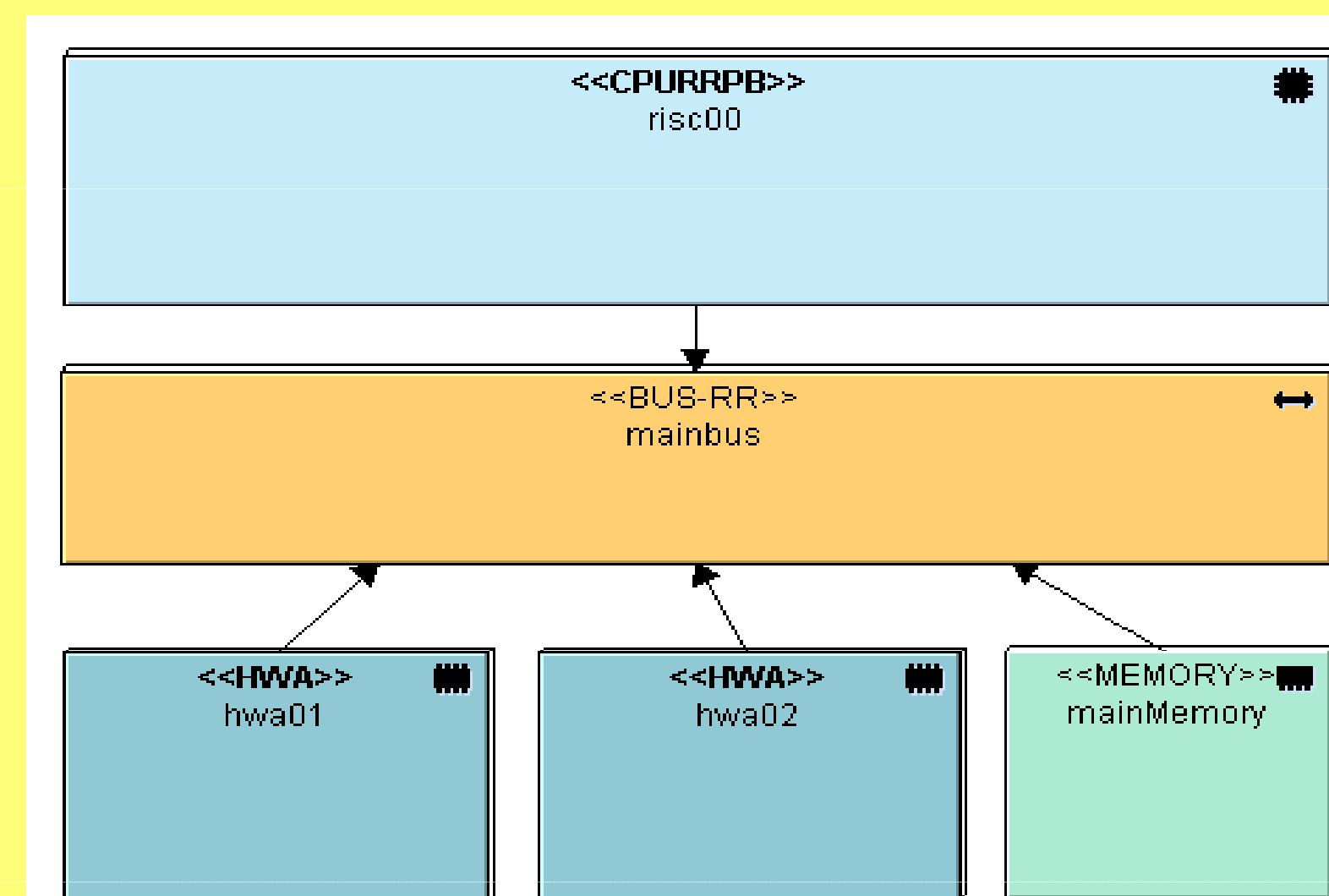
(1) Application Modelling

- System is modeled in terms of **communicating tasks** (UML class diagram)
- Behavior modeling is focused on **control part of the application** (UML activity diagrams)
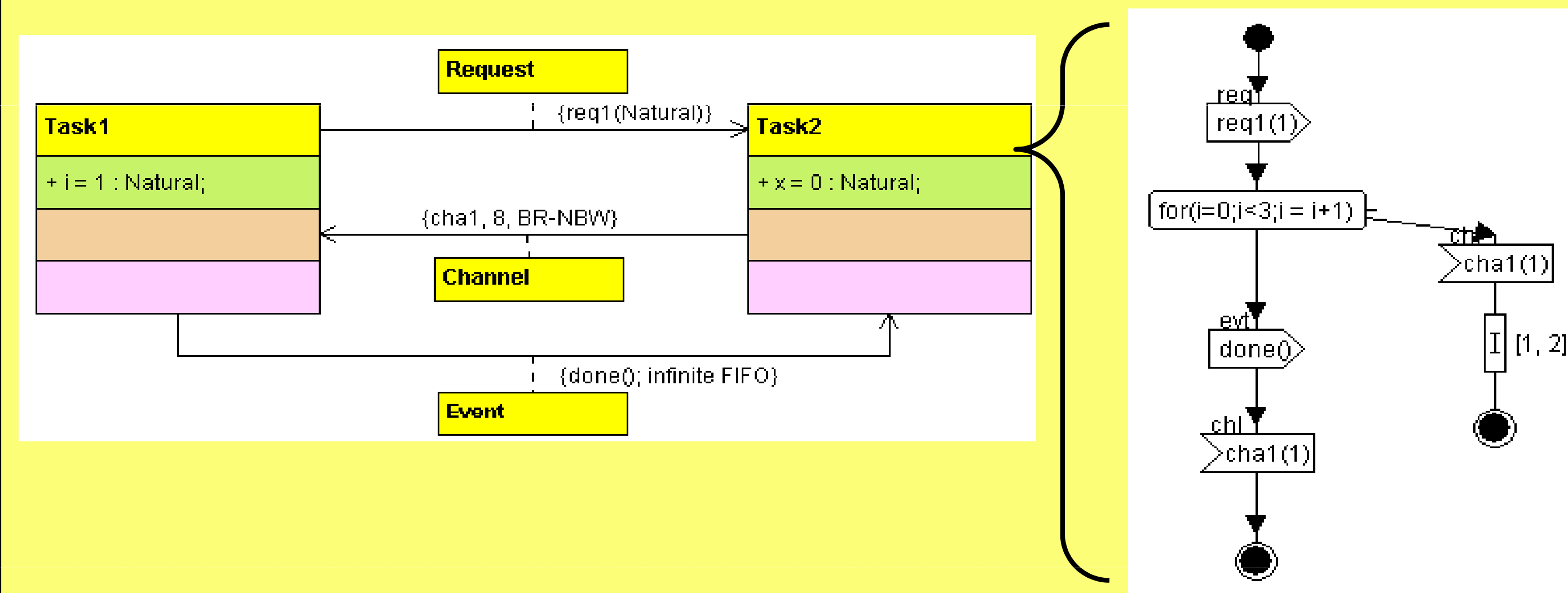
(2) Architecture modelling

- Hardware architecture is modeled using **generic hardware components** (CPUs, buses, hardware accelerators)

Mapping

(3) Application mapped onto an architecture

Refinement

An **open-source** toolkit – called **TTool** – fully supports this methodology

Simulation, Formal analysis

- **Computation** and **communication** operations are **abstracted using symbolic instructions**
- Abstractions allow for **fast simulation,** transactions spanning **hundreds of clock cycles** are **executed as a whole**
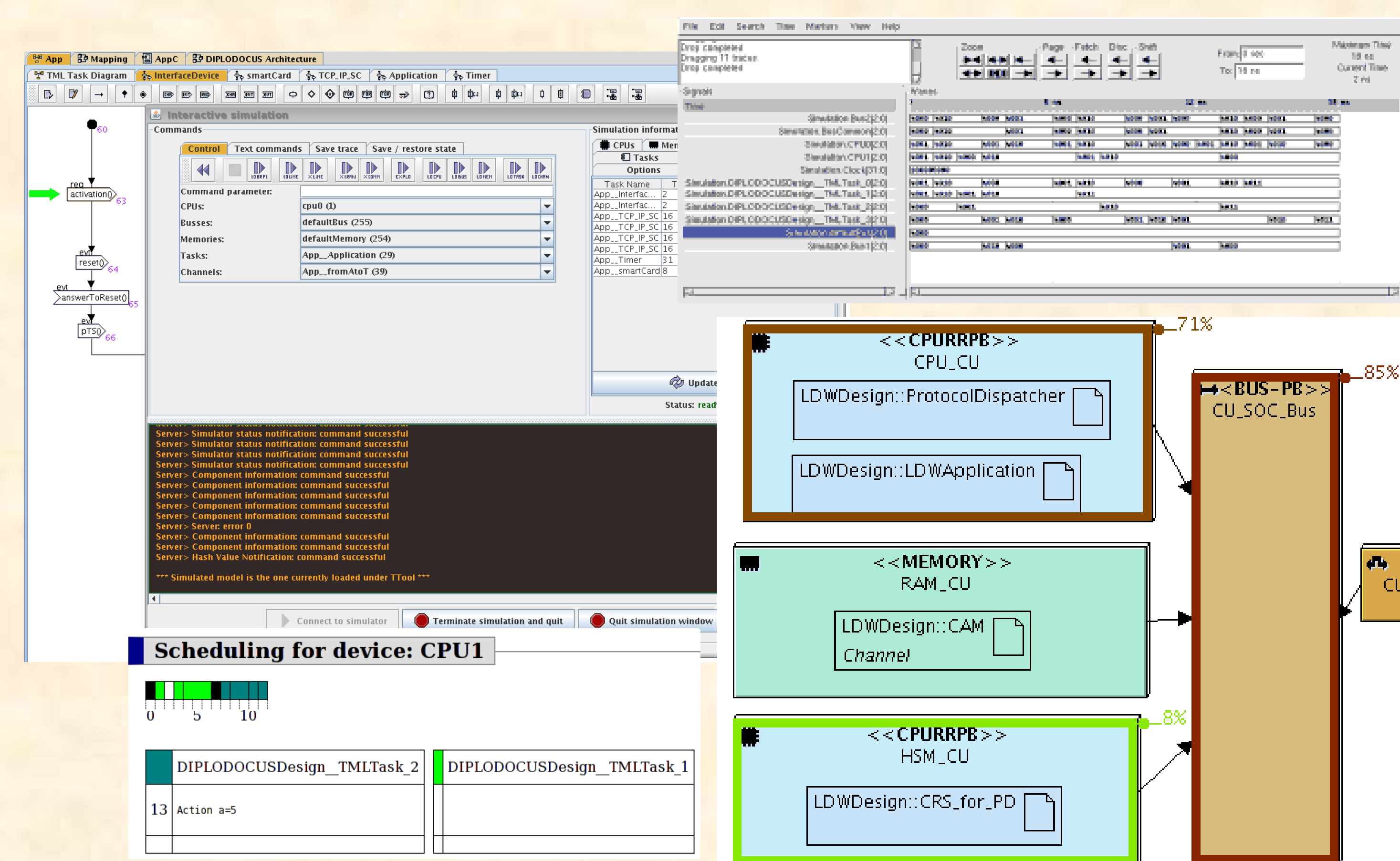- Possibility to generate traces in VCD format, as Gantt Diagrams and as reachability graphs

For a car communication application, we achieved an order of magnitude of simulation speed of
Billions of cycles/sec.

A more fine grained model of an MPEG decoder led to a rate of
Millions cycles/sec.

Variable Application Coverage

Formal verification

Coverage driven Simulation

Simulation

Operation Point

Model Coverage — Simulation Speed

Current Cmd in Tasks
Task Variables
Inter Task Comm. States

Application State Space

Coverage Selector
Not covered by Verification
Covered by Verification
Arch. Mapping
Non-significant

Sampled at Check Points
Local Dependence Analysis
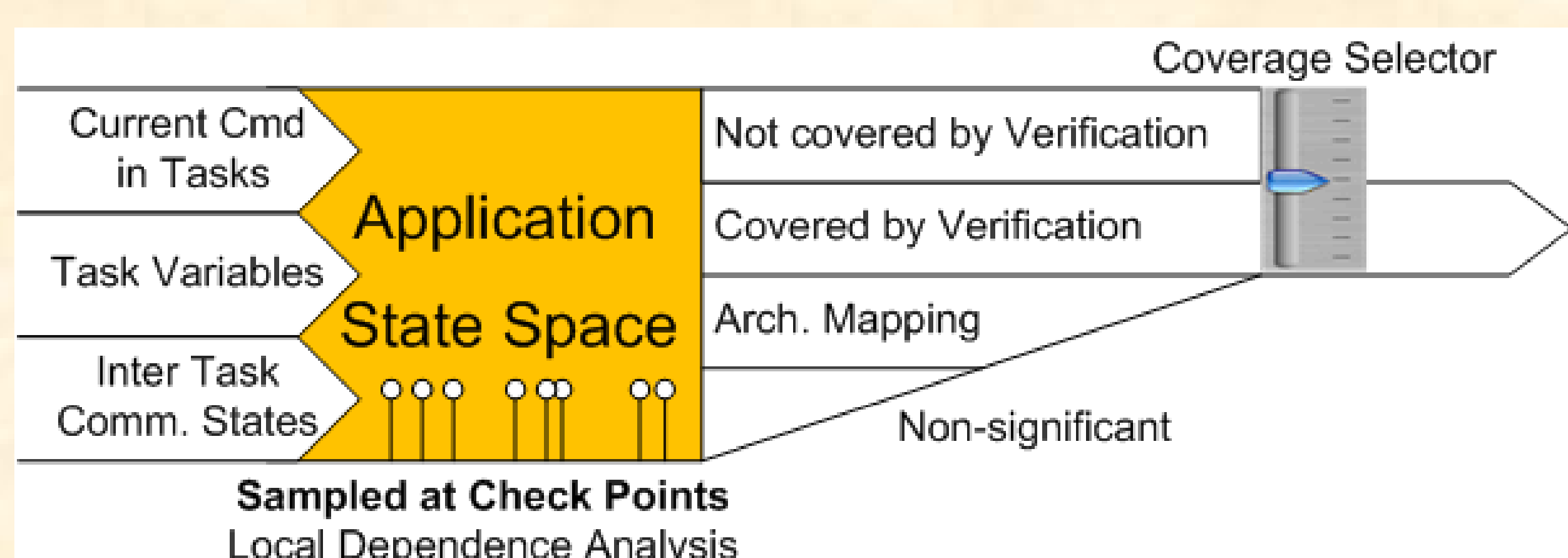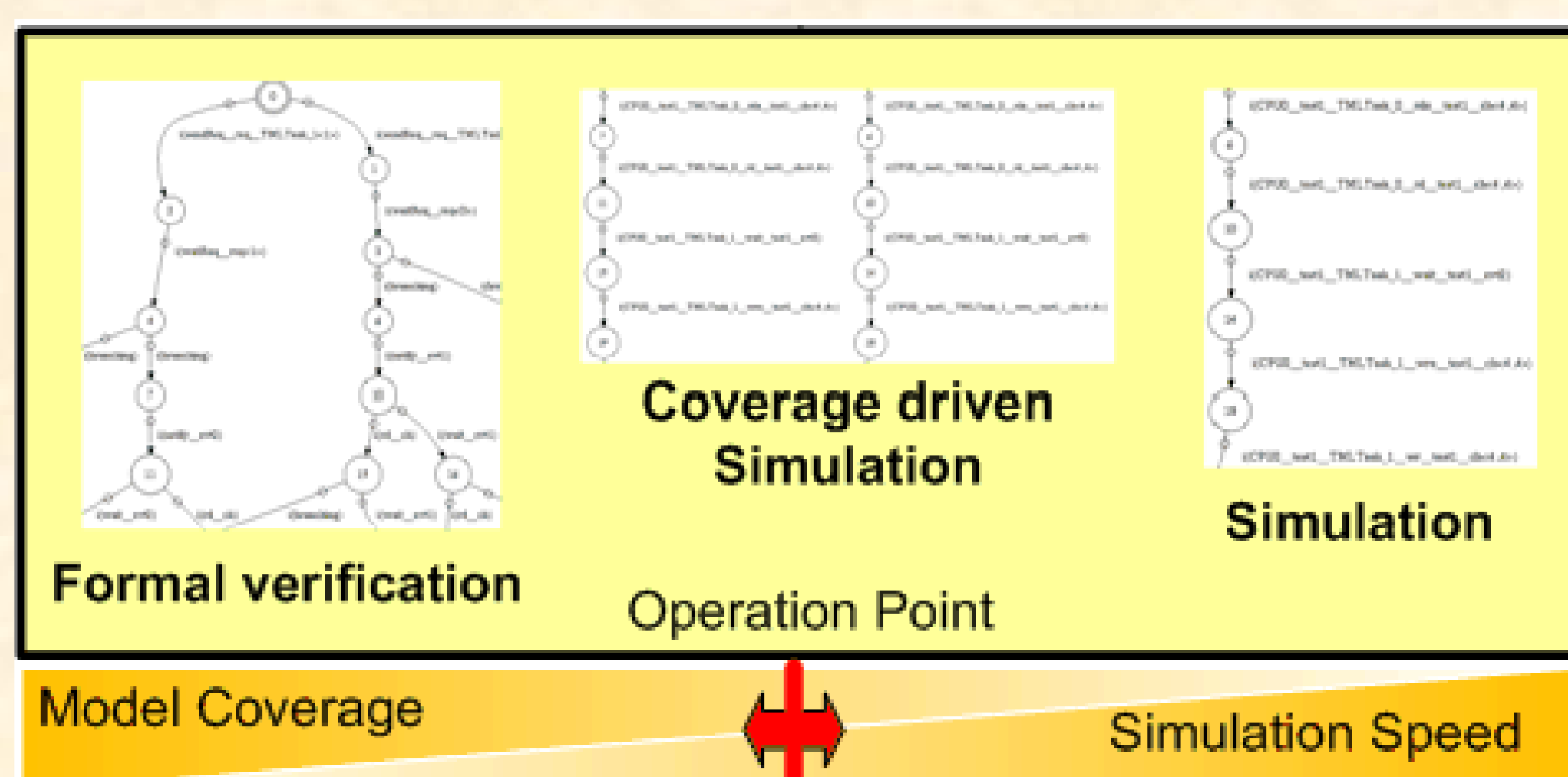
Interactive Simulation

For further information: http://labsoc.comelec.enst.fr/ttool/

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