

ChangeLog

Rev 1.0 :

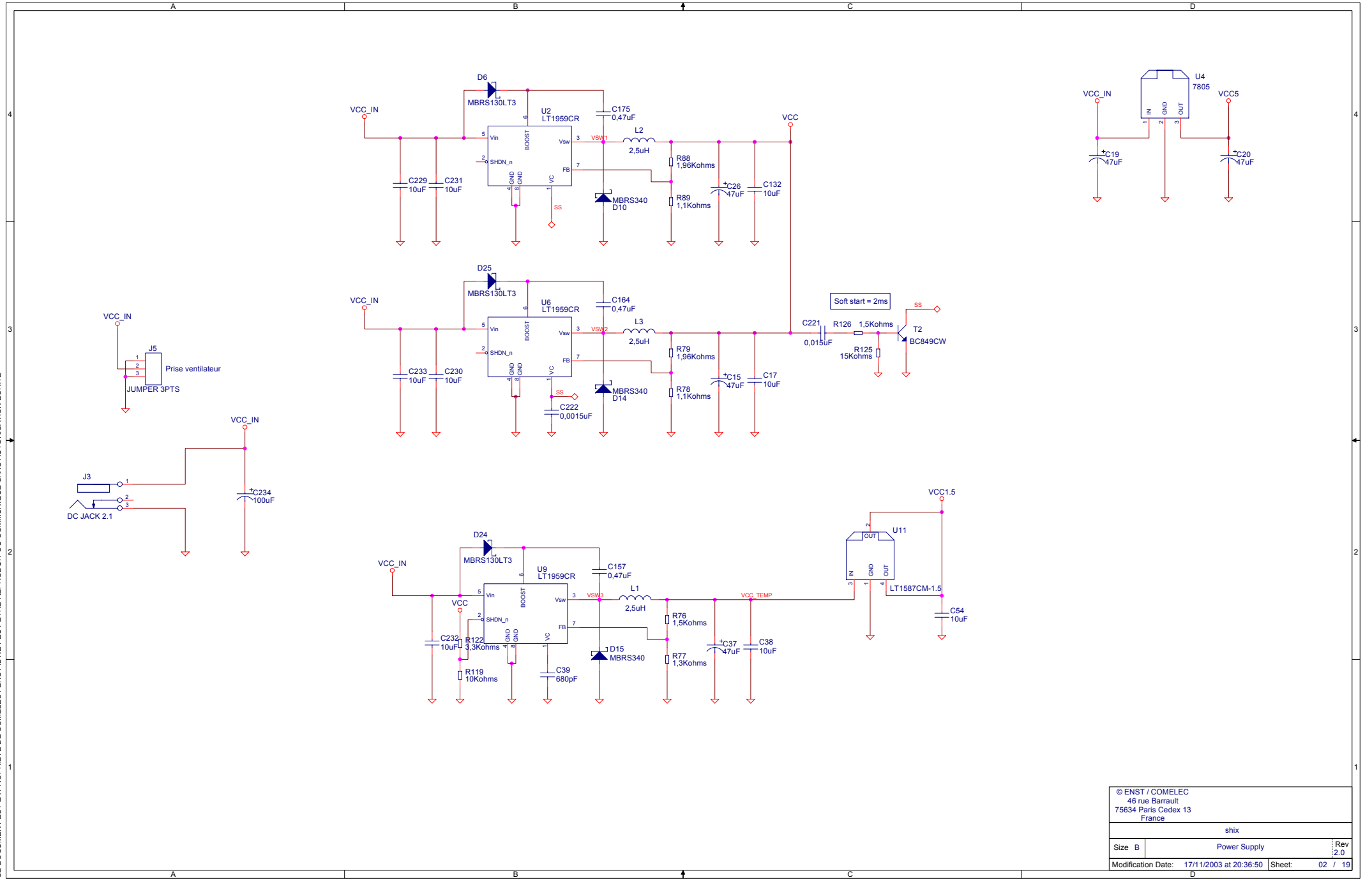
- 17/10/2002 : Project creation

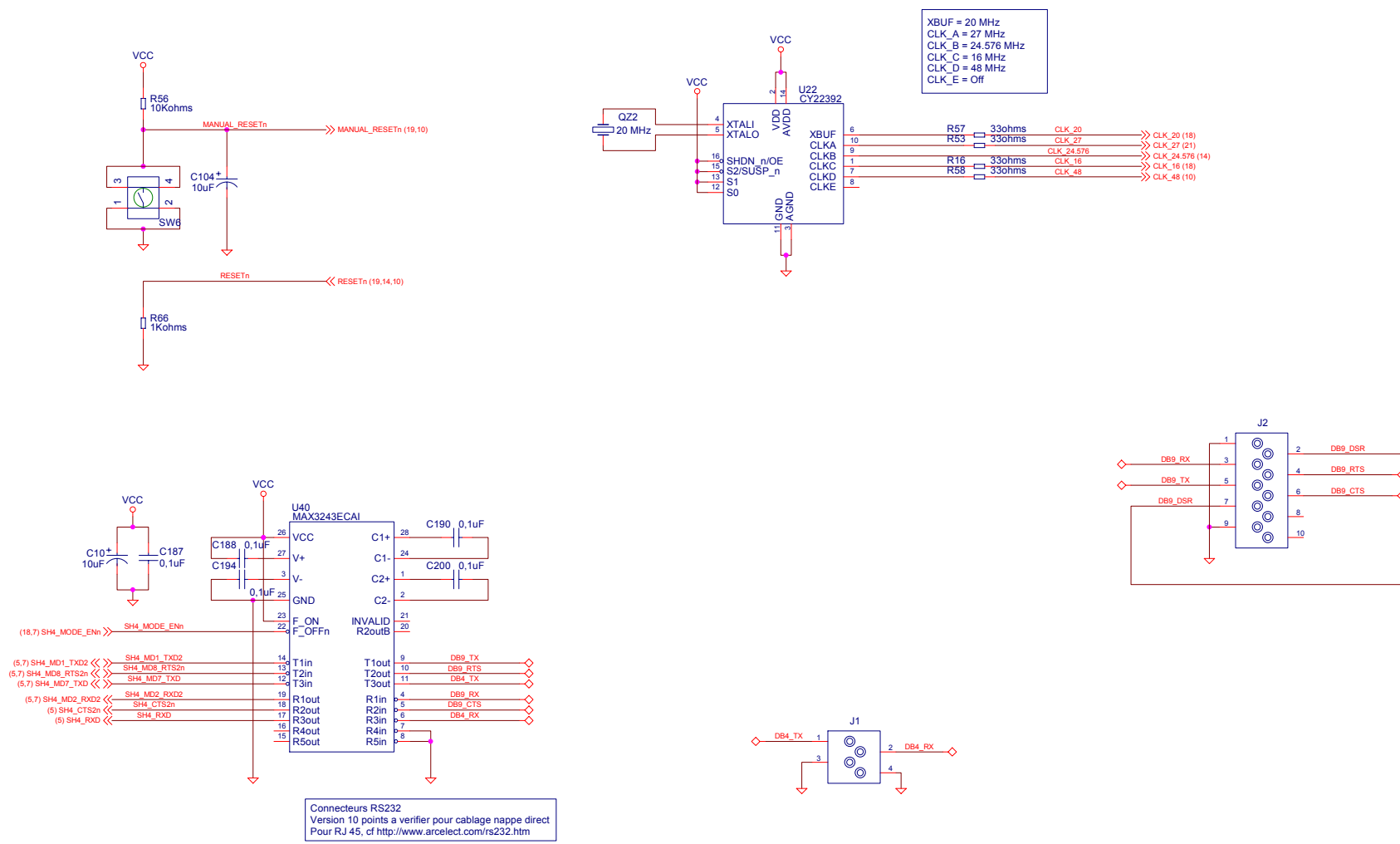
Rev 2.0 :

- corrected button switch wiring
- renamed SH4_BS into SH4_BSn
- removed jumpers for FPGA configuration, replaced with analog switch (p.13)
- changed SH4 mode configuration switches. "On" is now state "high".
- removed DACK and DREQ on USB Host (SL811) (host only mode)
- added USB 2.0 peripheral device
- removed LCD display
- changed TRSTn wiring (SH4 H-UDI interface) for full compatibility with Codescape
- Stratix PLL power supply : now VCC1.5 instead of VCC...
- Added 2 LVDS inputs (2*2) ans 2 LVDS outputs 2*2) on expansion bus
- corrected bicolor LEDs footprint
- corrected Power Jack type and footprint
- modified power supply / added soft start

- 1 : Cover page
- 2 : Power supply
- 3 : Reset / Clocks / UART
- 4 : SH4 Bus
- 5 : SH4 Misc
- 6 : SDRAM
- 7 : SH4 Boot Options
- 10 : USB host and Peripheral
- 11 : Nand Flash
- 13 : Config FPGA
- 14 : Video
- 15 : Video RAM
- 16 : FPGA Alims / Temp
- 17 : Leds / Switchs / Misc
- 18 : FPGA South (SH4 Bus)
- 19 : FPGA East (peripherals)
- 20 : FPGA West (Expansion Bus)
- 21 : FPGA North (Video)
- 22 : Synoptic

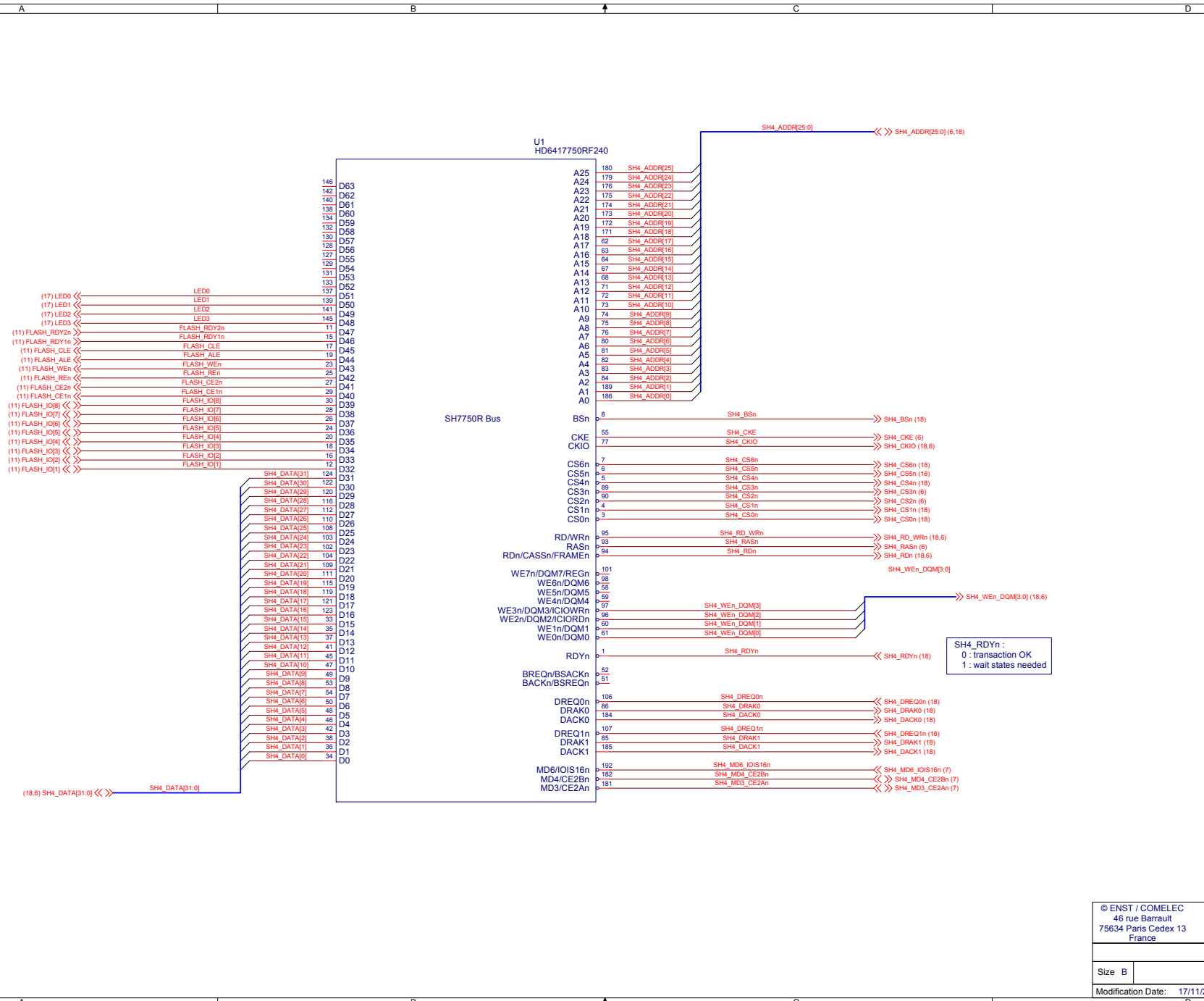
TODO :



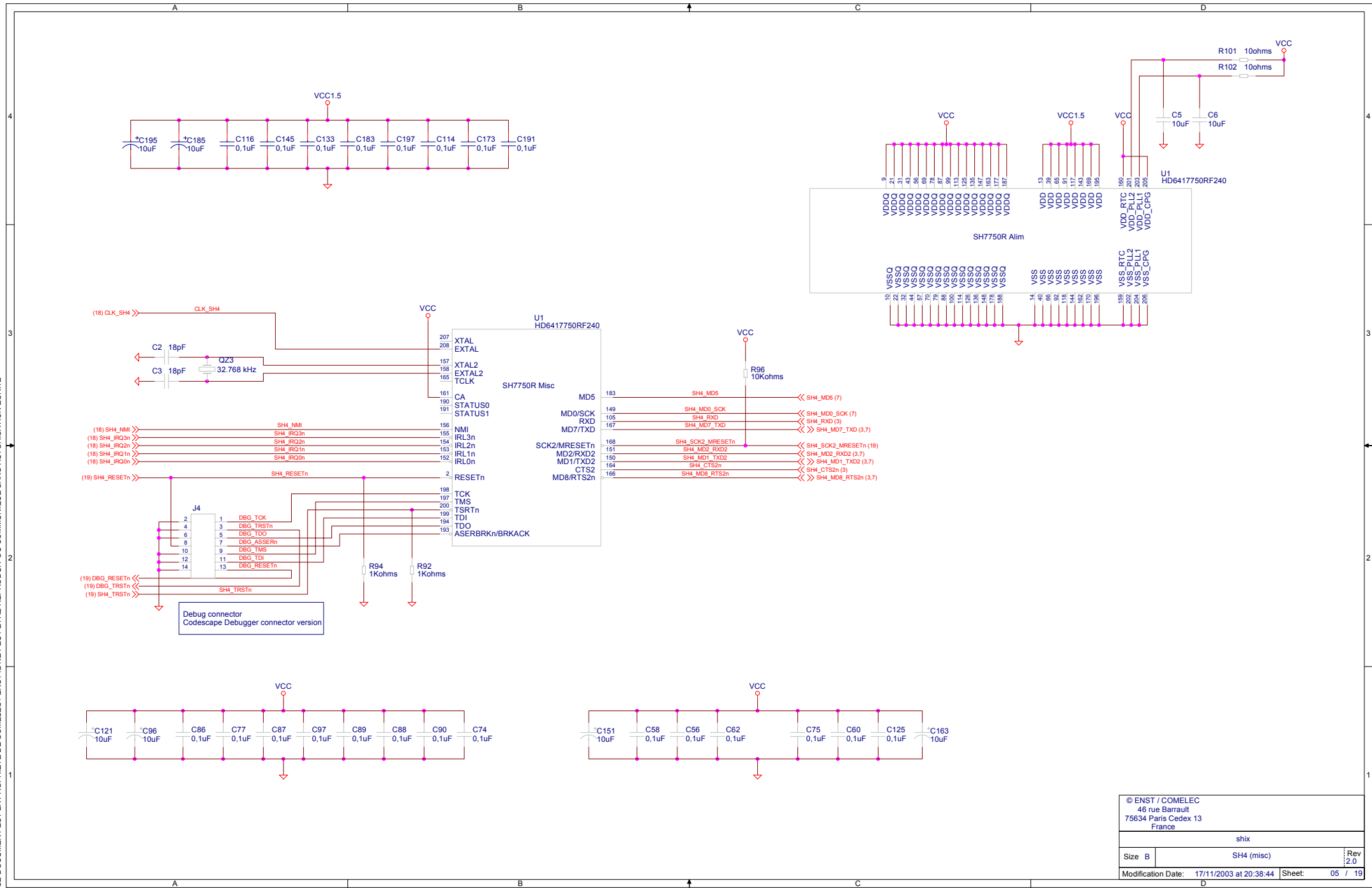


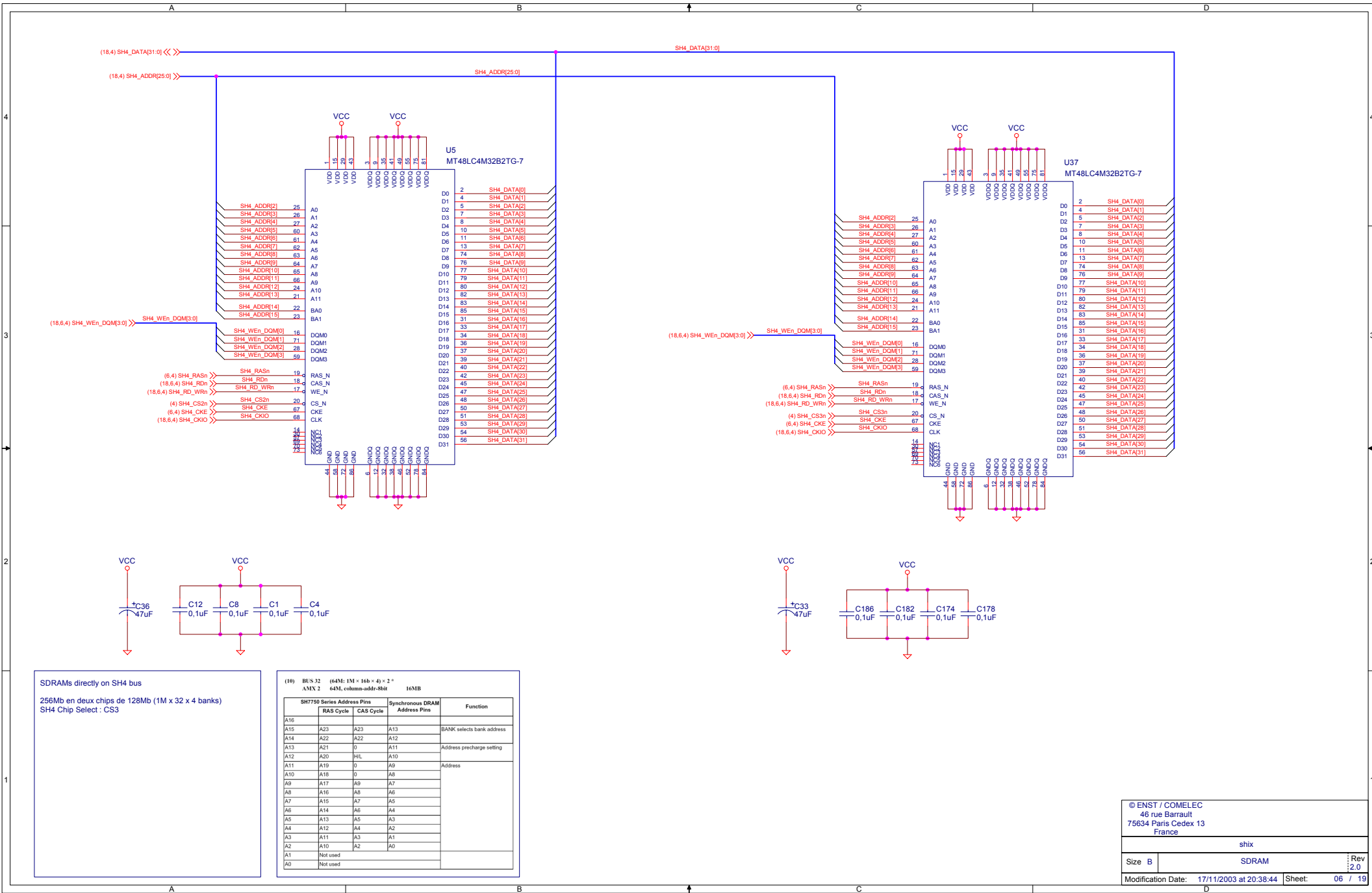
Connecteurs RS232
Version 10 points a verifier pour cablage nappe direct
Pour RJ45, cf <http://www.acelect.com/rs232.htm>

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SH4_RDYn :
0 : transaction OK
1 : wait states needed

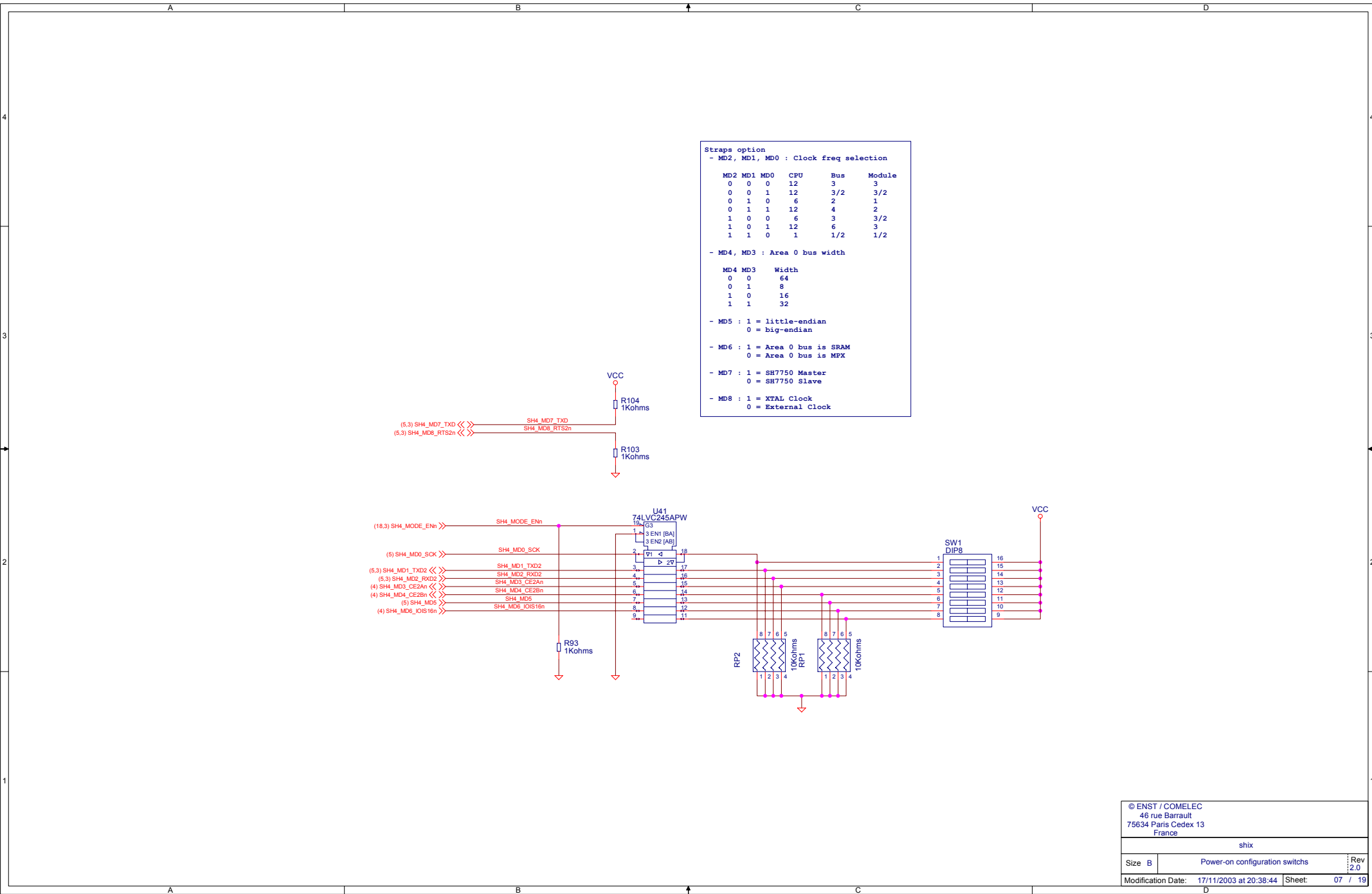




SDRAMs directly on SH4 bus
 256Mb en deux chips de 128Mb (1M x 32 x 4 banks)
 SH4 Chip Select : CS3

(16) BUS 32 (64M: 1M x 16h x 4) x 2 *
 AMX 2 64M: column-addr-8h 16MB

SH7758 Series Address Pins			Synchronous DRAM Address Pins		Function
	RAS Cycle	CAS Cycle			
A16					
A15	A23	A23	A13		BANK selects bank address
A14	A22	A22	A12		
A13	A21	0	A11		Address precharge setting
A12	A20	NIL	A10		
A11	A19	0	A9		Address
A10	A18	0	A8		
A9	A17	A9	A7		
A8	A16	A8	A6		
A7	A15	A7	A5		
A6	A14	A6	A4		
A5	A13	A5	A3		
A4	A12	A4	A2		
A3	A11	A3	A1		
A2	A10	A2	A0		
A1	Not used				
A0	Not used				



Straps option

- MD2, MD1, MD0 : Clock freq selection

MD2	MD1	MD0	CPU	Bus	Module
0	0	0	12	3	3
0	0	1	12	3/2	3/2
0	1	0	6	2	1
0	1	1	12	4	2
1	0	0	6	3	3/2
1	0	1	12	6	3
1	1	0	1	1/2	1/2

- MD4, MD3 : Area 0 bus width

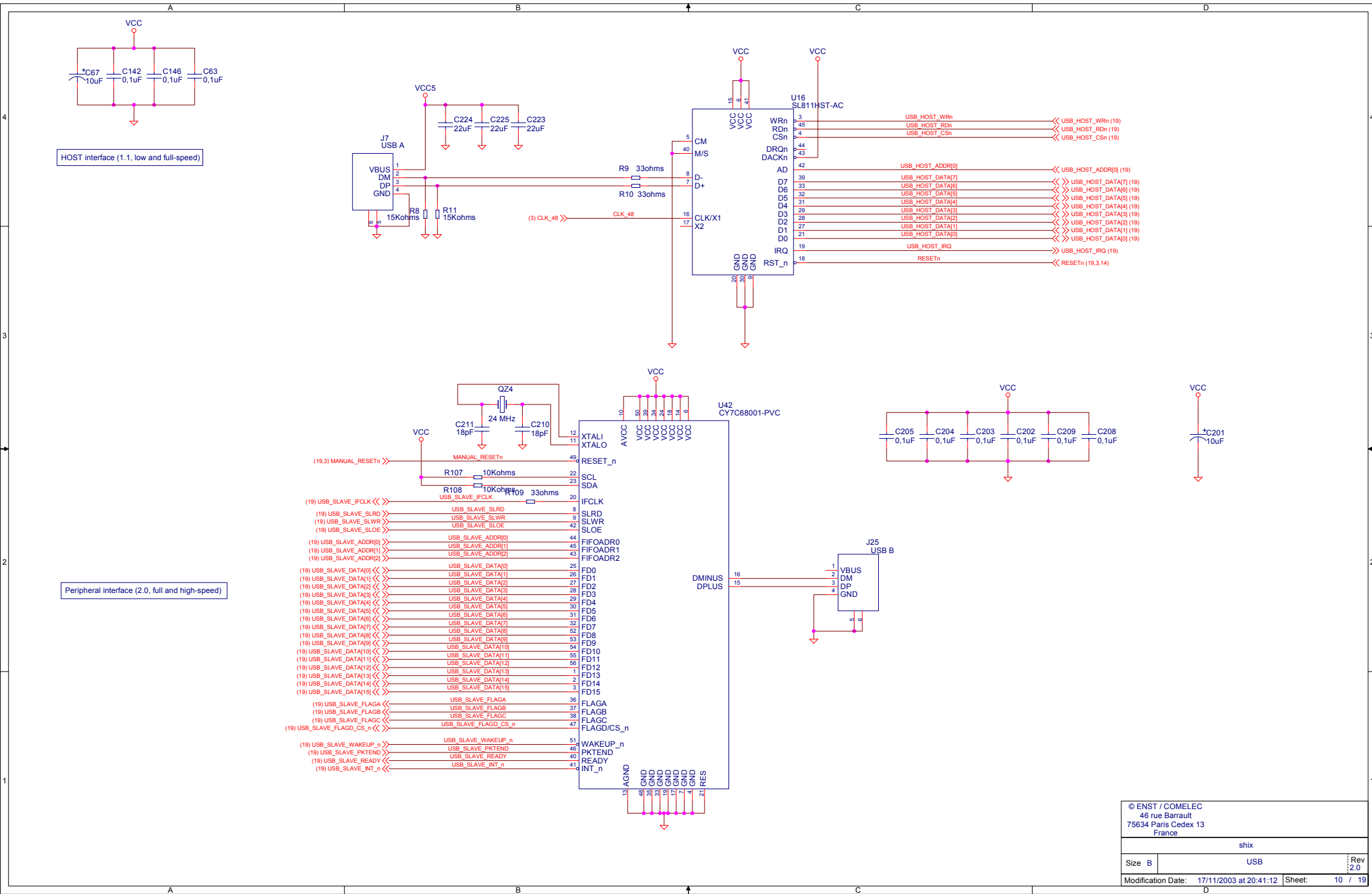
MD4	MD3	Width
0	0	64
0	1	8
1	0	16
1	1	32

- MD5 : 1 = little-endian
0 = big-endian

- MD6 : 1 = Area 0 bus is SRAM
0 = Area 0 bus is MPX

- MD7 : 1 = SH7750 Master
0 = SH7750 Slave

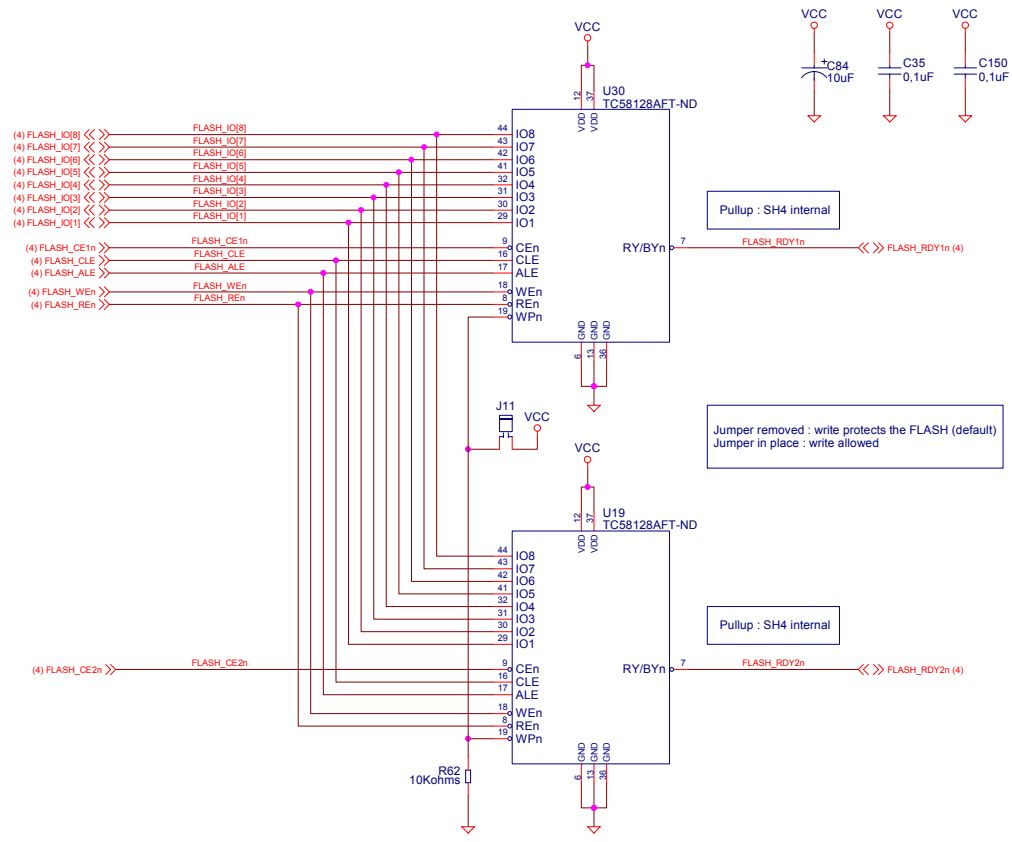
- MD8 : 1 = XTAL Clock
0 = External Clock



HOST interface (1.1, low and full-speed)

Peripheral interface (2.0, full and high-speed)

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shix		
Size B	USB	Rev 2.0
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Attention, une FLASH NAND ne s'adresse pas du tout comme une Flash (SRAM / ROM) normale.
C'est un device oriente IO, avec un protocole bien precis, gere par le FPGA

Deux devices de 128Mb (16MB, pages de 512+16 octets, blocks de 32 pages)
soit au total 32MB de flash.

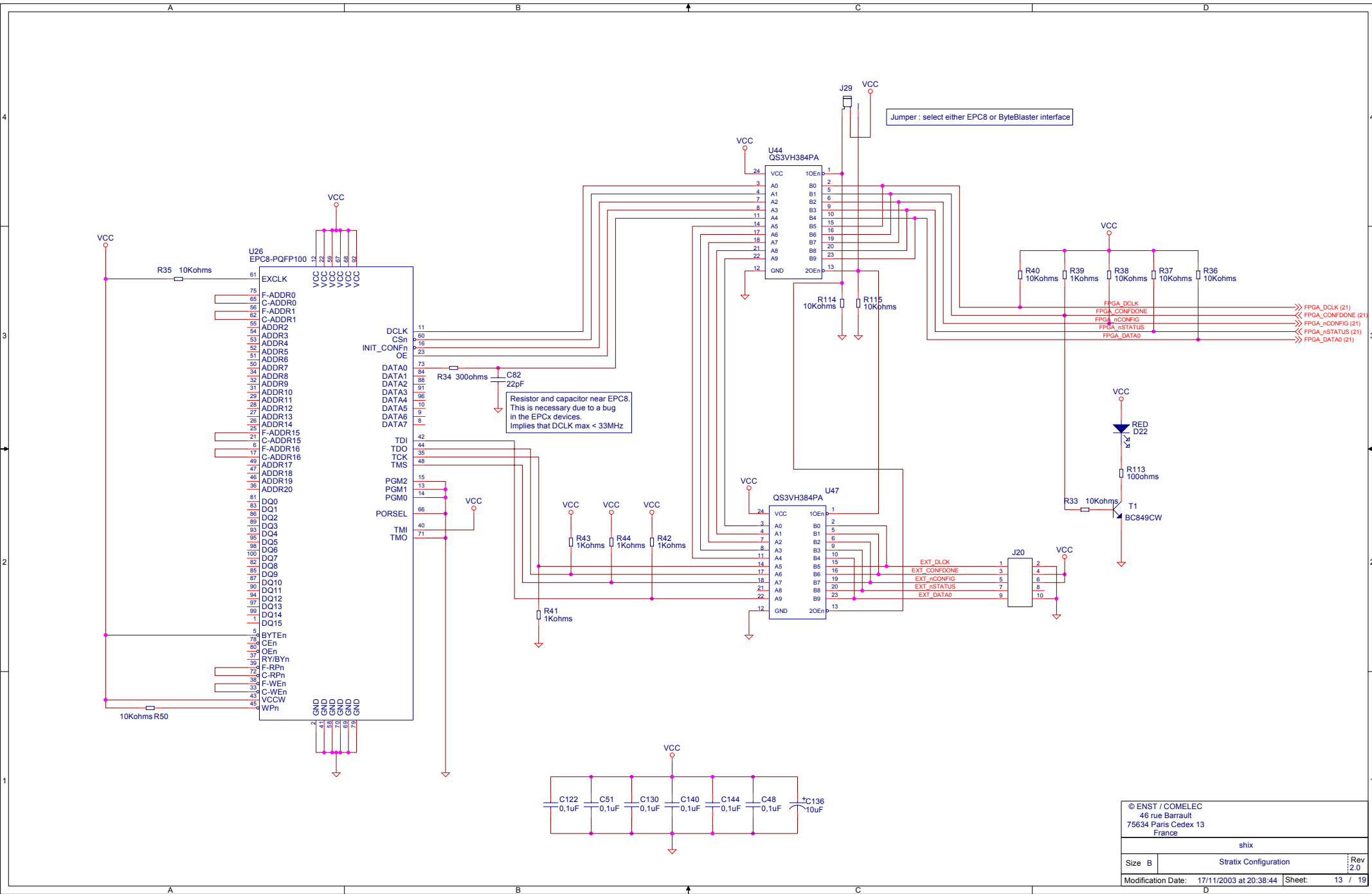
Le deuxieme chip est DNP par defaut

Jumper removed : write protects the FLASH (default)
Jumper in place : write allowed

Pullup : SH4 internal

Pullup : SH4 internal

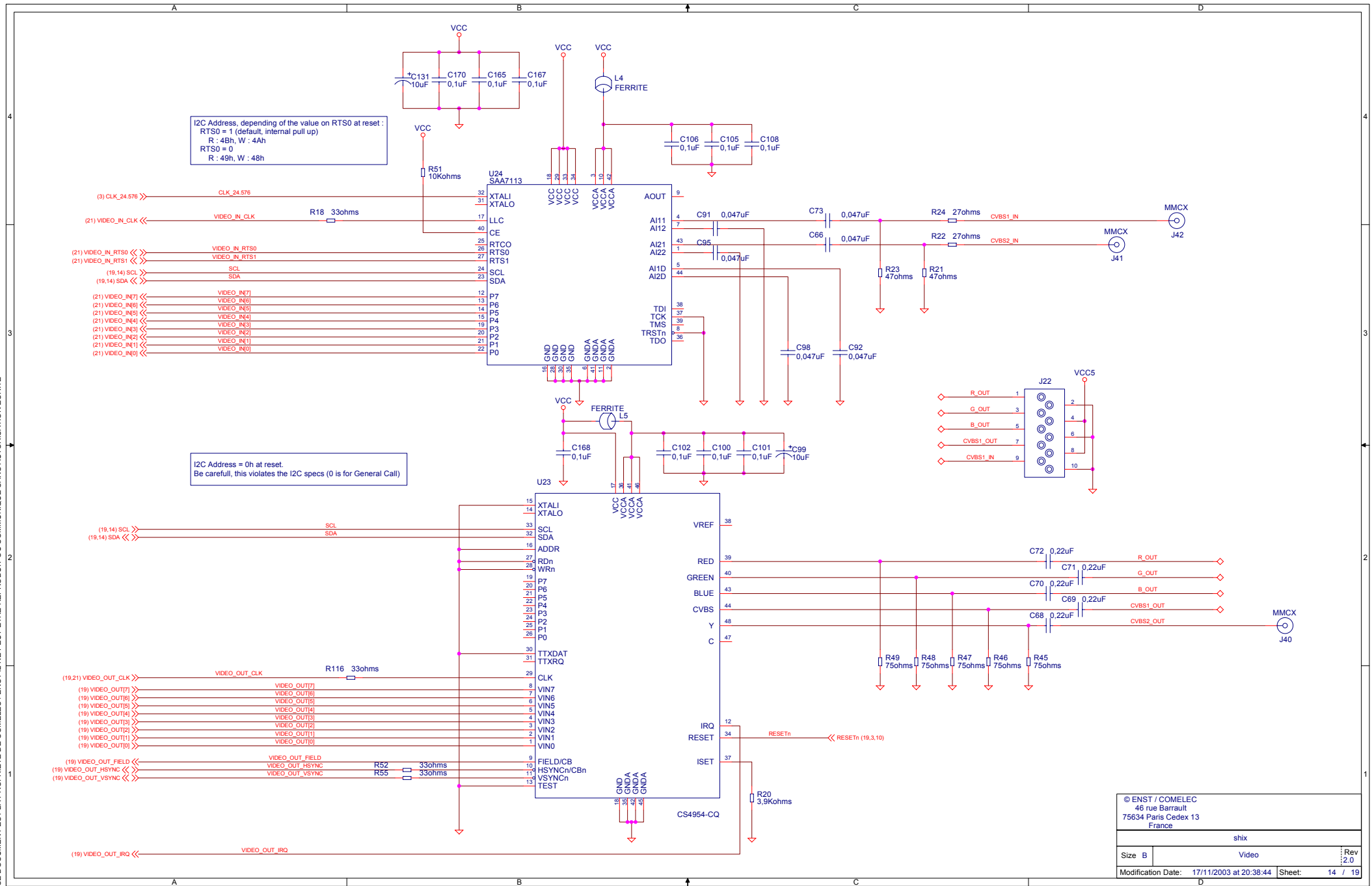
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Jumper : select either EPC8 or ByteBlaster interface

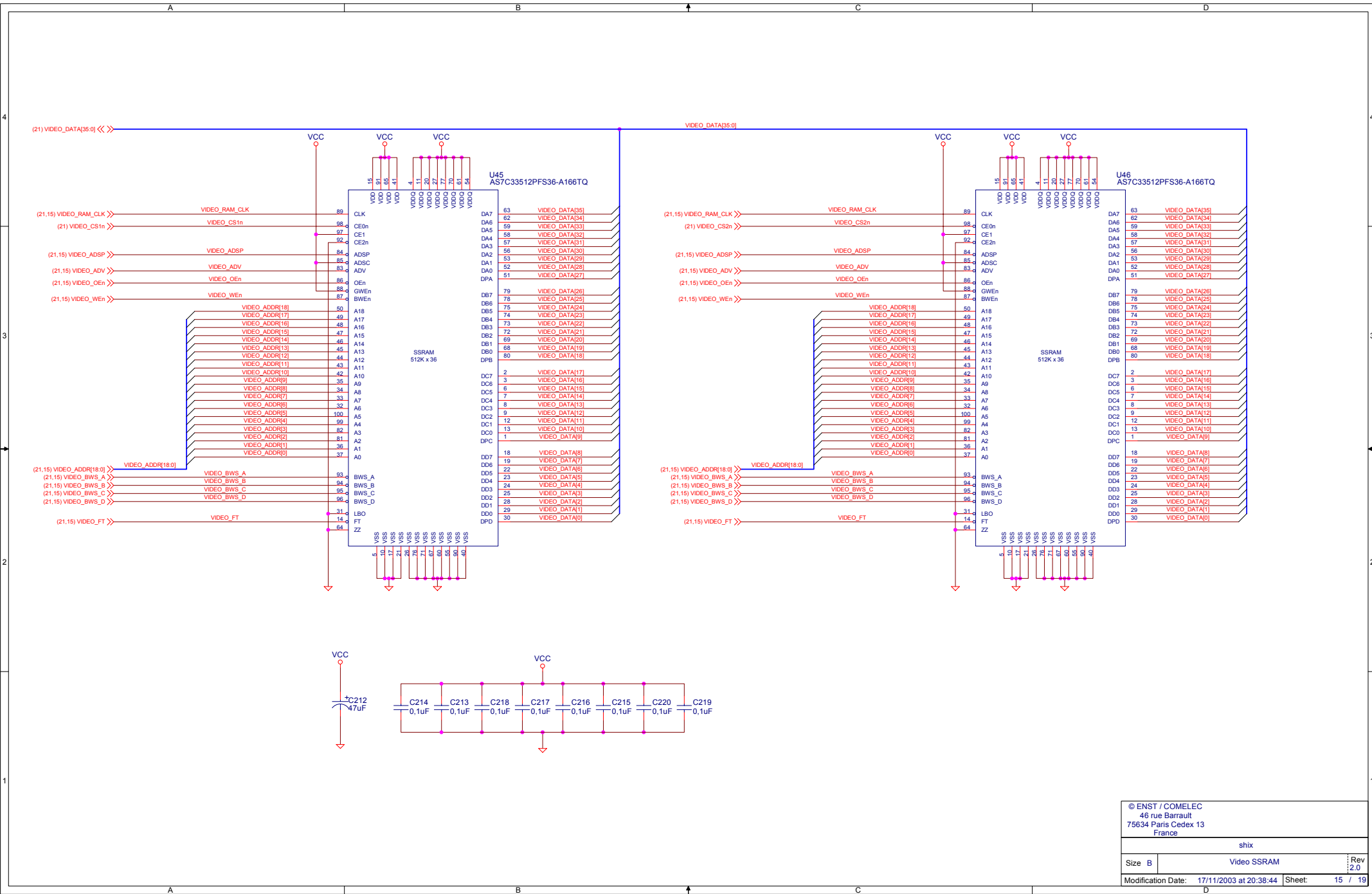
Resistor and capacitor near EPC8.
This is necessary due to a bug
in the EPCx devices.
Implies that DCLK max < 33MHz

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shix		
Size B	Stratix Configuration	Rev 2.0
Modification Date: 17/11/2003 at 20:38:44		Sheet: 13 / 19

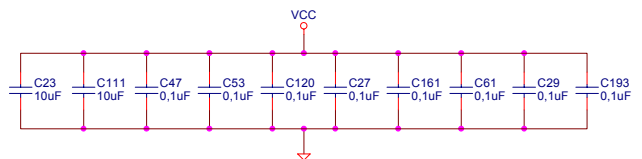
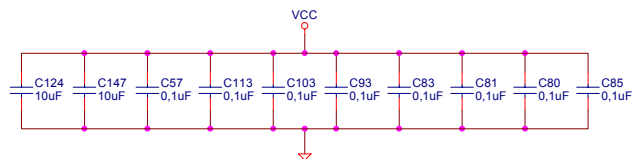
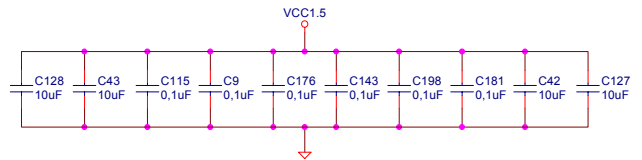
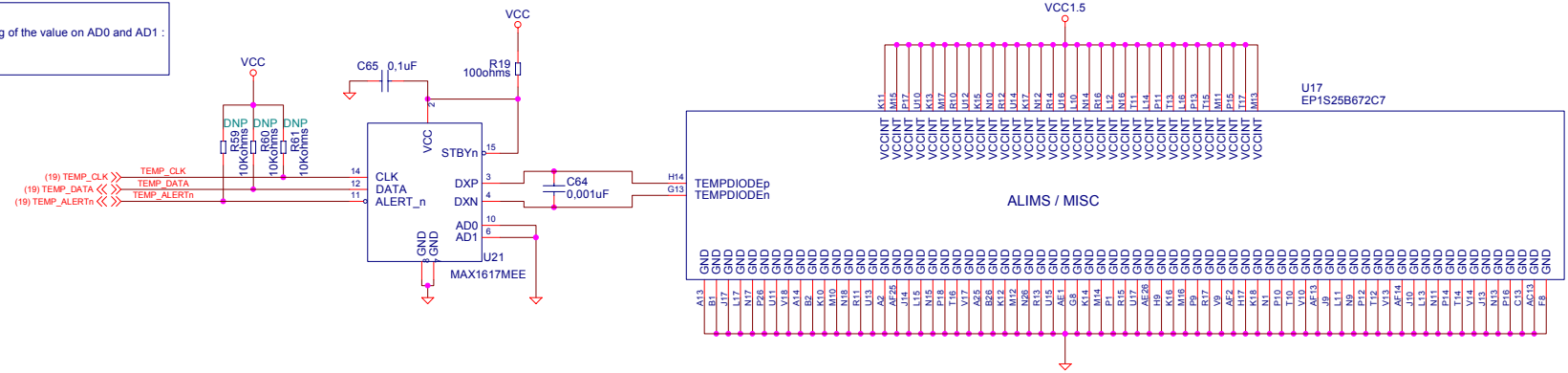


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shix		
Size B	Video	Rev :2.0
Modification Date:	17/11/2003 at 20:38:44	Sheet: 14 / 19

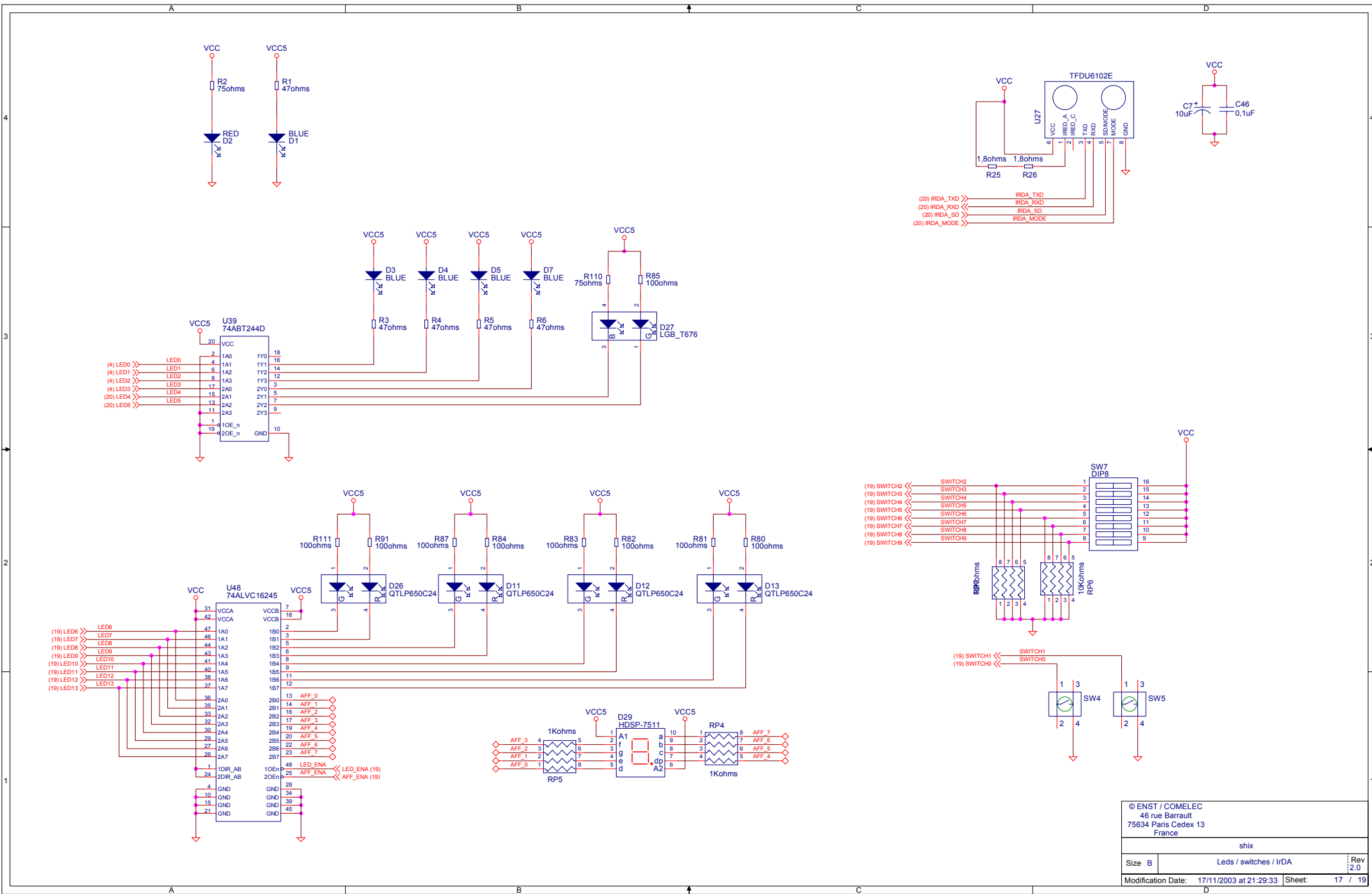
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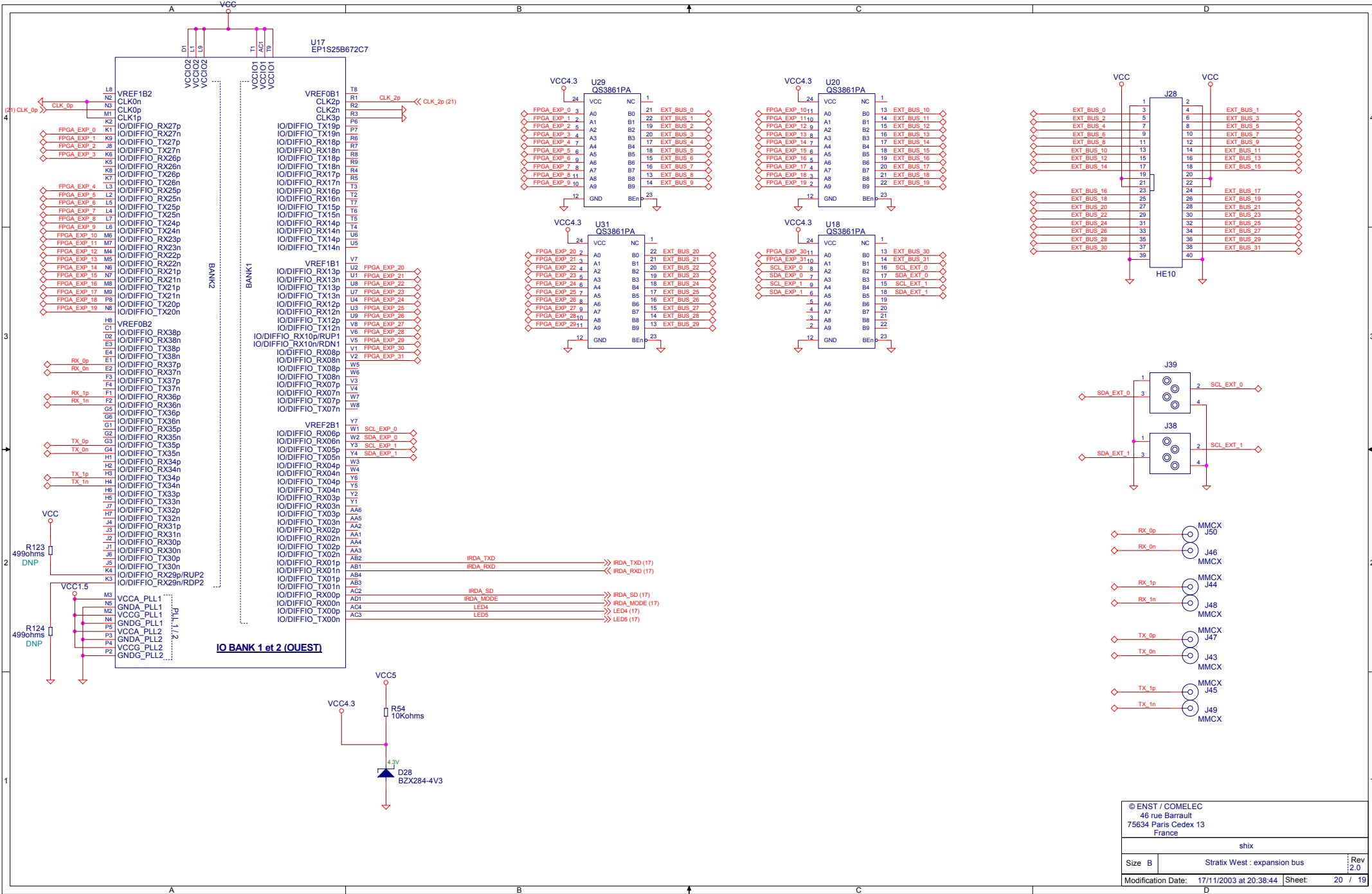
I2C Address, depending of the value on AD0 and AD1 :
GND / GND : 18h



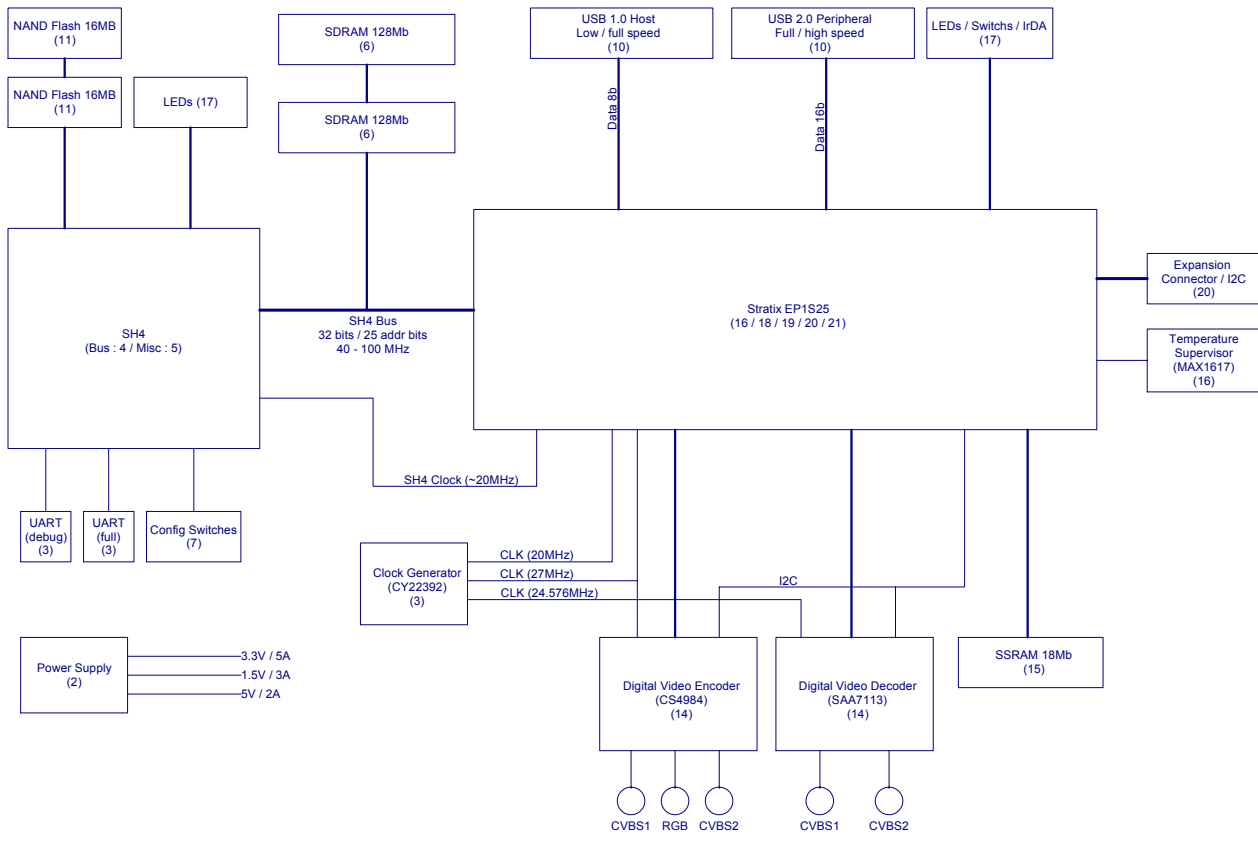
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shix		
Size B	Leds / switches / IrDA	Rev 2.0
Modification Date: 17/11/2003 at 21:29:33		Sheet: 17 / 19



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shix		
Size B	Synoptic	Rev : 2.0
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