Acronyme du projet/ Acronym of the project	**Innov-Xes** (or VePLATES or RIPES-X or RIDE 4 XES or Innov-Xes, or (Change the variable, not the text above) VePLATES: Verification and validation PLATform for Embedde Systems RIPES-X: Research and Innovation platform for Embedded System and complexity RIDE 4 XES: Research and Innovation platform in DEsign and validation for complex Embedded Systems Innov-Xes: Innovation for compleX embedded systems Embed-X: EASE-X:Embedded Architecture and System Engineering with compleXity PVC: platform for the V cycle
Titre du projet en français	Plateforme de Recherche et d'Innovation pour la Conception, Vérification et Validation des Systèmes Embarqués Complexes.
Project title in English	Research and Innovation Platform for Design, Verification and Validation of Complex Embedded Systems. (Change the variable, not the text above)
Coordinateur du projet/Coordinatorof the project	Nom / Name : Etablissement / Institution : CEA Laboratoire / laboratory : LIST Numéro d'unité/unit number :
Aide demandée/ Requested funding	Tranche 1/Phase 1 € | Tranche 2/Phase 2 €
Champs disciplinaires / disciplinary field	□ Santé, bien-être, alimentation et biotechnologies / health, well-being, nutrition and biotechnologies □ Urgence environnementale et écotechnologies / environnemental urgency, ecotechnologies X Information, communication et nanotechnologies / information, communication and nanotechnologies □ Sciences humaines et sociales / social sciences □ Autre champ disciplinaire / other disciplinary scope
Domaines scientifiques/ scientific area	Design, verification, realization and validation of complex embedded systems

Affiliation(s) du partenaire coordinateur de projet/ Organization of the coordinating partner

Laboratoire(s)/Etablissement(s) Laboratory/Institution(s)	Numéro(s) d'unité/ Unit number	Tutelle(s) /Research organization reference
Commissariat à L'Energie Atomique et aux Energies Alternatives (CEA)		

Affiliations des partenaires au projet/Organization of the partner(s)

To be completed with other (industrial) links

Laboratoire(s)/Etablissement(s) Laboratory/Institution(s)	**Numéro(s) d'unité/ Unit number**	**Tutelle(s)/Research organization reference**
ENS Cachan		
ENSTA		
INRIA		
Institut Télécom		
LRI		
Polytechnique		
Supelec		
Entreprise(s) / company	**Secteur(s) d'activité/activity field**	**Effectif/ Staff size**
Thales		
Delphi ?	Automotive/transportation	
	Microlectronics	
	Energy	
	xxx	

Avant de soumettre ce document :

Supprimer toutes les instructions en indigo (par exemple en faisant Format → Styles → Menu contextuel du style « Instructions » → Sélectionner toutes les occurrences → suppr.)

Mettre la table des matières à jour (bouton droit sur la table des matières → mettre à jour les champs → Mettre à jour toute la table).

Donner toutes les références bibliographiques en annexe 7.1 et 7.2.

Text in yellow need to be improved, modified or added.
Text in green is to be removed.
Text in blue is nominated action points.

RESUME / SUMMARY

(2 pages maximum)

Ce résumé devra démontrer l'originalité du projet, et présenter les points suivants :

- *le contexte et les objectifs scientifiques dans lesquels s'inscrit la demande d'équipement, et comment ces objectifs seront poursuivis par le(s) partenaire(s) au projet,*

- *les verrous scientifiques et techniques,*
- *le programme de travail,*
- *le caractère innovant des projets que permettra d'aborder l'équipement,*
- *les retombées scientifiques, techniques et économiques (ouverture pluridisciplinaire, aspect structurant pour les partenariats académiques et public-privé…),*
- *les modes de valorisation des résultats de la recherche (publications, cession ou licence de brevets…).*

Embedded electronic systems have had a tremendous impact on everyday life over the past decades in all domains, from transportation (by car, train or plane), to consumer electronics (mobile phones, audio and video systems, home), medicine, energy, etc. In the future, it will undoubtedly remain one of the major technologies for taking on societal challenges shaping France, its values, and its global competitiveness.
These systems are becoming more and more complex, not only due to the ever increasing integration of intelligent components (Systems on Chip – SoC -, multicores, etc) but also because of their use in heterogeneous systems of all sorts and their interaction with the real world ("cyber-physical systems"). Over the past five decades, researchers and developers have been creating abstractions that help them design in terms of their design intent rather than the underlying computing environment and shield them from the complexities of these environments. To cope with the new level of system complexity, the challenge is to create abstractions of the problem space that express designs in terms of concepts in application domains, such as telecom, aerospace, healthcare, insurance, and biology.
These systems also embed more and more programmable or reconfigurable devices, therefore an increasing impact of software. Software integration becomes THE challenge of embedded systems. Most of the costs during the development phase are due to the correct mapping of software on the hardware and to the validation and verification of the complete system, especially for real-time embedded systems. Those costs are closely related to the capability to have an efficient global design and realization (hardware and software, and matching of both), a correct validation of the design according to the specifications all along the design process, including formal techniques, prototyping or simulation.
<Adding a paragraph on the specificities of Saclay's area : AP T. C.>
Scientific challenges for future embedded systems are thus:

- Designing and validating complex software on heterogeneous multi-core architectures,
- Creating new tools to facilitate design and validation techniques in order to increase capability of managing complexity, performance and quality (including safety and security) of future software and hardware embedded systems.
- Developing new applications and usages of embedded systems using the last innovations in embedded system technologies.

To support these scientific objectives in this highly competitive domain, the innovation community needs to set up and use beyond state-of-the-art methods, equipments and tools.

Therefore, the aim of the proposed platform is allowing the scientific community to bridge the gap of the validation of embedded software and to scale their results to real-world industrial constraints.
The proposed equipment will offer a set of integrated, coherent, complementary high quality tools: (1) supporting the design, realization, verification, validation and experimentation of software, new applications and usages on a diversity of embedded system hardware, (2) allowing the development and evaluation of new concepts, architectures, tools, methods and processes along the whole life cycle (from early specifications to design, conception, maintenance and evolutions of embedded systems).

These tools are both software and hardware accelerators that will be located in the very center of the "Design and integration center of NanoInnov", in Saclay's area.
<introduction nanoinnov/digiteo: AP T. C.>

This unique platform will be composed of software engineering tools (modelers, virtual platform, design chains, provers, compilers), hardware modeling the system or its environment in all the phases of the "V" cycle, all that supported by high performance hardware accelerators. Its differentiating features are: (1) synergy between all the tools, with gateways that allow smooth transition from one phase to another, from model based engineering to code or hardware debug, (2) High Performance Computing-like accelerators allowing fine grain simulations and validations on very large systems (up to 100's of millions of gates), (3) hardware support for real simulation (of parts) of a systems or its environment.
Indeed, the realization of complex embedded systems is quite a mature domain and the improvement ways now lie in the better interaction of the various phases and how to scale up to bigger heterogeneous systems, improving the global result and reducing the time between early specifications and prototype validation.

Therefore, the proposed platform will enable system designers to validate new software on multi-core heterogeneous hardware (that can still be under development) on a scale that they cannot reach without the platform, and to and quickly design, implement prototypes. It will allow researchers to validate new methodologies of design, of verification and validation, checking that they really scale to real systems.
Due to the proximity of the platform, it will create synergies between software and hardware communities, between researchers in methodology and end-users, between research and industrial world, creating therefore an ecosystem around it.
Last but not least, it will allow the research community, with a minimum of efforts and time, to continue developing systems, architecture, processors that are matching the complexity of industrially realized systems, and not oversimplified "toy" examples.

More precisely, on the software side, the platform is composed of high level modeling software such as Scade, Modelica, Mathlab, Simulink, complemented by tools and software provided by the partners, and other validation tools.

But software only solution to the challenges is not enough anymore because of (1) the exploding increase of complexity and of use cases, (2) the difficulty to realistically simulate interactions with the physical world and (3) the prohibitive execution time of software only simulations and validations of complex systems. It is why this platform will essentially rely for its hardware part on FPGA based accelerators and on a (small) compute farm also possibly with accelerators allowing to drastically improving emulations, simulations and validations.
These rather generic accelerators are complemented with domain specific resources. For example, for in the transportation domain, the domain specific resource will be a complete set of electric and electronic devices of a vehicle, allowing reproducing with greater realism the behavior of embedded systems and of a part of the vehicle environment.
The size of the platform should be such that it should allow a complete validation of a system in its environment, to reduce errors and uncertainties; therefore the hardware accelerator should be able to emulate systems of hundreds of millions of equivalent gates. Such hardware is available on the market, for example "Veloce" from Mentor Graphics or "Zebu-server" from eVe. The platform will offer to users a coherent view of all tools, with a transparent use of the accelerators, for all the phases of the "V" cycle.

The cost of such system is unreachable for most research laboratories, SMEs or even some more important companies. One of the aims of this proposal is to open the platform to the French scientific community, to SMEs and start-ups, and to companies that ask for it. The partners can bring not only their know-how and their tools, but also add-ons specific to their application domain. This platform should be able to generate an ecosystem around it, and, for example, hardware or software IPs libraries could be linked to it, easing even further the access to embedded systems technologies. It will help synergies between domains, creating new innovative embedded systems.

The platform being neural from application point of view, it can be used in all domains of embedded systems (transportation, security, aeronautics, communication, multimedia). It will evolve, either by integrating more tools together or by increasing it hardware part to support more complex and diversified systems.

1. ENVIRONNEMENT SCIENTIFIQUE ET POSITIONNEMENT DU PROJET D'EQUIPEMENT / SCIENTIFIC ENVIRONMENT AND POSITIONING OF THE EQUIPEMENT PROJECT

(4 pages maximum)

Etat de l'art national et international décrivant le contexte et les enjeux scientifiques dans lesquels se situe le projet.

Inclure les références bibliographiques nécessaires en annexe 7.1.

Embedded systems are at the heart of everyday's life devices like mobile phones, cars, planes, medical devices, payment machines, etc. They are the core of the digital economy, which is now about 10 % of the world GDP. To bring even more functionalities to the users, their complexity is increasing over the years, correlated with an explosion of their development costs.

<Adding the industrial position of France and Saclay's area in embedded systems. AP: T. C.>

The aim of the platform is to allow the scientific community to develop software and hardware architectures, methodologies and tools that decrease the cost of building new embedded systems, integrated or not and add new applications domains. One essential challenge the embedded community is facing now is related to the design and validation of software on parallel embedded hardware platforms (either in the same package, like SoC - System on Chip –, or on the same board, or distributed like the ECU - Electronic Control Units - in a car). Figure 1 shows the ratio of software in the development cost of products according to technology node. It is nearly 70% of the global cost in 2014 for the smaller technology nodes that are used to build the most complex SoCs. As it can be seen on

Figure 2, most of the costs are related to the verification phase, and of the validation of the software.

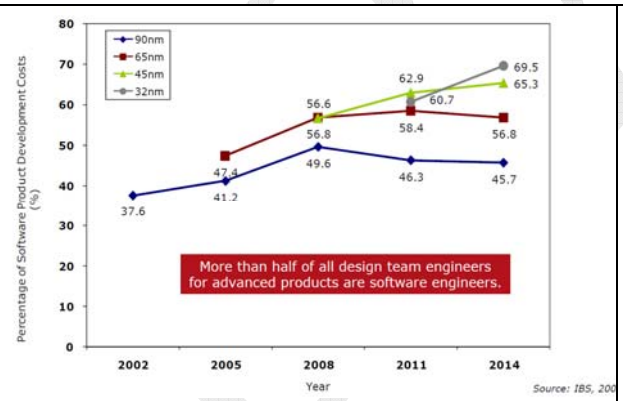

Figure 1: Ratio of software in complete product development costs

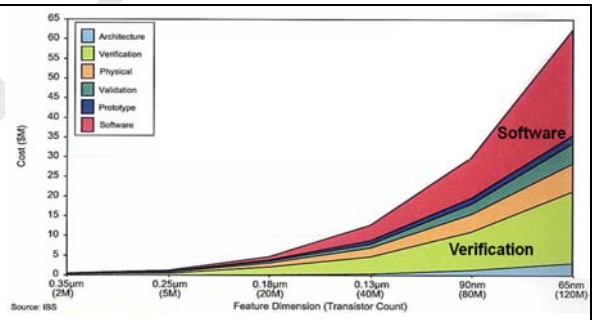

Figure 2: Split of development costs

It is therefore of paramount importance to reduce these costs that will limit the diversity of systems and the number of companies that can afford to make such expensive investments to deliver a product. Each error in the software or found during the verification delays the time to market of the product, and endangers the market place of the company.
A key element to solve the challenge is to have a good methodology and tools that allow finding problems as early as possible in the design chain.

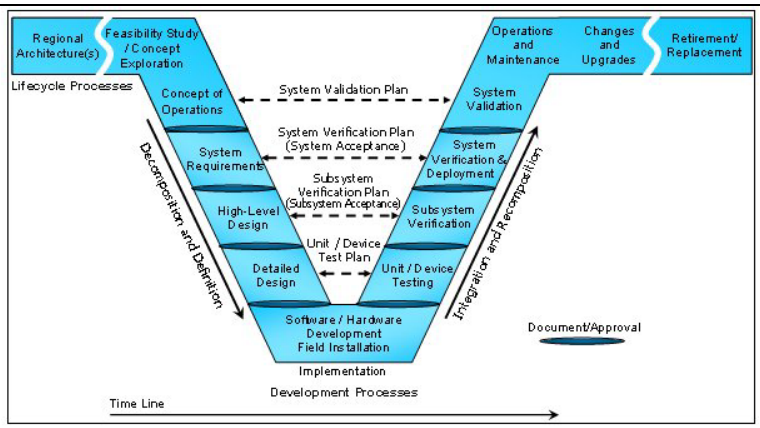

Figure 3: the "V" cycle (from xxx)

There are several initiative that try to solve (part) of the problem, and they follow the “V” cycle (see Figure 3) [Add reference].
Model-Driven Engineering offers an approach that alleviates the complexity of platforms and express domain concepts effectively [schmidt2006]. It is also important that the flow avoids as much as possible manual rewriting between phases, for example between an algorithm written in Matlab/simulink and its implementation in “C” for the final product. Manual translations are always error prone and correcting all the chain up to the specifications when a bug is found is tedious and not always easy. Therefore it is important to have a “unified” environment where all the phases of the “V” cycles are smoothly integrated with a maximum of automated translations. Ideally, the same high level specification will be enriched during the various phases to generate the functional code, the mapping, the validation suite, etc. This approach also help communication between the various teams involved in the design and is pursued in the proposed platform by its capacity to completely support complex embedded systems development, evaluation and validation, allowing a better synergy between embedded software, architecture and design of systems.

The complexity of embedded software is further increased by the underlying hardware architectures involving heterogeneous multi-cores. Already present in the embedded domain for long time, it is now the major paradigm for general computation as well. The race for speed has ended and the gain of performance is now by multiplying cores (“multi-core” and “many-cores” architectures) [Add reference]. To further increase power efficiency, coprocessors are often added, resulting in heterogeneous multi-cores architectures, theoretically very efficient but substantially increasing the complexity of the software, that need to be partitioned and parallelized on resources of various nature [Add reference]. Some techniques, like virtualization[Add reference] , allow to reduce the complexity for the programmer, but the overall problem of validating (efficient) software on those architectures is still a major challenge for the coming years. It is a clear objective of the proposed platform to be a tool for the research community to find new solutions to these challenges and to validate them on real case applications.

However, for real system, the complexity is such that its simulation or emulation requires High-Performance-Computing-like capabilities to be able to validate the software in a realistic simulation of the target hardware [Add reference]. Besides compute farms, that are practically limited to model high level abstractions of the hardware, most of the high performance systems use more dedicated hardware like FPGA to mimic accurately the target underlying hardware.
Those accelerators are available from several companies like Mentor (Veloce), Cadence (Palladium), Synopsis (HAPS), eVe (Zebu), …

One development in that field that emerged from the Berkeley Wireless Research Center of UC Berkeley is the RAMP system, now a product under the name BEE. Its target is mainly to

accelerate the validation of algorithms on systems. Their latest product, BEE4 is perfect for both high-speed RTL verification and real data rate system integration and validation. It is based on Xilinx Virtex-6 FPGAs, up to 500 MHz and with a fast interconnect system.
It directly addresses[Add reference]:

- LTE+ Digital and Mixed Signal Communication Designs with multiple integrated DAC/ADC components.
- High Speed Multi-core SoC Design Verification and Exploration, including Hypervisor based designs.
- Specialized Networking Chipset Prototyping including PHY chip designs, packet inspection, encryption IP, routers, etc.
- Application Processor designs with integrated high-end HD capability.

Figure 4: picture of the BEE4 platform

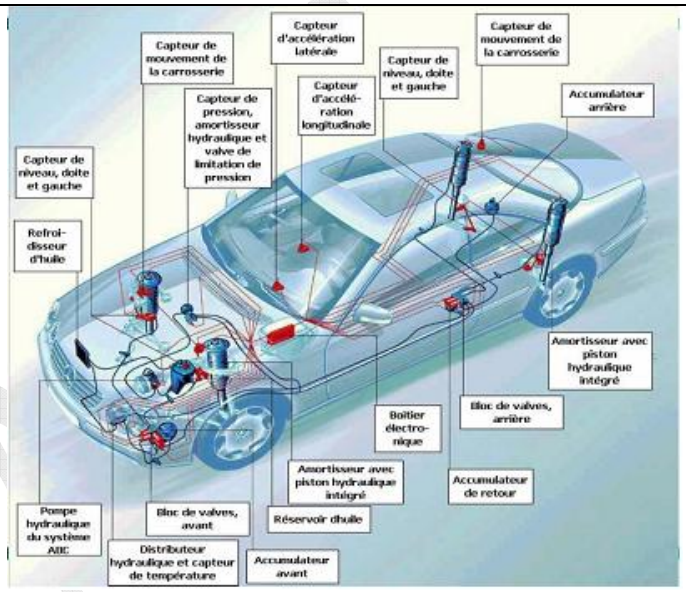

Figure 5: An example of complexity in the automotive domain : active suspension

This acceleration of simulation, validation is currently a hot topic in the scientific community, for example the following proposal of CMU/Berkeley ([Chiou]):
Derek Chiou from UT, James Hoe from CMU, and John Wawrzynek from Berkeley, *"are writing an NSF proposal entitled FAbRIC (FPGA Accelerator Research Infrastructure Cloud). The proposal is to acquire many high-end FPGA platforms connected together with high-speed Infiniband and/or FPGA-to-FPGA interconnect, CAD tools and high-end servers to run them on, and intellectual property (MPI interfaces to FPGAs, DRAM controllers, etc.) all to be placed in a supercomputer center and made available to the research community, free of charge."*
They are *"asking CAD tool vendors to provide their tools and to maintain those tools for free in exchange for all code compiled/processed by those tools to be made open. This rule will not only eliminate tool costs from the proposal, it will also result in a large amount of openly available FPGA code.*
Various usage models are possible. A transactional memory researcher could implement a TM machine from scratch or use various IP blocks already available. Another TM researcher could use the source code as a basis to improve the original work and thus be able to compare directly to the original. A software researcher could check out the FPGA configuration (bit) file for that TM and develop code for it without touching the RTL."

The aim of their NSF proposal shares some similarities with our proposal, except that our proposal wants to cover complete conception cycle, uses Model-Driven Engineering and addresses more particularly the validation of embedded software on new hardware architectures

(distributed or not heterogeneous multi-cores). It will also differentiate with the inclusion of specific hardware environments that will allow testing the embedded system in “nearly” real conditions and enabling research in the field of reliability.
The automotive example is very interesting in this context. Most innovations in recent vehicles come from electronic systems: the share of electronics in the cost of modern cars can reach up to 40% (some cars have up to 80 ECU – Electronic Control Units), and (according to car manufacturers) electronic systems are responsible for 35% of all failures [Add reference].
In modern cars, most ECUs are equipped with diagnosis functions, although sometimes very simple such as periodic data logging. But diagnosis is not extended to other electronic organs, such as sensors, actuators, cables, and complex functions distributed on several control units cannot be extensively diagnosed. Furthermore, cables can be a great source of electric problems in modern vehicles, which now hold up to 4 km of cumulated length. It has been recognized by OEM (Original Equipment Manufacturers) that 70% of ECUs returned for expertise were diagnosed free from defects: in these cases the faults were due to connectors and cables [Add reference]. The proposed platform will provide an environment that will represent the physical environment of the embedded systems – here ECUs – allowing investigating, and testing new methods coping with those problems.
In this automotive case, the embedded system of a car will be mapped on the proposed platform with (1) a toolset using Model-Driven Engineering, (2) hardware accelerators allowing to test and validate in accurate conditions the ECU software even if the ECUs are still under development (thanks to FPGA accelerated simulation, or to In Circuit Emulation – ICE- “plugging” a virtual chip on a circuit board) in (3) an accurate modeling of the car environment (wiring, actuators, sensors).

As a summary, the proposed platform will fulfill several uses:

- It will allow fast and realistic (because connected to accurate hardware models/emulators) validation of embedded software (from deeply embedded software up to application software),
- It will allow evaluating and scaling to real-size new applications or enabling novel use of software and hardware embedded systems. (For example, a control engineer can validate on real scale equipment a new control algorithm he is designing, or a research laboratory can use the system to validate a new image processing application),
- It will allow to co simulate hardware and software, and to integrate embedded system under development in their real environment.
- It is a research environment allowing elaborating new tools, methods and processing covering all stages of the design cycle, “from specifications to realization”.
- It will enable very fast exploration of new embedded systems concepts, by accelerating the validation of concepts and the exploration of the design space.
- It will also help education, either by its direct use or by the synergies between tools of various domains, creating inter-domain communication.

2. DESCRIPTION SCIENTIFIQUE ET TECHNIQUE / TECHNICAL AND SCIENTIFIC DESCRIPTION OF THE ACTIVITIES

2.1. ORIGINALITÉ ET CARACTÈRE NOVATEUR DU PROJET D'EQUIPEMENT/ORIGINALITY AND INNOVATIVE FEATURE OF THE EQUIPEMENT PROJECT

(2 pages maximum)

- montrer comment l'équipement permettra de mener des projets innovants par rapport aux recherches communément menées par chacun des partenaires,

- montrer comment le projet d'équipement vise à structurer des partenariats académiques mais aussi public – privé,

- montrer comment la valorisation des résultats de la recherche conduite grâce à ces équipements constituera un enjeu majeur pour les partenaires,

- expliquer précisément comment la pluridisciplinarité et la complémentarité du rôle des partenaires ainsi que leur positionnement territorial, national et international pourront être considérés comme des éléments forts en appui au projet.

Currently, all the phases of definition, specification, design, verification, validation and test of the "V" cycle are done with a set of disconnected tools and methods that impose extra coding or translation phases. The validation of the software and of the hardware is generally done independently, leading to undiscovered errors and delays in time to market during the integration phase, and therefore extra costs. The strength of the proposed platform is enabling research on unifying all the phases in a coherent methodology with integrated tools, assisted with accelerators allowing having results in a reasonable amount of time, while permitting in depth simulations. For example, the developer of an algorithm can quickly test it on hardware, with a nearly press-button approach that doesn't necessitate hardware knowledge. He could benefit of an accelerated simulation time and in a certitude that his software will run on the specific target hardware. Furthermore, the development of embedded software can start early and the debug can be done before the final hardware is ready, saving time and efforts. This is particularly important for research institutes, where algorithmic developments don't get easily feedbacks on the efficiency of their approach on hardware, and where architecture researchers have trouble implementing their research on real silicon due to cost, size and efforts required. Heterogeneous multi-core architectures are currently hot topics in the architecture community, but very expansive (and slow) to simulate/ emulate due to the silicon real estate they require (hundreds of millions of gate equivalent).
The platform will allow exploring next innovative territories for research: the bottleneck of complexity will be greatly lowered with the platform. For example, mapping and simulating an application on a highly parallel architecture with hundredth of cores will become feasible and easy therefore helping a large set of research in real-time distributed operating systems, middleware, task migration, cache design, interconnecting design, core architecture, etc.

Model driven design allows validating each step of the conception and realization phases down to a very low level, even for very complex embedded systems. It is naturally for this kind of systems that the cost of verification is the highest. The platform will allow developing new methodologies in that field, to marry techniques together, and to facilitate the communication between communities working on different steps of the V cycle

Working on all details of such complex systems is out of the scope of each of the partners alone: each one is more specialized in one part of the "V" cycle. Through the platform, all the tools will be integrated together allowing each organization to communicate more easily with the others and to validate and confront its ideas with the others. This synergy will be certainly very fruitful and will lead to developments difficult to imagine now. It will also help a closer work between the hardware and the software part of a project: due to its high simulation capability, the platform will

allow to run the real software on a detailed simulation of the complete hardware and its environment. The platform will also create new synergies between research communities in hardware architecture and in system and software engineering to develop new tools and tool integration. This will also facilitate research in new architectures, multi or many cores, SoC design, software, operating systems and their integration in order to support various applications. Besides, it will bring to research laboratories a set of state-of-the-art techniques to realize their own developments, prototypes and evaluations.

This real scale provided by the platform is something achievable with great difficulties by the partners alone (and also very expensive, here the cost of the hardware accelerators is “shared” by all users).

The targeted domains of the platform are (without specific order):

- Design of multi-core and many-core systems (software and hardware),
- Prototyping of applications, development and validation of algorithms,
- Early stage design of test / diagnosis / validation structures or services,
- Improved co-design of HW and SW systems,
- Embedded systems for automotive,
- Validation of secure real-time operating system,
- Vision systems (automotive, robots, home, security),
- Design and validation of (hardware / software) Intellectual Property blocks (IPs) and their validation in realistic conditions,
- Development of parallel programming tools,
- Command and control for engines and energy management,
- Wire test, diagnosis and reliability of systems or sub-systems,
- Etc.

The various partners of the proposal really complement each other:
<Give a list of all partners and what they bring to the proposal>

The platform will also facilitate fast transfer of research results, because they could be designed and validated far more easily. As confidentiality of the data will be ensured, it can also be used by companies or SMEs to decrease their time to market or make first time right products thanks to the realistic and complete validation environment provide by the platform.
By serving both the hardware and the software communities, it will act as a link increasing the cross fertilization between the various partners, and will establish stronger links between the users, mainly on the Saclay area because it will be a unique meeting point. It will also act as catalysis between academic and industrial research, due to the fact that they will share the same tools and same environment. It will be the heart of an “embedded system ecosystem”.

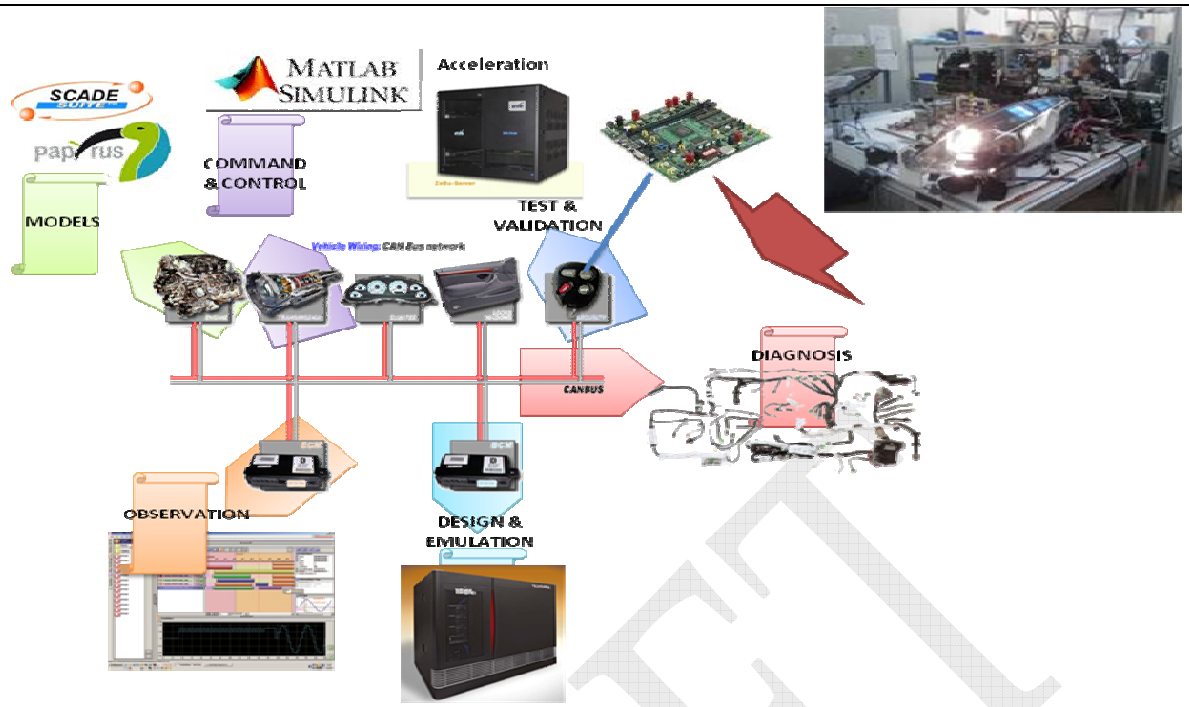

Figure 6: Schematic organization of the platform

2.2. DESCRIPTION DU PROJET / DESCRIPTION OF THE PROJECT

2.2.1 PRESENTATION SCIENTIFIQUE DU PROJET/SCIENTIFIC PROGRAMME

(6 pages maximum)

- préciser le positionnement du projet -national et international- vis-à-vis des projets et recherches concurrents, complémentaires ou antérieurs…

- indiquer si le projet s'inscrit dans la continuité de projet(s) antérieur(s) ou est lié à un ou plusieurs projets devant démarrer, ainsi que leur articulation. Dans ce cas, présenter brièvement ces projets ainsi que les résultats acquis. S'il s'agit d'un nouveau projet, montrer comment il s'articule avec les projets en cours ou devant démarrer.

- présenter un bilan des recherches menées par le(s) partenaire(s) (donner, en autre, des éléments chiffrés et la bibliographie à mettre en 7.2).

- dans le cas d'une action pluridisciplinaire, expliciter l'articulation entre les disciplines scientifiques et leurs apports respectifs.

- les objectifs scientifiques et techniques du projet. Présenter l'avancée scientifique attendue. Préciser l'originalité et le caractère ambitieux du projet, et dans ce cadre, préciser l'apport de l'équipement demandé.

- définir la manière dont l'équipement demandé pourra contribuer à une avancée scientifique significative (préciser la nature de cette avancée).

- le détail des verrous ou aléas scientifiques et techniques à lever par la réalisation du projet. Expliciter la démarche scientifique pour lever ces verrous (programme de travail).

- présenter les résultats escomptés en proposant si possible des critères de réussite et d'évaluation adaptés au type de projet, permettant d'évaluer les résultats en cours et en fin de projet.

- indiquer les avantages économiques qu'apporterait l'équipement demandé.

This domain of embedded systems is of paramount importance for France, because of its implications in economy, industry, security and defense and many academic researchers are also working in this domain.
To our knowledge, this platform will be unique in France for the scientific community because of its power, its accessibility for research labs and SMEs, how it could evolve and its capacity to address state-of-the-art research topics and complete embedded systems. Thanks to its large software toolset, it will cover a large part of the "V" cycle, unlike existing systems like BEE (Berkeley) more focused in the application development, Veloce or other platform of EDA providers restricted to SoC validation, etc. It is the synergy between all its elements that makes it different. For example, semiconductor manufacturers already have FPGA based accelerators, but they are only used to emulate and verify the hardware of System on Chip, not complete (discrete) systems including application software, OS and middleware, and their systems are not accessible by the scientific community or SMEs. The proposed methodology is generic, and could be applied to different application domains. It also has specific hardware for mimicking a real environment (e.g. for automotive applications).

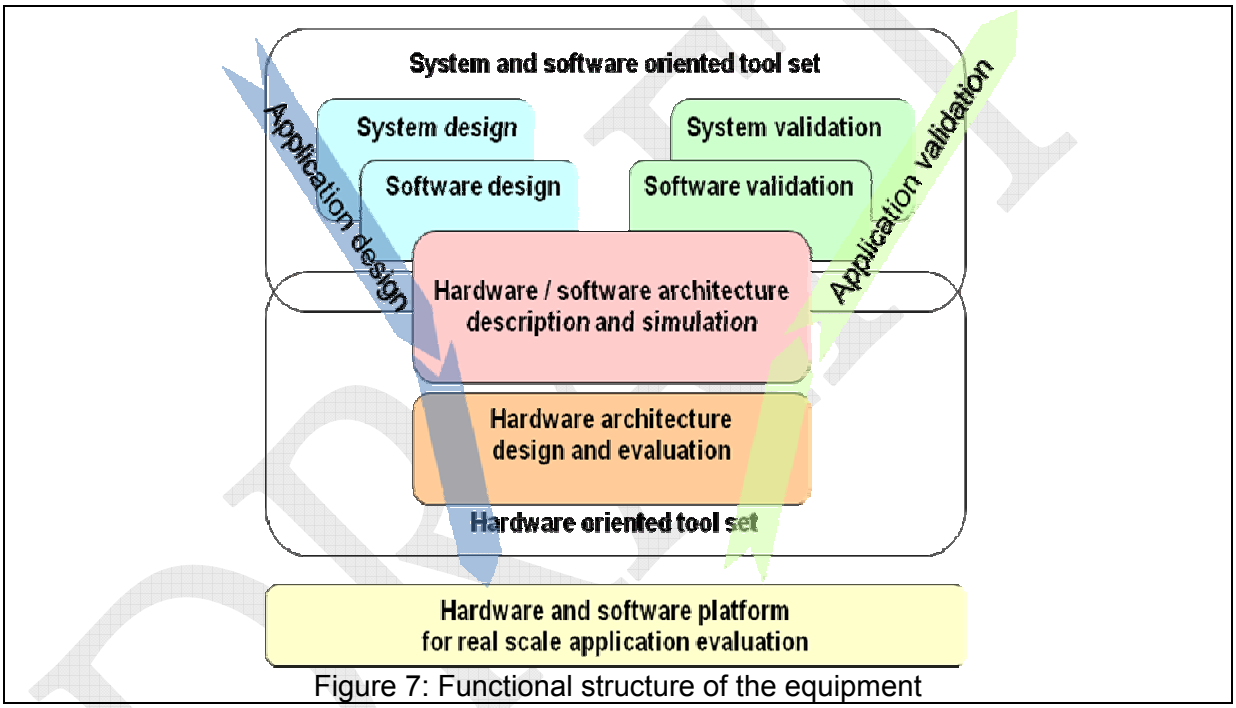

Figure 7: Functional structure of the equipment

The platform will be composed of:

1. Modeling tool suite for embedded system design including global views of the system, software oriented views and hardware architecture oriented views,
2. Tools for research on new approaches for system and software engineering,
3. Validation tools to validate the design models and implementation against the system requirements,
4. Virtual platforms and a framework to ease the development of new virtual platforms to provide software/hardware co-simulation,
5. A cluster of processors (processor farm) to run the software tools, simulators and to interface with the FPGA based accelerator, possibly also supporting dedicated accelerators boards,
6. FPGA based accelerator for hardware architecture emulator to support co-verification hardware/software of complex system up to several hundredth of millions of gates,
7. Application related hardware to provide real scale evaluation on use cases of the benefit of the new design, validation and architecture solutions built thanks to the equipment and

upon it. It will serve also as representative of industrial target to develop and validate advanced control laws.

The system and software design tool suite has to fulfill the following essential requirements:
- for validation of embedded software, it has to be compliant with tools widely used and to offer an ease of use (for example, in hiding the hardware acceleration for the software developers).
- for research on system and software engineering, it has to be based on easily extendable technology allowing to experiment new concepts with a user friendly access and a low cost of implementation.
- to give access of industrial solutions to facilitate technology transfer and real scale evaluations.
- it has to ensure interoperation with the main industrial technologies and all the exploratory technologies built by the laboratories of the project.
- For the hardware modeling, it should have the capacity of reusing existing hardware component models and their storage in a large and open library together with a very high level of performance and of flexibility.

The need for more accurate and wide range diagnosis systems is then essential, and this kind of system must be designed and tested in conditions as close as possible to real life. For example, as new car technologies are emerging (hybrid and electric vehicles holding new electric and electronic systems), this need will be more important. The maturity of the existing work now requires new tools to help:

- Validate the assets and ensure the update of knowledge in adequacy with the rise of new technologies,
- Accompany mechanics in their daily work by the development by dedicated diagnosis equipments,
- Reduce the intervention costs by a widening of the diagnosis capacities and by developing a systemic analysis method of faulty subsystems in the vehicle,

Provide training infrastructures for present and future maintenance and repair operators. This platform will provide such a environment, which will be used for several purposes: design diagnosis and maintenance systems or functions along with the system to be diagnosed ; integrate the results of the various academic teams working on this field ; test and validate these systems in real environment ; train maintenance and repair operators to use these new tools.

In general, the synergies of various activities around the platform will help cross-domain fertilization. Directly, it is planned to have seminars about the platform and its various tools to increase awareness or each domain involved.

On the economical side, the benefit of the platform is the cumulative result of integrated methodology, reducing errors as early as possible in the “V” cycle, and powerful computing/simulation platform. The hardware part of the platform form a dedicated High Performance Computing Platform dedicated to the simulation/verifications of embedded systems. According to a study from IDC, 97% of firms using high performance computing declare that they give them a clear competitive edge. In the 80’s, Boeing aerospace had to built more than 70 wings to validate the reliability of a plane. Now, thanks to high performance computing, they only have to test about 10. It is an extraordinary gain in time and cost. An investment of 1 dollar in High Performance Computing (in the military domain), produces a gain of 7 to 13 dollars [supercomputers].

The partners of the proposal will not always use the complete platform: some will be interested in particular aspects (high level modeling or reliability, or defining new compute models for multi-cores, or defining new embedded systems, etc), but they can easily access to the rest of the resources allowing them to focus on their knowhow and to have a better understanding of the others parts.

This platform will be an enabler that will remove current bottlenecks in research topics.

<Presentations of the partners' activity be squeezed in 4 pages to fit in the page budget with the following recommendations:
- Don't forget the educational aspect

- indiquer si le projet s'inscrit dans la continuité de projet(s) antérieur(s) ou est lié à un ou plusieurs projets devant démarrer, ainsi que leur articulation. Dans ce cas, présenter brièvement ces projets ainsi que les résultats acquis. S'il s'agit d'un nouveau projet, montrer comment il s'articule avec les projets en cours ou devant démarrer.

- présenter un bilan des recherches menées par le(s) partenaire(s) (donner, en autre, des éléments chiffrés et la bibliographie à mettre en 7.2).

- dans le cas d'une action pluridisciplinaire, expliciter l'articulation entre les disciplines scientifiques et leurs apports respectifs.

- les objectifs scientifiques et techniques du projet. Présenter l'avancée scientifique attendue. Préciser l'originalité et le caractère ambitieux du projet, et dans ce cadre, préciser l'apport de l'équipement demandé.

- définir la manière dont l'équipement demandé pourra contribuer à une avancée scientifique significative (préciser la nature de cette avancée).

- le détail des verrous ou aléas scientifiques et techniques à lever par la réalisation du projet. Expliciter la démarche scientifique pour lever ces verrous (programme de travail).

- présenter les résultats escomptés en proposant si possible des critères de réussite et d'évaluation adaptés au type de projet, permettant d'évaluer les résultats en cours et en fin de projet.

- indiquer les avantages économiques qu'apporterait l'équipement demandé.

>
<Summarize CEA LIST in no more than 1.5 pages. AP: T. C.>

CEA/LIST/DACLE/LCE is developing parallel architectures with dynamic resources management. Due to the architectures' complexity, only abstract prototypes can be built to validate the new concepts before chip design. Also, the inability to deal with accurate hardware model during early software development process prevents its performance optimization. Besides, those high level simulations take hours, preventing a complete Design Space Exploration. The platform will enable to run simulations several orders of magnitude faster, and with more accuracy. Design Space Exploration technique for optimization will become affordable in simulation time. The increase of simulation performance will allow moving the architecture from "multi-cores" to "many-cores", i.e. allowing handling large number or processing units working and communicating in parallel. LCE is also developing highly parallel programmable architectures for vision. The platform will allow to emulate the architectures and to test them with real applications, therefore analyzing what could be further improved.

<Reference of the papers at the end of the proposal>

CEA/LIST/DILS/LISE is developing tools on new approaches for system and software engineering. The modeling core tool **Papyrus** has been supported by numerous projects as FUI Usine Logicielle, FP7 ATESST, FUI Lambda, FUI EDONA and FUI TopCased creating a convergence of developments of the research and industrial community around this open

implementation. ***Papyrus DSL builder*** provides very advanced customization features to exploit intensively and easily the paradigm of language profiles. It allows formalizing the language extension/specialization and the domain and context to which they apply (meta-models and constraints). ***Papyrus modeler*** will come with already operational integration of Papyrus SysML modeler to SCADE performed in the context of the LISTEREL join laboratory among CEA LIST and Esterel Technologies. Initial implementations of the MARTE profile and specialization for scheduling analysis issued from FP7 project INTERESTED and FUI project EDONA will be provided as input for the equipment.
It is expected to add new features during the lifetime of the project:

- ***IP-XACT*** specialization and model transformation to provide integration of the hardware simulator and emulators. It will integrate results from Nano 2012 projects driven by STMicroelectronics and conducted by both CEA LIST and INRIA
- ***Usage profiles*** for SysML and MARTE and model interfaces to Simulink and Modelica.
- Model import services from usual commercial UML tools (at least: RSA, MagicDraw and Enterprise Architect)
- Documentation and C/C++ code generators including behavioral aspect for dedicated SysML and MARTE sub-profiles
- Model sharing and model revision management

CEA LIST proposes to integrate several verification/validation tools in the platform for embedded systems. One of the important features of embedded systems is that they generally include lots of numerical computations, in particular in control of physical apparatus (plants, airplanes, automotives etc.), and specific static analyzer have been designed to help track bugs, and check for functional properties, such as the abstract interpreter FLUCTUAT (which also tracks discrepancies due to the use of finite precision arithmetic), the program prover FRAMA-C, or **ALCOOL**, a static analyzer for asynchronous concurrent systems, from specifications to programs. Its second prototype is currently completed in the ANR Project PANDA, with a particular involvement of end-user Airbus France. The aim of the analyzer is to be embedded in the platform, at the level of high-level system verifications (proving coherence of these).
These tools form a coherent choice for being incorporated in a platform for embedded systems, if some more maturation is performed. For instance, most of these analyzers take C (or ADA) code as input, and complete integration with higher-level description languages such as SCADE or Simulink are only sketched, requiring in particular a lot of engineering work. <Discuss if the maturation is in or out of the proposal>

CEA/LIST/DILS will also propose a **Diversity framework:** this framework is based on symbolic execution of the model depending of various analysis objectives and provides the tree of the execution paths implicitly specified by the model. This technology is used for example to generate conformance testing, or simulation scenarios or to verify some safety related properties on the models. Initial integration with Simulink developed in the FUI project EDONA and Eureka project SysPEO with automotive partners (namely Johnson Control and Delphi) will be provided. The framework will be extended by enhancing the Simulink integration, developing integration with SysML and MARTE models. Research on this topic have already be started in the FUI project Usine Logicielle and ITEA 2 project VERDE projects, providing the initial specifications for a first step development. The tools will be provided as common source for the academic project partners in order to ease research related evolutions and adaptations.

CEA/LIST/DILS/LSL is proposing virtual platform environment based on **UNISIM.** It provides several virtual platforms and a framework to ease the development of new virtual platforms. Most of UNISIM virtual platforms are full system simulators, which means that they are sufficiently representative of the real hardware that whole operating systems (e.g. Linux, VxWorks), unmodified software stacks (e.g. an AUTOSAR software stack), and industrial applications can run on them.

The UNISIM virtual platforms are modular: a simulator is the assembly of properly configured simulation components (e.g. CPU, RAM, buses). They are written in C/C++ and based on industry standards, like IEEE1666TM, OSCI SystemCTM and OSCI SystemCTM TLM 2.0.
Some possible use cases of UNISIM virtual platforms on the equipment are:

- Development of SystemC IP (intellectual property) development and new virtual platforms: UNISIM is an open development environment that provides a SystemC module library, and a set of services (debugging, program loaders …). UNISIM can act as a base for the development of new SystemC IPs and new virtual platforms on the equipment.
- Hybrid virtual platform: UNISIM/systemC and the FPGA accelerator can be used together to build hybrid virtual platforms: e.g. microprocessors cores under UNISIM/SystemC, and specialized IPs/devices prototyped on the FPGA accelerator. The hybridization allows using indifferently of IPs in UNISIM/SystemC or in VHDL for th FPGA accelerator, but also to increase simulation speed of very large systems.

Several open source virtual platforms for different targets (ARM, PowerPC, Star12X, and TMS320C3X) and different hosts (Linux, Windows, Mac OS X) are available. These virtual platforms have been evaluated and used in various industry domains such as automotive, avionic, military, electrical equipments for medium tension, nuclear safety.

CE/LIST/ is working on the development of systems for the electric vehicle, where the energy storage/recovery is one of the biggest scientific challenges. It permits to augment the capacity in autonomy of the vehicle. Then, an optimal energy management is needed and is realized thanks to the synthesis of intelligent predictive control laws.

In the national scope, three projects can be quoted here. “Vel-Roue” is a project of electric vehicle with motorized wheel. This project involves MICHELIN, RENAULT companies and the IFP institute amongst the different partners, and proposes to test a concept of commercial vehicle. The project called “VEGA-SYTHER” deals with the problematic of electric vehicle with a high efficient autonomy thanks to the use of a thermal management system. MICHELIN, SAINT GOBAIN SEKURIT, CNRS and INSA Lyon take part of this project. The “MOVEO-DEGE” project is dedicated to the study of the safety risks analysis and the environment protection. It involves a technological platform which is able to model and characterize in performances, robustness, life cycle and failure modes, different electronic and mechatronic components of the vehicle when reproducing its conditions of normal operations.

The use of this platform proposal is highly focused on the development of the electronic hardware for the control of electric vehicle, as well as the associated laws for regulating its energy flows.

The recent emergence of this type of project encourages the big vehicle manufacturers to pass through a commercial deployment phase of their electric vehicle in the next years. Renault company foresees to sell its electric Kangoo ZE-Concept and Scenic ZEV-H2 vehicle in 2011 and 2020. To meet demand, some companies propose some technical and hardware assistances for the deployment of this car fleet.

In that sense, this platform proposal, which gathers together research institutes and companies, has for ambition to develop efficient ways of modelling and controlling the powertrain system of innovative vehicle.

This test bench will progressively integrate the different components present in the powertrain and auxiliary systems of the vehicle under several conditions: virtual (software model) and hardware (“Model In the Loop” and “Hardware In the Loop”) according to different objectives (design, test, validation). This experimental bench will enable the design and validation of a hierarchical control system for the electric vehicle. Issues relating to the low-

level motor control, the supervision of power components, the regulation of the energy flows within the whole engine and its link with the environment, as well as the Man-Machine interface, will be investigated.

Coupled with a real size mockup of the entire electrical and electronic architecture (EEA) of a given system (e.g. a car, truck or part of a plane), this tool will provide very interesting and productive environment for several activities such as:

- Design of the system or sub-system under real life constraints, together with additional structures or services dedicated to validation and maintenance phases,
- Integration of the various sub-systems in a real operating system, with real life communications and healthy / faulty functionalities,
- Validation and test of the system or sub-systems under environmental conditions as close as possible to real life operational conditions, possibility of inserting faults or defects in various parts of the system and observing the behavior of the sub-systems under design, possibility to observe and acquire various signals coming from or going to the sub-systems under design,
- Validation and test of the operating system and application software under the same operational conditions.

One of the main interest in this part of the platform is the possibility it provides to submit the system or sub-system in an operating environment very similar to the real life environment. This will help taking into account some potentially difficult constraints as soon as the early modeling and design phases and test the first prototypes very soon in the V cycle for incremental validation under real life conditions.

Figure 6: Electronic integration platform for automotive application

Telecom/ParisTech is working on **RAVENSCAR:** The Ravenscar Profile is originally a subset of the Ada tasking model, restricted to meet the real-time community requirements for determinism, schedulability analysis and memory-boundedness, as well as being suitable for mapping to a small and efficient run-time system that supports task synchronization and communication, and which could be certifiable to the highest integrity levels. This concurrency model can be adapted to other programming or modeling languages. For instances, it has been successfully adapted to the Real-Time Specification for Java. Being compliant to the Ravenscar Profile allows being consistent with the use of tools that allow the static properties of programs to be verified. Potential verification techniques include information flow analysis, schedulability analysis, execution-order analysis and model checking. The Ravenscar Profile has been used in conjunction with modeling approches in several european and french research projects such as FP6/ASSERT or ANR/Flex-eWare.
The aim of this component for a Ravenscar oriented support (and possibly other approaches to design partitioned high integrity systems) is to ease the methodology use, evaluation and

refinement by setting up interface among common modeling tools and various code generators. It will provide translation of MARTE models built in the Papyrus modeler into AADL models and code generation from AADL models [Faugere & Cie]. The code generation will be also considered as a model to model transformation in order to ease high level evolution and adaptation of the code generator and to ensure independency with textual specific technologies. For that it will expose a set of transformation rules that the users can assemble or overload as he want to adapt the code generation. Two target languages will be supported: Ada (according to RAVENSCAR style) and C (according, for example, with MISRA style). They will be formalized through meta-model to ensure as much as possible the homogeneity of the technologies and approaches used to manipulate the design models and the implementation code. They will ensure that even with small modifications of the generation code strategy, the structure of the code generated will remain correct.

<Describe the activities of the partners and how they could benefit from the platform to progress in their research>

Model-X xxxx tbc by Supelec xxx
RT-fUML simulator xxx tbc by CEA & Supelec xxx
Model based simulation support: In addition to the support of modeling activities, the MDE case tool will provide facilities to perform model based simulations with particular attention of ability to exploit various Models of Computation and Communication (MoCCs).

ENSTA has developed a very active research in embedded systems for the past 10 years and has developed fully automatized multiobjective design space exploration techniques on FPGA platforms for complex SOC and since 2006 for embedded manycores. For the time being, the team has developed the largest embedded multiprocessor in the world on an EVE ZeBu server based on 255 FPGA devices.

ENSTA has been a partner of the TERAOPS project from System@tic cluster(http://teraops-emb.ief.u-psud.fr/) and is currently a partner in the project MPSOCEXPLORER of the System@tic clusterwhich includes Eve and Arteris companies.

Description of the contribution and the use of the platform.

ENSTA wish to contribute to the platform EQUIPEX (SYSEMBEX ?) through:

1. Automatic design space exploration flows for homogeneous and heterogeneous multicore SOC with execution on FPGA platforms (intensive experience)
2. Multicore IP templates with HLS based generation of hardware accelerators,
3. NOC synthesis tools.

ENSTA wish to use the platform to pursue its strategy of fully automatic design flows for complex SOC and manycores:

1. Multicore/manycore architectures
2. An extension of current work would consist in moving up in abstraction and consolidate work done around synthesis form SysML/UML (CEA LIST)
3. Applications for advanced electronic systems based on multicore in the automotive sector(AUTOSAR)

2.2.2 STRUCTURE ET COMPOSITION DE L'EQUIPEMENT /STRUCTURE AND BUILDING OF THE EQUIPMENT

(2 pages maximum)

Décrire en détail l'équipement faisant l'objet de la demande, en indiquant, le cas échéant, la localisation d'équipements de même nature en France ainsi que dans les autres pays européens.

Pour la description décomposer, autant que de besoin, l'équipement en éléments constitutifs pouvant être distingués par leurs caractéristiques. Pour chacun de ces éléments constitutifs, vous préciserez :

- *s'il s'agit d'un nouvel équipement complet*
- *s'il s'agit d'une première tranche d'un nouvel équipement, en précisant alors comment et quand cet équipement sera complété*
- *s'il s'agit du remplacement partiel ou complet d'un équipement en place*
- *s'il s'agit d'une extension d'un équipement existant*
- *la(les) localisation(s) prévue(s) de l'équipement (mono-site ou multi-site)*
- *les éléments relatifs à la maturité technologique des équipements*
- *les indications relatives au respect des standards et normalisations existants.*

- *Elément 1/ Element 1*
- *Elément 2/ Element 2*
- *Etc.*

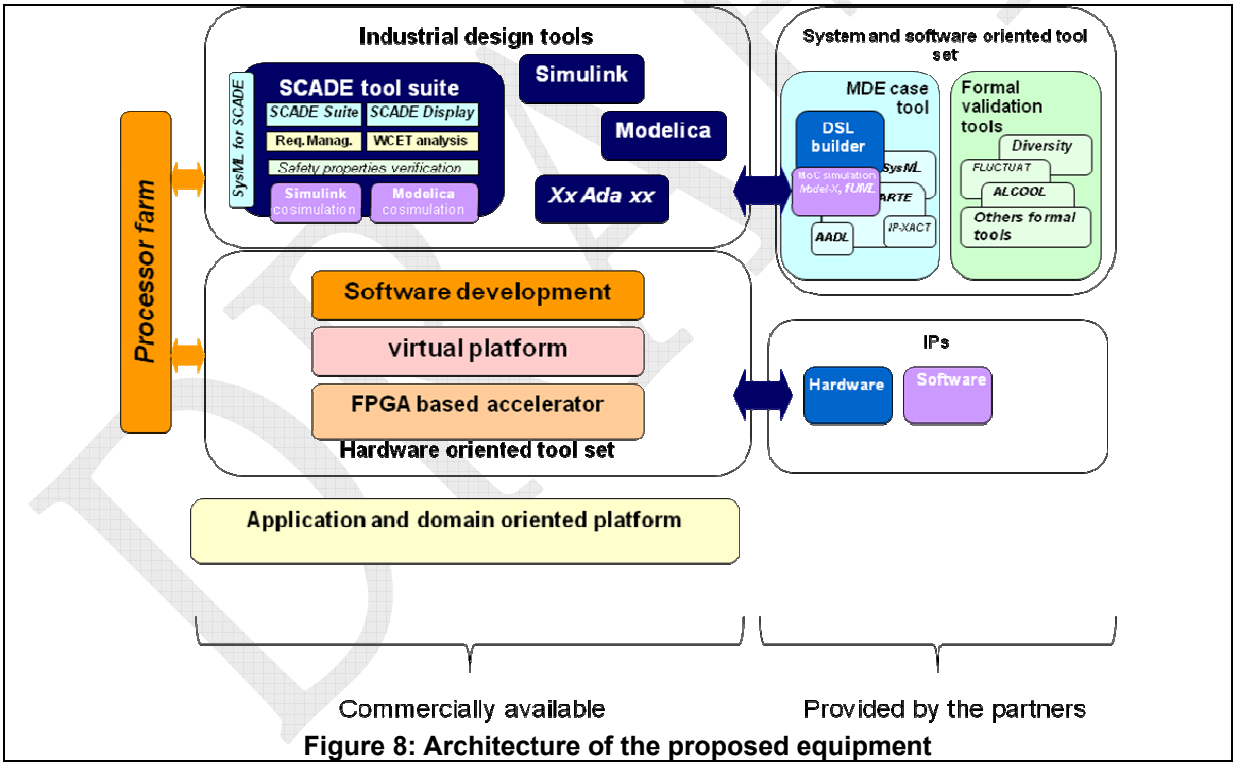

Figure 8: Architecture of the proposed equipment

The platform is composed by a set of design and validation tools, interconnected and cooperating, and of a hardware platform to either accelerate those tools or provide real scale evaluation of the elements produced and analyzed by the tools.

Figure 8 shows an overview of the tools composing the platform and of their interaction. On the right side, the tools are developed by the partners and will be provided for the platform. The left part is commercially available tools that will be part of this proposal.

System and software design and validation tools

- Modeling tool suite for embedded system design:
  - Continuous and discrete world modeling: Matlab/Simulink with code generation of C but also of RTL directly usable by the FPGA-based accelerator, verification, validation and testing. Modelica.
  - SCADE related tool sets: SCADE suite case tool, SCADE Display tool, SCADE System Designer, the code generator and the extensions for: requirement management, WCET analysis, safety properties verification, Simulink to SCADE import and co-simulation, SCADE-Modelica co-simulation

  These tools are commercially available tools acquired for and provided in the equipment. They will use floating licenses, allowing partners and user to use them on any system connected to the network of the platform. A security system will allow only authorized computers to access the platform network.
  Initially, as the FPGA-based accelerators can support up to four simultaneous users, we propose to have four complete suites of all the software, with licences allowing to cover all the "V" cycles, including code generation for the FPGA-accelerators. During the life of the platform, with a growing interest of using it, this number will certainly be not adequate. The proposed solution is that either users buy their own licenses, once they tested what they really need with the platform, or we buy new licenses with the fees we gain from the users.

  How to ensure that the software will not be used for something else? User signs a user's agreement explicitly stating that?

- Tools for research on new approaches for system and software engineering:
  These tools will be taken from the open source community or provided by the partners and extended for usage in the equipment through development contracted with specialized SMEs under control of project partners.
  - **Papyrus**, ***Papyrus DSL builder*** , ***Papyrus modeler.***
    - New features will be added during the life of the platform through research projects:
      - ***IP-XACT*** specialization and model,
      - ***Usage profiles*** for SysML and MARTE and model interfaces to Simulink and Modelica,
      - Model import services from usual commercial UML tools,
      - Documentation and C/C++ code generators including behavioral aspect for dedicated SysML and MARTE sub-profiles,
      - Model sharing and model revision management.
  - **RAVENSCAR oriented support:** It will provide translation of MARTE models built in the Papyrus modeler into AADL models and code generation from AADL models.
  - **Model based simulation support:**
    - ***Model-X*** xxxx tbc by Supelec xxx
    - ***RT-fUML simulator*** xxx tbc by CEA & Supelec xxx

- Validation tools:
  These tools will be also provided by the partners.
  - **Diversity framework,**
  - **FLUCTUAT,**
  - **ALCOOL,**
  - **TimeSquare.**

- Virtual platform:

The platform will use UNISIM that provides several virtual platforms and a framework to ease the development of new virtual platforms. Several open source virtual platforms for different targets (ARM, PowerPC, Star12X, and TMS320C3X) and different hosts (Linux, Windows, Mac OS X) are available.

Hardware accelerators:

- A cluster of processors (processor farm) composed of classical x86 multi-core processors equipped with large amount of memory to run the software tools, development tools and compilers, simulators and to interface with the FPGA based accelerator and to the extensions. Some of the nodes in the cluster can also embed accelerator boards either provided by some of the partners or off-the-shelf (GPU boards - for example Fermi boards -). Development tools and compilers will also be provided.

  The basic system is composed of 4 high end desktops PCs for controlling the FPGA-based accelerators and allowing having up to 4 simultaneous accesses to them.
  The processor farm is composed of <TbD> and will be used to accelerate simulations but also for the compilation phase of a design for the FPGA-based accelerators.
  This is new equipment fully dedicated to the platform, will be installed in a room in the NanoInnov building in Saclay, and is compliant with all safety and regulation standards. It is the latest versions that are available from the distributors.

- An FPGA based accelerator:
  The FPGA-based accelerator is new equipment fully dedicated to the platform.

  - Zebu-Server, from eVe (co-verification hardware/software of complex system up to a billion gates).

  Or

  - Veloce Quattro, from Mentor Graphics (emulation and verification design with up to 120 Millions gates in emulation ICE or acceleration of simulation).

  Equivalent systems exist in France in companies (ST Microelectronic for example) but it is not accessible for researchers, and the CIMPACA platform [CIMPACA] is dedicated for characterization of ICs

- Application related hardware: All these components form new equipments.

  A powertrain system test bench with a synchronous motor with permanent magnet, a Foucault current brake, a converter/inverter, a high voltage electric power supply, a cooling system, a synchronous motor for load, a dissipative electric energy system (discharge resistor), measurement instrumentation (torque and speed measurement system, voltage and current meters), a field bus (control of the load motor and Foucault break), a real-time operating system, a battery emulator (able to take into account the state of charge, the saturation on current demand, the cells imbalance,…), convertor DC/DC, low-tension battery, dissipative load resistors.

  BIVREE (Banc d'Intégration et de Validation de Réseaux Electriques Embarqués) for simulation of particular electric environments of equipments under development, xoupled with a real size mockup of the entire electrical and electronic architecture (EEA) of a given system (e.g. a car, truck or part of a plane):
  - Use of models (Matlab, Saber, Scade, Amesim, …) allowing modeling equipments,
  - Real-time acquisition and analysis of data,

- Generation of pattern for stressing the system, with an environment very similar to real use.

Other extensions could be added to the base platform, for example a test bed for critical and safe embedded systems. It could allow simulating:

- Typical automotive environment (representative of actuators and sensors),
- A heterogeneous and redundant computing platform, with multiple computing elements multi-core connected by a network.

It will also have all the tools required to test and probe in real-time of the various hardware parts of the emulated system: data acquisition, compiling the software, debugging it. It will also include high level software description (Matlab, Scade, Amesim) to model the complete equipment. This extension targets critical embedded systems such as automotive and avionics. Extra costs for the setting and maintenance/update for this extension will be integrated in the global cost of maintenance.

After its initial setting, the platform could evolve in time, according to the different requirement, therefore limiting its obsolescence.

2.2.3 ENVIRONNEMENT TECHNIQUE / TECHNICAL ENVIRONNEMENT

(3 pages maximum)

Après avoir précisé la description de l'équipement et sa localisation, décrivez les infrastructures nécessaires pour sa mise en place (bâtiment, espace spécifique, alimentation électrique…). Vous préciserez ainsi si l'environnement matériel nécessaire à l'installation de l'équipement est disponible actuellement. Si ce n'est pas le cas, dire précisément quand il le sera (nota : les infrastructures ne sont pas éligibles dans le cadre de l'action EQUIPEX, ni les personnels nécessaires au fonctionnement de l'équipement, voir le « règlement relatif aux modalités d'attribution des aides au titre de l'appel à projets équipement d'excellence »).

Un engagement du(des) responsable(s) du(des) site(s) d'accueil confirmera que l'équipement pourra être installé et mis en service à sa livraison, et que les moyens nécessaires à l'accompagnement de son fonctionnement, y compris en termes de personnel, seront effectivement mis en place.

This proposal has a close link with IRT SystemX. <Add more references to IRT SystemX> It is proposed to install the hardware platform in a building (still under construction) of the "Centre d'intégration" of NanoInnov, on the Saclay area. There are several drives for this location: it is near the NanoInnov academic and industrial partners, it is not so far from some industrial companies that could be interested by accessing the platform (PSA in Vélizy, Renault in Technocentre, Clemessy in Les Ulis, Delphi in Cergy, Thalès in Palaiseau, Sherpa Engineering in Saint Quentin en Yvelines, Valéo in Cergy, …).

<Give more details on the link Digiteo/Nanoinnov. AP: T. C., J-N. Patillon>

The hardware part of the proposal is composed of 3 elements, a cluster of processors (processor farm), an FPGA based Accelerator and application related hardware (powertrain test bench, "banc d'intégration et de validation de réseaux éléctriques embarqués", etc).

<Give mode details on the server farm, and possible extension with GPU, multi-cores boards>

The most demanding in term of technical environment are the FPGA-based accelerators that will be described in more details below. For this platform, we will privilege companies that are providing state-of-the-art systems and that are near the location of the installation platform, for fast response to the needs, potential collaboration and also to help local employment. For

example, the eVe company, located in Palaiseau, is selling an FPGA based system, using Xilinx components, which allow co-verification hardware/software of complex system up to a billion gates.

<Waiting for more input from eVe + squeeze to fit in pages>

Mentor Graphics, also located in the area, is also proposing a validation platform assisted by hardware. They have developed their own FPGA in France (Meta Systems company, now part of Mentor, but R&D center located in France, Meudon la Forêt). The “Veloce” Quattro is a multi-user platform allowing to emulated and verify design with up to 120 Millions gates in emulation ICE or acceleration of simulation.

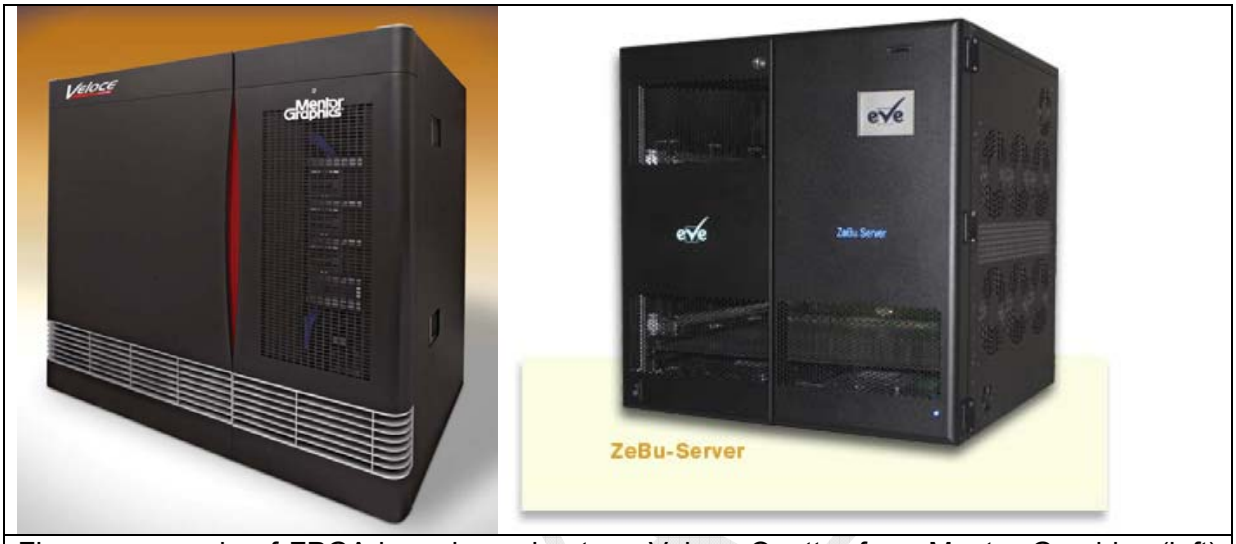

Figure : example of FPGA-based accelerators: Veloce Quattro from Mentor Graphics (left) and Zebu-Server from eVe (right)

The equipment proposed by Mentor Graphics for this platform, Veloce QUATTRO, is a state of the art hardware emulator and accelerator, able to map any design described in RTL (VHDL/SystemVerilog/Verilog) in order to handle verification acceleration in different modes at the very beginning of the design cycle:

- High level of abstraction verification using SystemC/C/C++/SystemVerilog environments to drive the Design Under Test mapped in the Veloce QUATTRO,
- Simulation acceleration by reusing the same environment developed for the pure simulation,
- In Circuit Emulation (ICE) where the design mapped in the Veloce QUATTRO can be connected to other external equipment (testers, custom hardware board, standard bus interface …),
- Mix of high level abstraction environments (C/SystemC/C++/System Verilog) and In Circuit Environment for full flexibility.

This capability of ICE allows to replace an non-existing chip by the FPGA system. Due to timing constraints, the maximum distance between the system cabinet and the board where the chips are emulated are limited to few meters. The system is able to have up to 4096 IOs.

This allows the Veloce QUATTRO to be used at all stages of the verification cycle of a project, whether at block level, System on Chip level (SoC) or system level (interconnection of multiple SoCs). This makes it a perfect fit for verifying blocks of Intellectual Property and then connecting them in a bigger design where real time OS, software drivers, external interfaces and system validation can be done conveniently.

As the verification can be run at the MHz speed (10000X faster than simulation), it enables application tests to be run in few minutes versus few days/weeks (for example 25 HDTV frames (1 sec of real time) to be run in few minutes on Veloce versus few weeks in simulation).
The design capacity that the equipment can handle is up to 100 million gates, making it suitable for today and tomorrow's designs.
The Veloce Quattro allows full visibility at any time to any node of the design under test without impacting the gate capacity or model performance. The full visibility make Veloce used a lot in post silicon validation, where an issue is found on the silicon and visibility is needed (not possible with the silicon), then Veloce is used to emulate the design, reproduce and debug the error to fix the silicon.
The TBX software, Testbench Xpress, transaction based methodology associated with the Veloce QUATTRO, enables the hardware emulator to be connected to high level C, C++, SystemC, SV based environments enabling verification very early in the design cycle and the possibility to connect a wide variety of other tools to the emulator for building complete systems.Such a system can be used in conjunction with Matlab. For example, in a FIR filter design, Matlab will generate the coefficient values of the FIR on the fly and they will be applied to the real hardware implementation of the FIR in the Veloce QUATTRO.

The Veloce QUATTRO can be shared by up to four users in order to maximize the usage of the machine. A key point as we mention about Intellectual Property is the protection, soit has added the ability to encrypt the input to Veloce or the output from Veloce. This encryption is based on the IEEE1365.
The Veloce QUATTRO is being used by most of the major semiconductor companies in all regions of the world, with some examples of STMicroelectronics in France, Broadcom in the US or Huawei/HiSilicon in China.
The Veloce family of emulator is starting with this QUATTRO equipment and will be maintained for numerous years (over 10 years). It will in addition be enhanced over the years in order to cope with new advances in technology (this is what they are doing with the French project with NANO2012) and new need from its users.

Due to all those constraints, he hardware will be installed in an dedicated air-conditioned room for the FPGA based accelerator and for the farm of computers. Due to the capability of In-Chip-Emulation of the FPGA accelerator, it cannot be in a standard server room. The hardware based platform will also be installed in the same room, allowing using the FPGA-based accelerator to emulate chip on the test beds. This room will be with controlled access, but the partners and users will have access if they need to have physically access to the boards under test or to the test beds.
Due to the weight density of the servers, the floor of the room will be able to support up to 500 Kg/m². The electric power available will be above 15 KW, with back-up of 5 mn (time enough to safely shutdown the system, but not to save all the simulations, but as the power outages should be exceptional and it is mainly research equipment, this is considered as acceptable). The cooling capacity for the room will be of about 10 KW.
The equipment will be connected to the outside world by standard Ethernet routed through VPN for users outside of the installation.

The main room will be in the building N2 of the NanoInnov Paris Région (in Palaiseau, in Quartier Ouest de Polytechnique [Nonoinnov]. The building is expected to be available in Q1 2011; and the main room by Q2 2011. The special equipment of the room will consist in:

- Reinforcement of the floor to support 500 kg/M² (or adding special floor distributing the load),
- Local backup power system, up to 5 mn at 10 KW (FPGA-based accelerator and computer farm),
- Air-cooling (10 KW),
- Ethernet connection,
- Access control.

One of the servers in the room will also be a license server for the various software tools that will be part of the platform.

For the support of the system, a global load of 1 FTE (Full Time Engineer) is expected, but physically split on 2 to 3 persons.

3. STRATEGIE DE VALORISATION DES RESULTATS/ DISSEMINATION AND EXPLOITATION OF RESULTS

(2 à 3 pages maximum)

Présenter les stratégies de valorisation de l'équipement :

la communication scientifique,

la valorisation des résultats attendus,

les échéances et la nature des retombées scientifiques, techniques, industrielles, économiques …,

le cas échéant, la place du projet dans la stratégie des entreprises partenaires,

autres retombées (normalisation, information des pouvoirs publics…),

l'incidence éventuelle sur l'emploi, la création d'activités nouvelles,

- …

Présenter les grandes lignes des modes de protection et d'exploitation des résultats

Pour les projets partenariaux organismes de recherche/entreprises, les partenaires devront conclure, sous l'égide du coordinateur du projet, un accord de consortium dans un délai de un an à compter de la date d'entrée en vigueur des actes attributifs d'aide.

The intrinsic power of the platform will allow validating software of complex embedded systems, which is an identified need for several research laboratories, SMEs and companies. A partnership with the users will allow extending the platform by adding their own contributions (hardware or software), allowing other users to benefit from it and creating an ecosystem around the platform. (Few companies that were already contacted expressed their willingness to provide IPs for the platform). The contributions are related to embedded systems, allowing other users to focus on their own knowhow, or are related to the platform, extending its application domain, or its ease of use (new interface software or supported features).

In the automotive area, the technological platform will embed some hardware components of the powertrain system of vehicle architecture. It enables to reproduce some specific operating modes of the vehicle (traction, energy recovery, urban/extra-urban driving cycle), as well as a part of the vehicle environment (road profile, driver behaviour). This platform will enable to build a common vision for the design, simulation and validation of embedded system for automotive.

In this project, several national research laboratories will bring their expertise in the field of the design, model, analysis of electric propulsion systems, the optimization of the electronic components sizing, as well as the energy flows management.

Several companies from the automotive area (e.g. Lumeneo – vehicle integrator -, ADM Concept – electric vehicle diagnostic - , Sherpa Engineering – development of model and control algorithms-) will find in this platform some interest for scientific collaboration and for increasing their market position. They also will contribute to the building of the platform thanks to their experience feedback.

For user willing to use the platform without sharing their Intellectual Properties, an access fee will be requested, to contribute to the maintenance cost or to the acquisition of new hardware/software/licenses.

Scientific publications, obtained with the results from the platform, should explicitly quote its contribution.

The Platform should be easily accessible to software developers. Training sessions about the hardware and the software of the platform will be key elements to demystify the approach proposed by the platform and to allow the users to take full benefit of it. The user-friendliness is very important, because most of software developers don't want to know the details of the underlying hardware.
Another use of the platform is about teaching of embedded systems: its localization and its access by the network will make it an efficient tool for Digiteo Labs.

The platform will be open to SMS and companies, allowing them to reduce their time to market and time of design, verification and validation of their embedded systems. One particular point will be to ensure that the platform can be used while keeping all data confidential, a necessary requirement for some companies.

A list of academics having shown interest in using the platform is enclosed below:
<To be contacted, list to be updated and sorteb by alphabetic order>

Name	Organization/company	Domain	Comment
O. Sentieys	ENSSAT	Traitement numérique du signal	AP: M. D.
F. Petrot	TIMA CNRS/INPG/UJF		AP: M. D.
A. Seznec	IRISA		AP: M. D.
O. Temam	INRIA Saclay		AP: M. D.
A. Greiner	LIP6		
J. Sifakis	IMAG		

4. MANAGEMENT DU PROJET / PROJECT MANAGEMENT

4.1. ASPECTS ORGANISATIONNELS / MANAGEMENT

4.1.1 QUALIFICATION DU COORDINATEUR DE PROJET /RELEVANT EXPERIENCE OF THE PROJECT COORDINATOR

(1 page maximum)

Fournir les éléments permettant de juger la capacité du coordinateur à coordonner le projet.

<TbD, Choose a coordinator>

4.1.2 MODALITÉS DE COORDINATION/ COORDINATION MODALITIES

(1 page maximum)

Préciser les aspects organisationnels du projet en fournissant un organigramme (nom du coordinateur du projet, responsables scientifiques et financiers pour chaque partenaire…)
Prévoir les règles d'utilisation de l'équipement (accessibilité, conditions d'utilisation, tarifs…)

<TbD>

The platform will be daily managed by a set of system managers and by power users, under a supervision of a supervision board comprising a member of each partner. On open hours, at least one system manager will be available to support the users and manage the machines (back-ups, upgrades, licenses, etc). For supporting the users, it will be helped by power users that will have experience of the various tools composing the platform. Training will be regularly organized for new users.
It is proposed to have a set of people that can act of system manager, but not full time dedicated to that.
In case of conflicts (in attribution or resources), the supervisory board will be called and it should give its decision in a minimum amount of delay <specify?>.
The decisions concerning the management of the platform (schedule, price and conditions to access he various part of the platform, evolution by adding new hardware) will be done during regular meetings (one per month) of the supervisory board.
Statistics will be collected during the operation of the platform, allowing tuning it for better user experience.

The platform will be accessible remotely through VPN for partners or users that don't need to have physical access to the hardware. Access control will secure the access to only authorized users.
The users that require to have physical access to the platform (because they use its ICE capabilities or its hardware environment support, e.g. for automotive applications), will be able to easily enter the building and the room (after access control), and a neighboring office room will be available.
The partners will have full access to the platform, but users will have access according to their contribution to the platform.
The hardware FPGA-accelerator can have up to 4 simultaneous users, and the amount of resource they can use is under control of a supervisor. If the resources requested are below the available amount, they can have immediate access. If not, a priority schedule will be set by a supervisory board of the project.
Similarly, if some user require a complete access to the hardware (for confidentiality reasons or size of their design), the rules will be set be the supervisory board of the project.

<Define more precisely access control, rules to select access for users, how to set priorities, etc>

4.2. ORGANISATION DU PARTENARIAT / COLLABORATION ORGANIZATION

4.2.1 DESCRIPTION, ADEQUATION ET COMPLEMENTARITE DES PARTENAIRES/PARTNERS DESCRIPTION , RELEVANCE AND COMPLEMENTARITY

(0,5 page maximum par partenaire)

Décrire brièvement chaque partenaire et fournir ici les éléments permettant d'apprécier sa qualification dans le projet. Il peut s'agir de réalisations passées, d'indicateurs (publications, brevets), de l'intérêt du partenaire pour le projet...

The success of the platform is closely related to its openness, the proposal includes partnership with institutes, laboratories or enterprises that will extend it in several directions:

- Hardware of software extensions to extend the application domains covered by the platform,

- Contribution to the software chain easing the use of the platform for non-specialists (for example, by delivering interfaces with high level or domain specific languages such as UML, MARTE, SysML, EAST-ADL; SysML/C, SCADE, Matlab,…)
- Use of the platform for accelerating algorithmic developments (input languages such as “C” or “C++”, System-C).
- Increase of the IP library.
- Adding extra accelerator to the platform, either from the partners or available on the market.

The initial list of partners is:

- CEA: Design of systems, verification, design of IPs,
- Institut Télécom: System modeling and provider of interfaces,
- ENSTA: Modellization of architectures, multi-cores, Design Space Exploration,
- INRIA:
- Polytechnique:
- Supelec:
- LRI: System diagnostic, embedded software,
- ENS Cachan: control algorithms
- Thales: System validation, transport and security applications.

Potential users could be (they were not yet contacted):

<To be ordered by alphabetic order>

- Academics: LIP6, UTC, IRSEEM, LASMEA, LIRMM, TIMA, LASS, …
- Companies: EADS, ALSTOM, DELPHI, VALEA, Safran, ST, STE, ALTIS, …
- SMEs: Esterel Technologies, Magilem, Confluent, eVe, DXO, Scaleo Chip, Arteris, Virtual Logic, Trialog, …
- Start-ups: Kalray, PharOS.

<Defining the conditions for accessing to the platform>

CEA :

<To be summarized: AP: T. C.>

Embedded system cores: CEA LIST Embedded Computing Laboratory is developing several architectures based on multi-cores, for various applications domains such as vision and image procession. Research activities includes dynamic migration of task, hardware support for scheduling, efficient and programmable processing chain,

<To be Done>

Embedded system diagnosis: the need for more accurate and wide range diagnosis systems is then essential, and this kind of system must be designed and tested in conditions as close as possible to real life. As new car technologies are emerging (hybrid and electric vehicles holding new electric and electronic systems), this need will be more important. CEA LIST LFSE together with other academic and industrial partners, has been working for several years on cable diagnosis systems and specific diagnosis systems for batteries and fuel cells. It has been recognized by OEM (Original Equipment Manufacturers) that 70% of ECUs

returned for expertise were diagnosed free from defects: in these cases the faults were due to connectors and cables. The maturity of this work will require new tools to help, like the proposed platform.

Motor control and energy management: the Interactive Robotic Laboratory (CEA LIST LRI) has developed an expertise in the field of motor and electric actuators control for several years. This research works focuses on the analysis of complex mechatronic systems: development of new technologies, tools and design methodologies, as well as control algorithms. To face with these multidisciplinary challenges, the laboratory includes several scientific and technical skills, such as mechatronic design (system architecture, structure, motor, actuator, measurement, design methodology), modelization (energetic and multi-physics), as well automatic control (electronic, signal processing, advanced control, supervision). Some of the system technologies developed in the laboratory is exploited within the industry. The final objectives of the works performed are the components sizing and modelization of the powertrain system, in the perspective of the control and energy management of the vehicle.

Another project at the LRI, called Forewheel, is a technological breakthrough in the field of electric vehicle. The objectives of this project supported by the ADEME is to demonstrate the technical feasibility and the economic viability of a new concept of a fully electric vehicle endowed with some communication tools (ITS environment, permanent internet connection, machine-to-machine communication,…). This project is based on the Active Wheel concept (motorized wheel with integrated electric suspension) associated with the by-wire and IT technologies.

Sherpa Engineering and CEA LIST (LRI) are collaborating within an industrial project for the development of model and control algorithms for electric vehicle.

ENSTA :

ENSTA is a public organization for higher education under the authority of the French Ministry of Defense . ENSTA develops Embedded Systems Research through:

- des méthodologies d'exploration et de paramétrisation automatique de processeur embarqué (paramétrisation de la micro-architecture, du jeu d'instruction avec extension SIMD sur mesure)
- Automatic design space exploration of embedded multiprocessors (MOCDEX),
- automatic synthesis from parallel programs of embedded multiprocessors (MOCSOC),
- applications in image processing/compression vision (JPEG-2000, artificial retina), telecommunications (SDR – Software Defined Radio) .

On these research topics, ENSTA cooperate with DGA since many years for military applications and with other partners in the framework of national or European projects.

<To be translated. AP : O. Hammami>

MENTOR GRAPHICS :

Le groupe MENTOR GRAPHICS est un des leaders mondiaux sur le marché de l'automatisation de la conception électronique (Electronic Design Automation, EDA). A ce titre, elle fournit des solutions pour la conception de logiciels et de matériels permettant aux entreprises de développer plus rapidement des produits électroniques de pointe tels que, par exemple, des téléphones portables ou des ordinateurs.
Le groupe MENTOR GRAPHICS a également une activité permettant d'optimiser et de faciliter la conception de cartes et circuits intégrés.
Le groupe MENTOR GRAPHICS est un partenaire majeur de la société STMicroelectronics dans le cadre du programme NANO2012 et a indiqué son intention d'accroitre ses effectifs d'environ 30 personnes en région grenobloise dans le cadre de ce programme.
Le groupe MENTOR GRAPHICS a été crée aux Etats Unis en 1985 et est côté sur le marché américain du NASDAQ.
Lors de son exercice clos le 31 décembre 2010, il a réalisé un chiffre d'affaires d'environ USD 802.000.000.
Il emploie 4425 salariés à travers le monde (dont 235 en France) et dispose de 28 centres de recherche et de développement.

La société META SYSTEMS est une filiale française du groupe MENTOR GRAPHICS dont le siège social est situé à Meudon la Forêt. Elle a été créée en France en 1991. La société META SYSTEMS emploie environ 50 ingénieurs et docteurs-ingénieurs sur son site parisien.
Au titre de ses activités, la société META SYSTEMS conçoit, produit et commercialise des émulateurs dit software emulators qui sont des appareils qui permettent de vérifier le design c'est-à-dire la capacité technique et l'efficacité opérationnelle de produits électroniques complexes.

(1 page maximum)

Montrer la complémentarité et la valeur ajoutée des différents partenaires dans le cadre des coopérations passées, présentes et à venir. L'interdisciplinarité et l'ouverture à diverses collaborations seront à justifier selon les orientations du projet.

<To be done, collaborations and complementarity of partners>

Liste des utilisateurs

Partenaire/Partner	Nom/Surname	Prénom/First name	Poste/Position	Discipline/Domain	Organisme de rattachement ou entreprise/Organization or company	Rôle dans le projet (4 lignes max.) / Contribution in the project (4 lines max)
Utilisateur	SORINE	Michel	Directeur de Recherche de 1ère classe à l'INRIA. Responsable de l'équipe-projet SISYPHE de l'INRIA	Modélisation, analyse et commande de systèmes dynamiques complexes en physiologie ou en ingénierie	INRIA Rocquencourt, équipe SISYPHE	Acquisition de données pour recalage de modèles
Utilisateur	ZHANG	Quinghua	Chercheur	détection et diagnostic de pannes, identification de systèmes non linéaires	INRIA IRISA, équipe SOSSO2, Campus de Beaulieu, Rennes	Acquisition de données pour recalage de modèles

				observateurs adaptatifs pour systèmes linéaires et non linéaires		
Utilisateur	PICHON	Lionel	Directeur de recherche 2ère classe au CNRS, Responsable de l'équipe ICHAMS Interaction champs – matériaux et structures	Modélisation de Systèmes Electromagnétiques - Propagation d'ondes - Compatibilité Electromagnétique - Outils de conception et de simulation	SUPELEC LGEP, Laboratoire de Génie Electrique de Paris	Acquisition de données pour recalage de modèles
Utilisateur	LOETE	Florent	Chercheur	Conception de systèmes électroniques embarqués, diagnostic de câbles	SUPELEC LGEP, Laboratoire de Génie Electrique de Paris	Test de systèmes de diagnostic sur plateforme matérielle
Utilisateur	LOUIS	Anne	Responsable du Pôle Electronique et Systèmes à IRSEEM et Directrice de la Formation Doctorale de l'ESIGELEC	Compatibilité électromagnétique, conception de systèmes embarqués	IRSEEM, Rouen	Test de systèmes embarqués sur plateforme matérielle
Utilisateur	PICON	Odile	Responsable de l'équipe « Electronic, Communication, Systems and Microsystems Laboratory » (ESYCOM) à l'Université Paris Est Marne La Vallée	Modélisation électromagnétique, antennes, propagation et communication numérique	Laboratoire ESYCOM, Université Paris Est Marne La Vallée	Acquisition de données pour recalage de modèles

4.2.2 QUALIFICATION, RÔLE ET IMPLICATION DES PARTENAIRES / QUALIFICATION, ROLE AND INVOLVEMENT OF INDIVIDUAL PARTNERS

Qualification des personnes : préciser leurs activités principales et leurs compétences propres. Pour chaque partenaire remplir le tableau ci-dessous

Partenaire/Partner	Nom/Surname	Prénom/First name	Poste/Position	Discipline/Domain	Organisme de rattachement ou entreprise/Organization or company	Rôle dans le projet (4 lignes max.) / Contribution in the project (4 lines max)
Exemple	LATIFI	Fatima	Professeur		CNRS	Gestion de l'installation de l'équipement
Coordinateur			Engineer/scientist		CEA LIST	

5. EVALUATION FINANCIERE DU PROJET/ FINANCIAL ASSESSMENT

Justification scientifique et financière du coût complet du projet. S'il y a lieu, en partant de la décomposition en éléments constitutifs de la partie 5, vous préciserez les points suivants :

1- La justification scientifique et financière des montants demandés au titre du coût d'investissement (tranche 1 du « règlement relatif aux modalités d'attribution des aides au titre de l'appel à projets équipement d'excellence »). Vous indiquerez tout d'abord, s'il s'agit :
- *d'un élément disponible sur étagère, indiquer le ou les fournisseurs potentiels et leur localisation (pays) ainsi que le coût HT d'acquisition (basé sur un ou plusieurs devis mis en annexe 7.3), tels que connus à ce jour,*
- *d'un équipement réalisé spécifiquement : une estimation du coût de réalisation HT (basée sur un ou plusieurs devis mis en annexe 7.3).*

Dans tous les cas vous préciserez :
- *les coûts liés à la passation et à la réalisation de marchés,*
- *le nombre d'hommes.mois et le coût des personnels nécessaires à la réalisation de l'équipement, s'il est élaboré et construit (tout ou partie) par les partenaires du projet,*
- *les coûts liés à l'installation (adaptation de l'environnement d'accueil, installation électrique, climatisation, renforcement du sol, modification des cloisons…),*
- *les frais de propriété intellectuelle,*
- *dans le cas d'équipements de données : frais de collecte, de numérisation, d'aide à la production et à la préservation de données,*
- *T.V.A non récupérable.*

2- La justification scientifique et financière des montants demandés au titre du coût de fonctionnement hors masse salariale (tranche 2 du « règlement relatif aux modalités d'attribution des aides au titre de l'appel à projets équipement d'excellence »). Vous préciserez :
- *le coût de la formation des personnels devant assurer le fonctionnement de l'équipement,*
- *les coûts d'opération de l'équipement (fluides, petit matériel, consommables…) hors masse salariale,*
- *le coût annuel de la maintenance constructeur.*

3- La justification scientifique et financière des autres frais engendrés par l'acquisition et le fonctionnement de l'équipement, qui ne seront pas financés (hors assiette de l'aide), mais qui seront pris en compte pour le calcul du coût complet de l'opération. Vous préciserez :
- *le nombre d'hommes.mois de personnel administratif et scientifique (technicien, ingénieur, doctorant, post-doctorant…) nécessaire à son fonctionnement,*
- *le cas échéant, les éventuels co-financement apportés par un partenaire (donner tous les détails utiles),*
- *le cas échéant, le coût unitaire de la contribution qui serait demandée si l'équipement devait être loué,*
- *la durée d'amortissement couramment pratiquée pour ce type d'équipement.*

- *Elément 1/ Element 1*
- *Elément 2/ Element 2*
- *Etc.*

Ces éléments sont nécessaires pour la préparation du document de soumission A.

Chaque partenaire justifiera les moyens qu'il mettra en œuvre, en distinguant les différents postes de dépenses.

<To be Done>

The initial proposed cost is <TbD> M€. The operating costs can be split in cost of maintenance, and licenses (12% of the initial cost), training and local support for helping users and managing the system. The latter cost is not supported by this Equipex.
<Recurrent costs are supported by 3.43% interest rate>

The initial software investment is mainly licenses to access different commercial software, and subcontracting to realize the interface between them.
<To be completed>

- In order to make the connection to the modelisation part of the platform, CEA LIST's static analyzer FLUCTUAT would be linked to Esterel/SCADE and to Matlab/Simulink. A feasability study is currently almost complete in European FP7 project INTERESTED (leader: Esterel Technologies), for connection with SCADE, and in System@tic project EDONA (leader: Renault), for connection with Matlab/Simulink. Results have shown both an interest of end-users and software publishers for these connections. One of the goals of the plateform is to allow for these connections to be experimented by end-users. The validation process would then be seemingly included in the full development cycle.
Budget: 100 K€ for prototyping the SCADE/Fluctuat connection, 100 K€ for prototyping the Matlab/Simulink connection, by CEA LIST, and 300 K€ for re-engineering the prototype into a real tool, by the startup companies SAFE-IA and Knowledge Inside (for the part dealing with the current interconnection Matlab/Simulink with Arkitect and FLUCTUAT), 30 K€ of annual maintenance, as documented in the "cahier des charges 1" (details attached on the startup company).
- To address a larger panel of industrial programs, the analysis need to be scaled up. Part of this can be done through the parallelization of parts of the FLUCTUAT analyzer on the farm of PCs/GPUs of the platform. A first experiment had been made on the prototype, but further engineering work is needed. This would be subcontracted for an amount of 150 K€, with 15 K€ for annual maintenance.
- In order to make the connection to the low-level part of the development cycle, FLUCTUAT will be adapted to the assembly/binary level. A first prototype has been realized at CEA LIST, and with the University of Perpignan as a subcontractor ("FLUCTUAT/TMS320"). One of the objectives is to finalize this tool and embed it into the platform.
Budget: 150 K€ (3*50 K€) for subcontractors ABSINT Gmbh, SAFE-IA and University of Perpignan for finalizing the prototype, and 15 K€, as annual maintenance of the tool in the platform. 50 K€ will be dedicated to the "maitrise d'ouvrage" at CEA LIST. University of Perpignan would finish the prototype, ABSINT Gmbh which has a strong experience of analysis of binaries, would make the connection between FLUCTUAT and the binary level, and SAFE-IA would re-engineer the assembly tool.

Concerning ALCOOL, the static analyzer for asynchronous concurrent systems, it also requires to be interfaced to the rest of the platform.
Budget: 100 K€ for the prototyping and engineering at CEA LIST of the connection of ALCOOL with the high-level modeling tools of the platform, and 10 K€ per year as maintenance.

The main hardware related investments are the FPGA platform for accelerating simulation/validation/emulation, its associated software and hardware extensions to adapt to particular application domain.
For example, the eVe company, located in Palaiseau, is selling an FPGA based system, using Xilinx components, that allows co-verification hardware/software of complex system up to a billion gates. The estimated cost for a system with a capacity of several hundred of millions of gates is around 5 M€ depending on the configuration. About 400 K€ extra should be added for a local compute farm able to efficiently drive the system and to compile the netlist used by the accelerator. Software required to translate HDL languages towards a

netlist for the accelerator are about 160 K€. eVe is also proposing a rather complete list of components (memories, interfaces, etc) for 300 K€.
Maintenance cost is estimated at 12% of the initial investment.
Mentor Graphics, also located in the area, is also proposing a validation platform assisted by hardware. They have developed their own FPGA in France (Metasystem company, now in Mentor). The "Veloce" Quattro is a multi-user platform allowing to emulated and verify design with up to 120 Millions gates in emulation ICE or acceleration of simulation. The cost of the platform is between 500 K€ to 6 M€ depending on the configuration.

According to user's needs and requirements, the platform can be upgraded, for example by adding extra FPGA boards, or hardware boards interfaced with the FPGA platform.

Application related hardware
A system allowing to test embedded functions of a car and its environment ("iron car") is sold by CLEMESSY and I called BIVREE (Banc d'Intégration et de Validation de Réseaux Electriques Embarqués) and has the following characteristics:

- Simulation of particular electric environments or equipments under development,
- Use of models (Matlab, Saber, Scade, Amesim, …) allowing modeling equipments,
- Real-time acquisition and analysis of data,
- Generation of pattern for stressing the system, with an environment very similar to real use.

Besides this hardware extension (cost of about 500 K€), various software will be required to operate the system and to adapt it to the targeted applications.

Other extensions could be added to the base platform, for example a test bed for critical and safe embedded systems. It allows simulating:

- Typical automotive environment (representative actuators and sensors),
- Heterogeneous and redundant computing platform, with multiple computing elements multi-core connected by a network.

And it will have all the tools required to test and probe in real-time of the various hardware parts of the emulated system, for data acquisition, to compile the software, to debug it. It will also include high level software description (Matlab, Scade, Amesim) to model the complete equipment. The estimated cost for this extension is about 400 K€ and targets critical embedded systems such as automotive and avionics. Extra costs for the setting and maintenance/update for this extension will be integrated in the global cost of maintenance.

After its initial setting, the platform could evolve in time, according to the different requirement, therefore limiting its obsolescence.

	Year 1	Year 2	Year 3	Year 4	Year 5	Year 6	Year 7	Year 8	Year 9	Year 10
Total cost (k€)										
Equipex's contrib.										
Partners' contrib										
Users' contrib										
Total of gains										
Personal cost										
Hardware										

cost										
License cost										
Total of costs										
Exploitation result										

The following tables summarize the various costs:

System and software oriented tool set; commercially available tools:

Item	Description	Status	Initial cost (K€)	Maintenance
	SCADE			
	Matlab/simulink licences	Quote	464	7
	TOTAL		**464**	**7**

System and software oriented tool set; proposed by the partners:

Item	Description	Status	Initial cost (K€)	Maintenance
	MATLAB-Simulink/Fluctuat connection		100	
	Re-engineering of Fluctuat		300	30
	Parallelization of Fluctuat		150	15
	Adaptation of Fluctuat to binary level		150 + 50	15
	Interfacing ALCOOL		100	10
	MARTE vers AADL		175	17
	Générateur de code		350	35
	TOTAL		**1375**	**122**

Hardware oriented tool set; commercially available tools:

Item	Description	Status	Initial cost (K€)	Maintenance
	Server farm		400	40
	FPGA accelerator	Quote	4970	496
	FPGA tools	tentative	included	
	GPU accelerator boards			
	IP libraries	tentative		
	Equipment installation (Air conditioning)			
	TOTAL		**5370**	**536**

Hardware and software platform for real scale application evaluation; commercially available tools:

	BIVREE	tentative	500	50
	“Iron Car”			
	Testbed critical and safe embedded systems		400	40
	TOTAL		**900**	**90**

Grand total:

Type		status	Initial cost	Maintenance

			(K€)	
System and software oriented tool	commercially available tools		464	7
System and software oriented tool			1375	122
Hardware oriented tool set	commercially available tools		5370	536
Hardware oriented tool set				
Hardware and software platform for real scale application evaluation	commercially available tools		900	90
Hardware and software platform for real scale application evaluation				
Total			**8109 K€**	**755 k €/year**

6. ANNEXES / APPENDICES

6.1. REFERENCES BIBLIOGRAPHIQUES DE L'ETAT DE L'ART/STATE OF ART REFERENCES

Inclure la liste des références bibliographiques utilisées dans la partie « Etat de l'art ».

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6.3. DEVIS POUR L'EQUIPEMENT/ESTIMATE FOR THE EQUIPEMENT

Insérer la copie des différents devis de la partie 6.
En cas d'absence de devis : demander une estimation à partir de coûts d'équipements comparables ou d'appels d'offres.