# Analog to Digital Converter (ADC)

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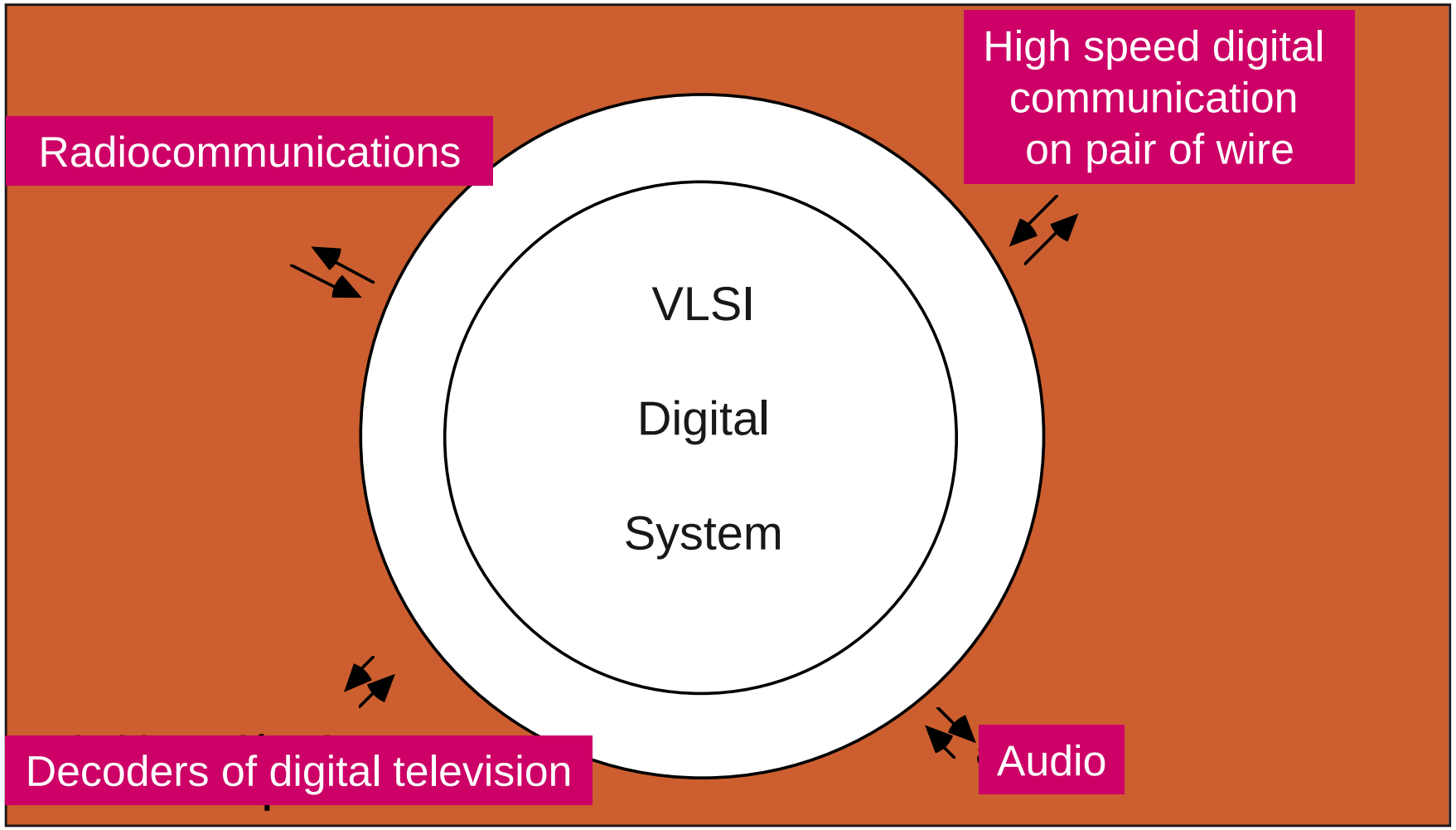
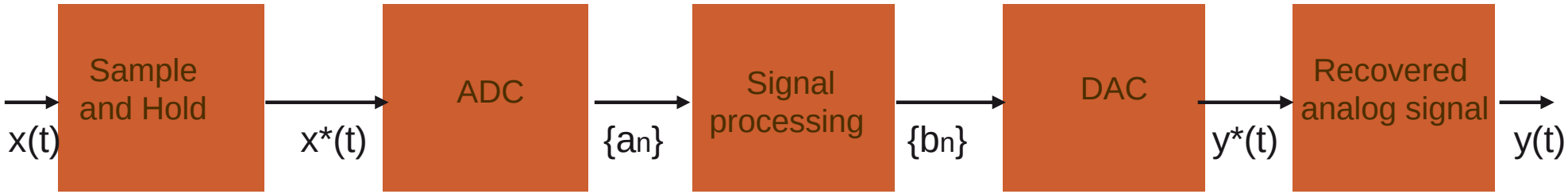
# Outline

- “Nyquist” ADC
- Parallel comparators (Flash) ADC
- Successive-approximation-register (SAR) ADC
- Integrating ADC
- Oversampling ADC
- Performances

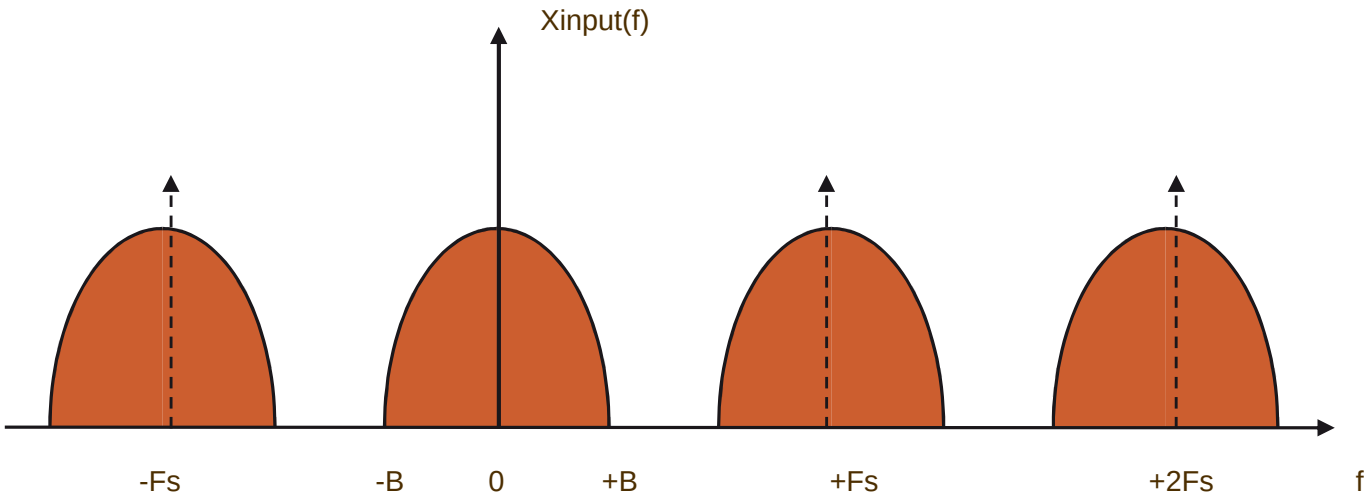
# Telecommunications draw the performances



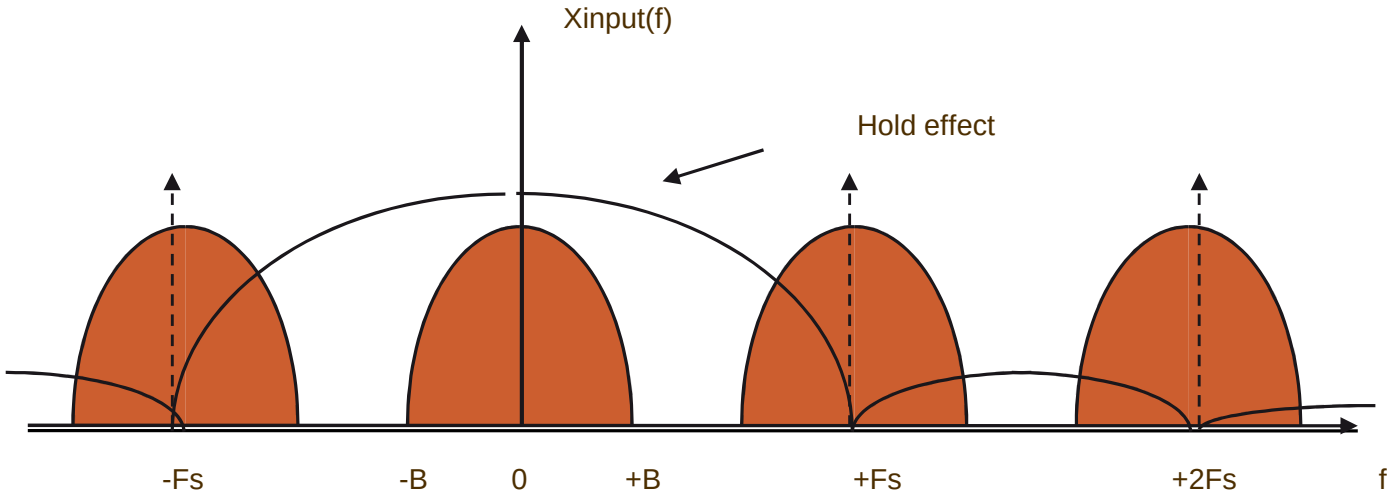
# Signal acquisition



# Sample and hold effect

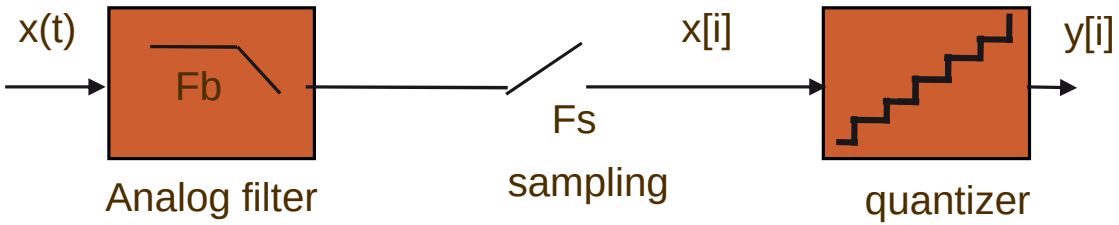


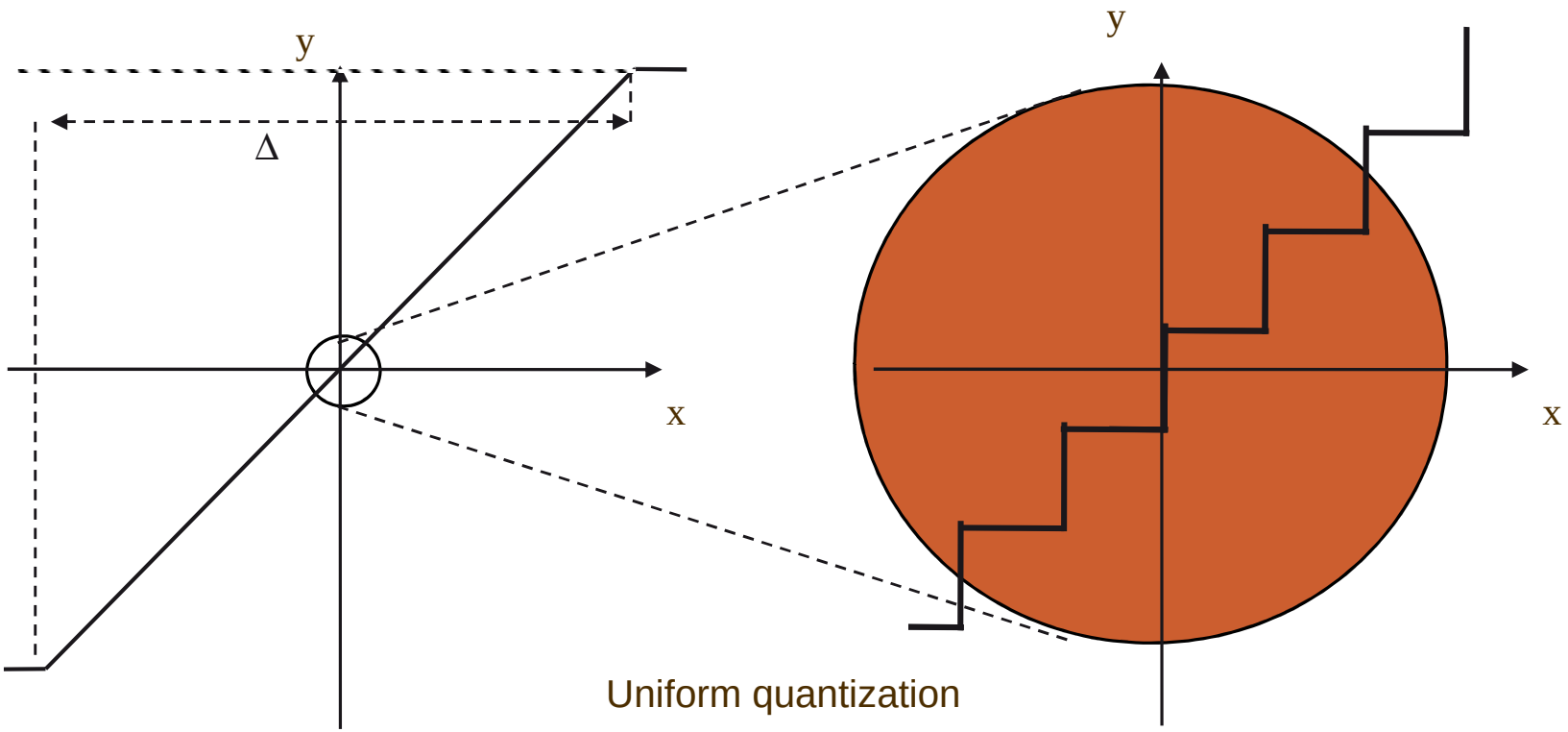

Spectrum of sampled signal




Hold effect on the spectrum

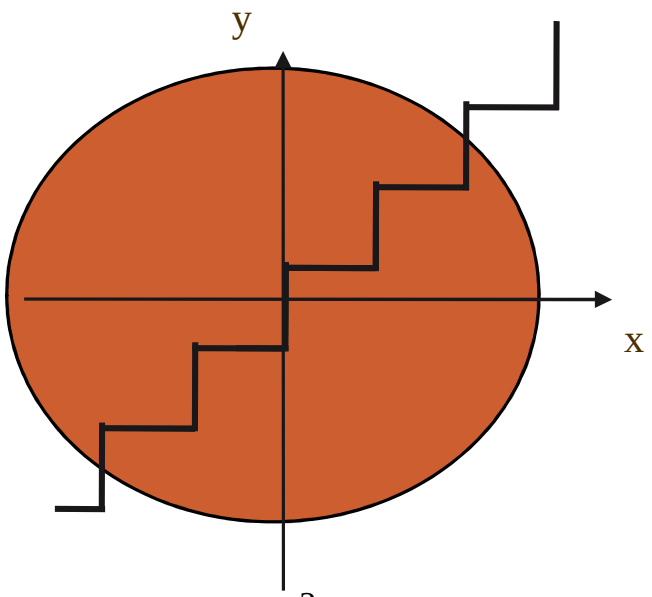
# Nyquist ADC

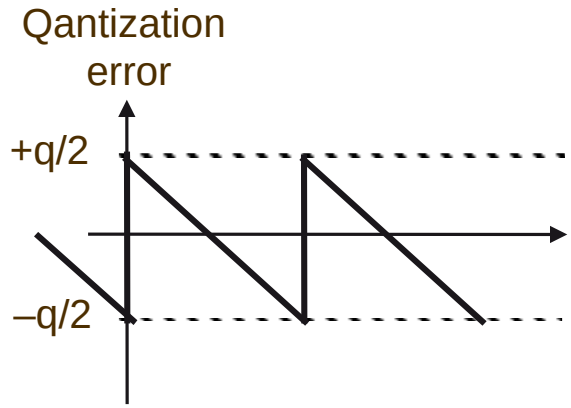



Uniform quantization

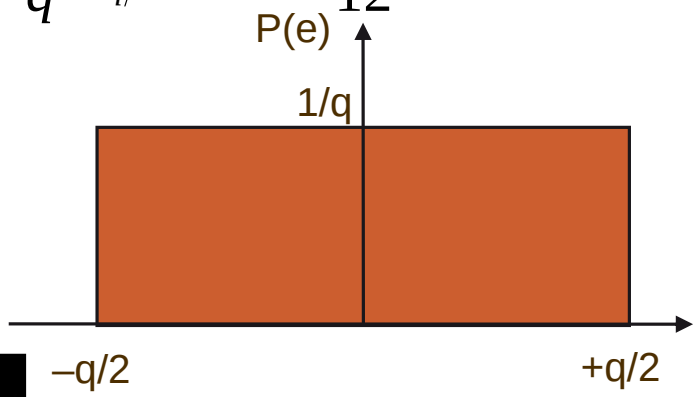
# Quantization error

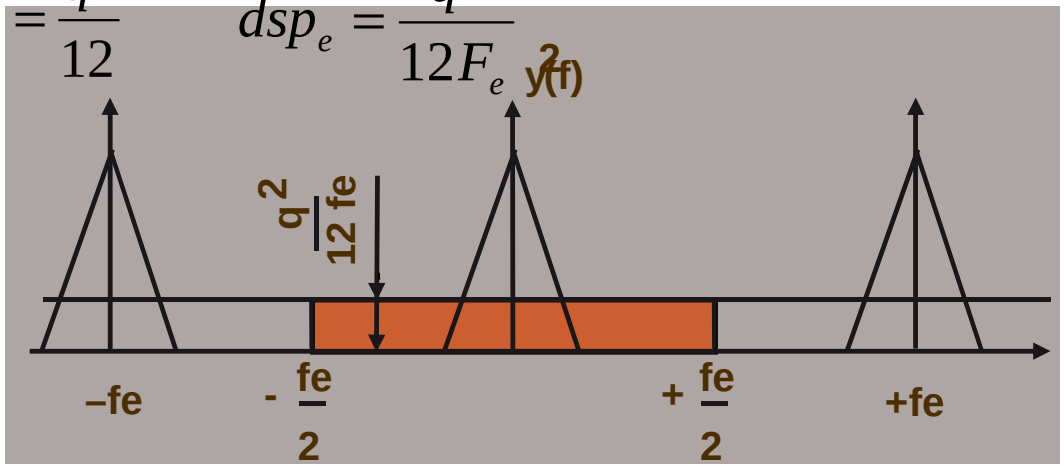



$$e = y - x$$

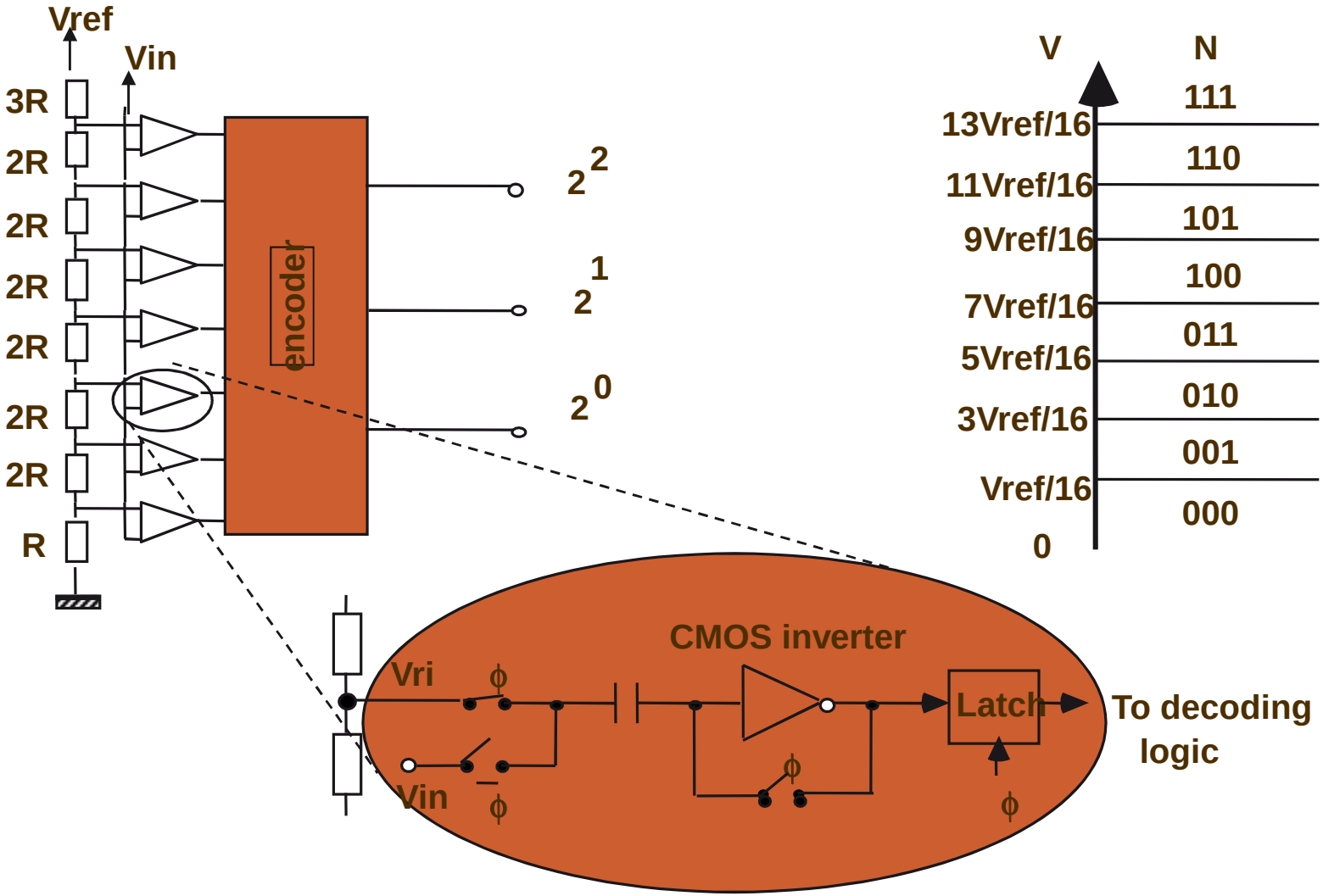
$$\sigma^2 = \frac{1}{q}\int_{-q/2}^{+q/2} e^2 de = \frac{q^2}{12} \qquad P_e = \int_{-Fe/2}^{+Fe/2} dsp_e df = \frac{q^2}{12} \qquad dsp_e = \frac{q^2}{12F_e}$$



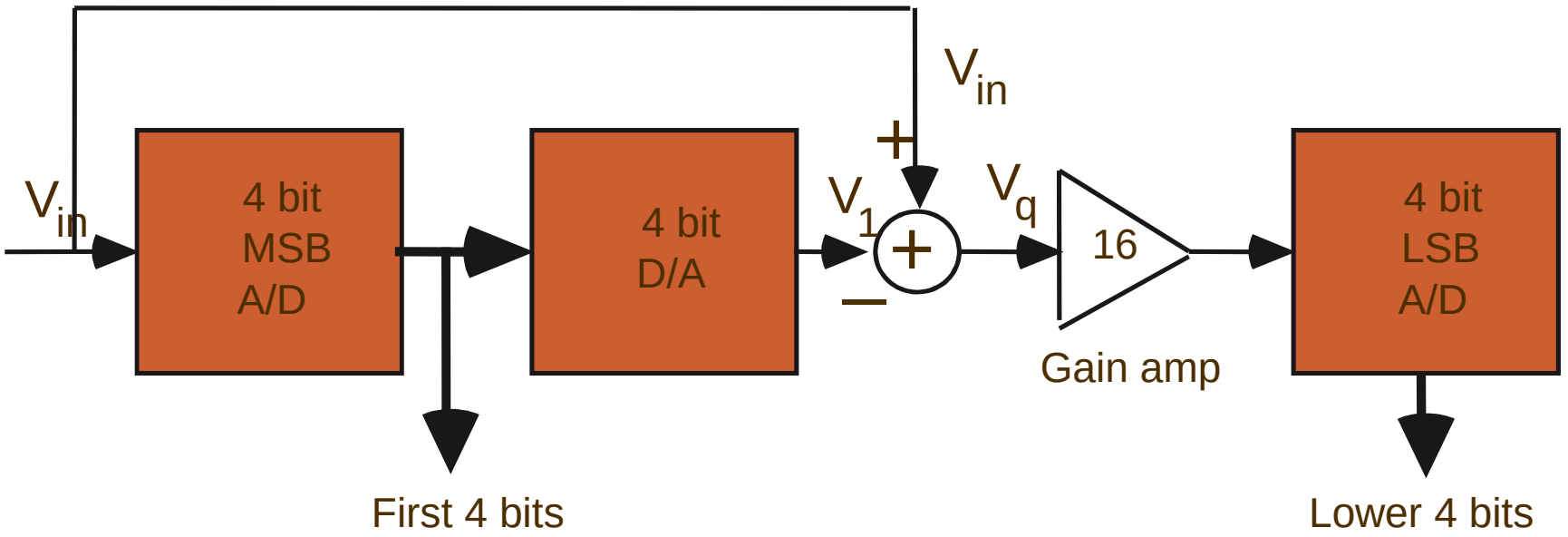




Quantization noise power: $q^2/12$

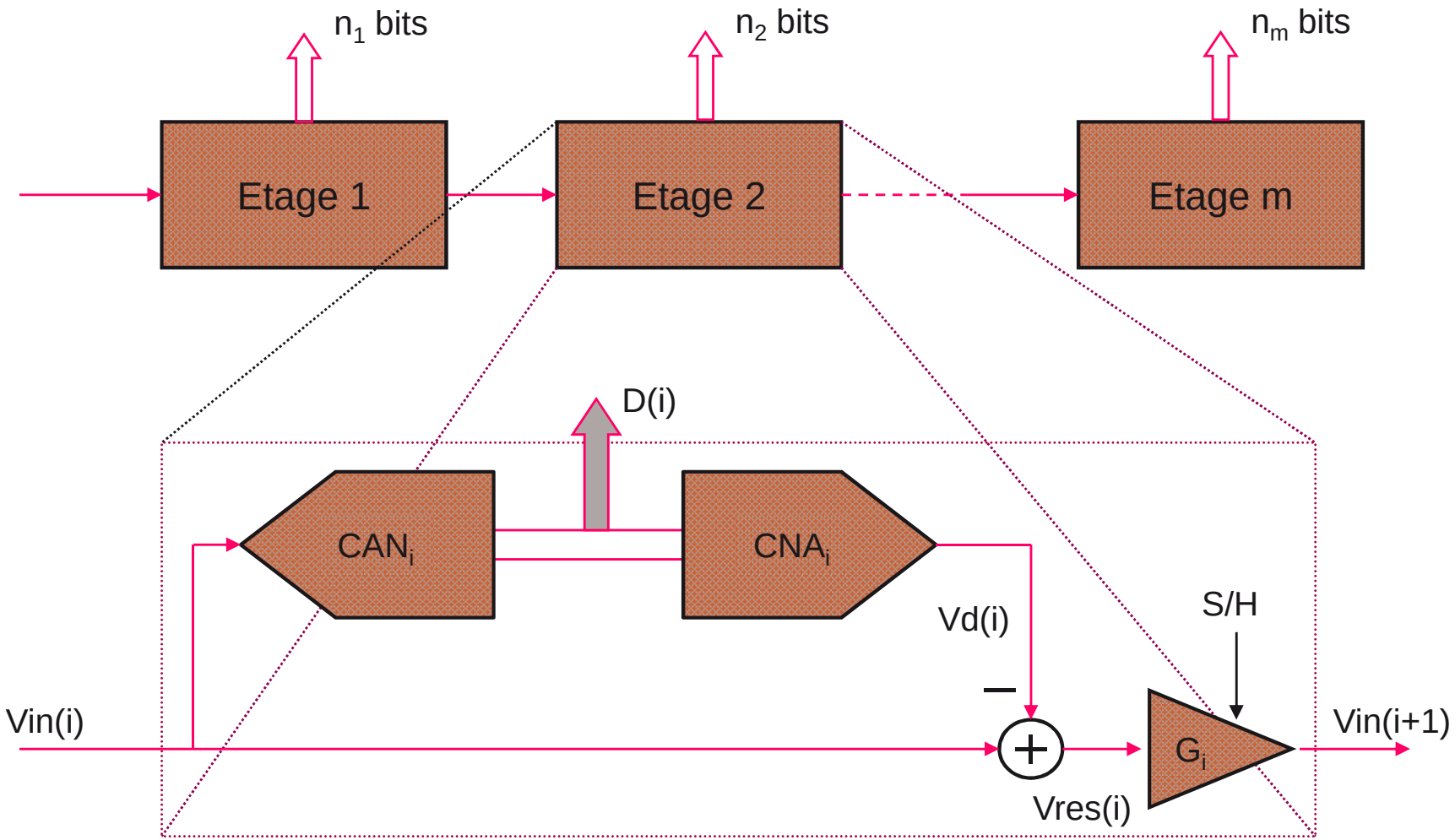
# Flash ADC


Vref
Vin
3R
2R
2R
2R
2R
2R
2R
R
encoder
$2^2$
$2^1$
$2^0$
V
N
13Vref/16
11Vref/16
9Vref/16
7Vref/16
5Vref/16
3Vref/16
Vref/16
0
111
110
101
100
011
010
001
000
CMOS inverter
Vri
Vin
ϕ
Latch
To decoding logic

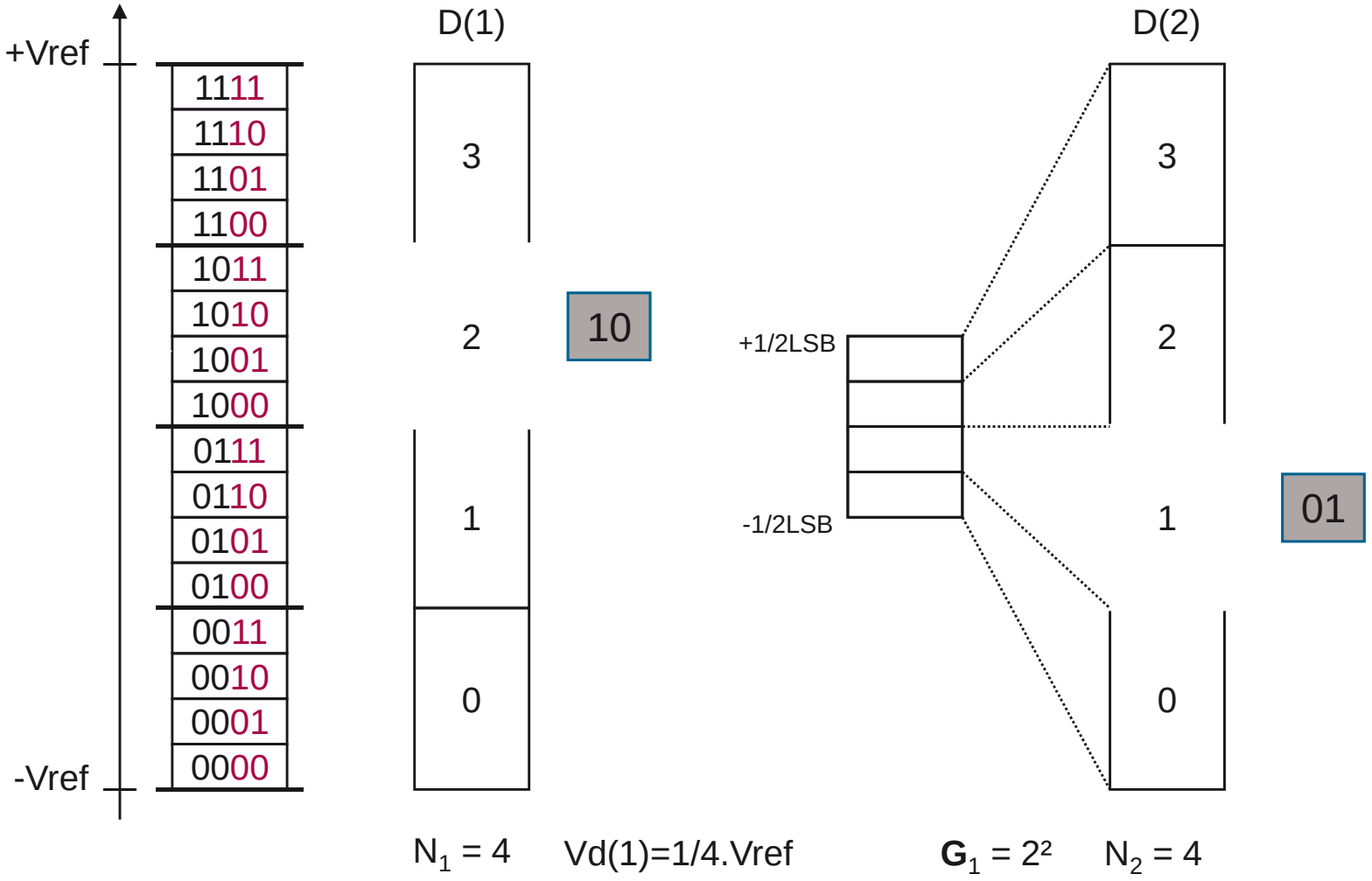
# Subranging (or two-step) ADC



# Principe du CAN pipeline

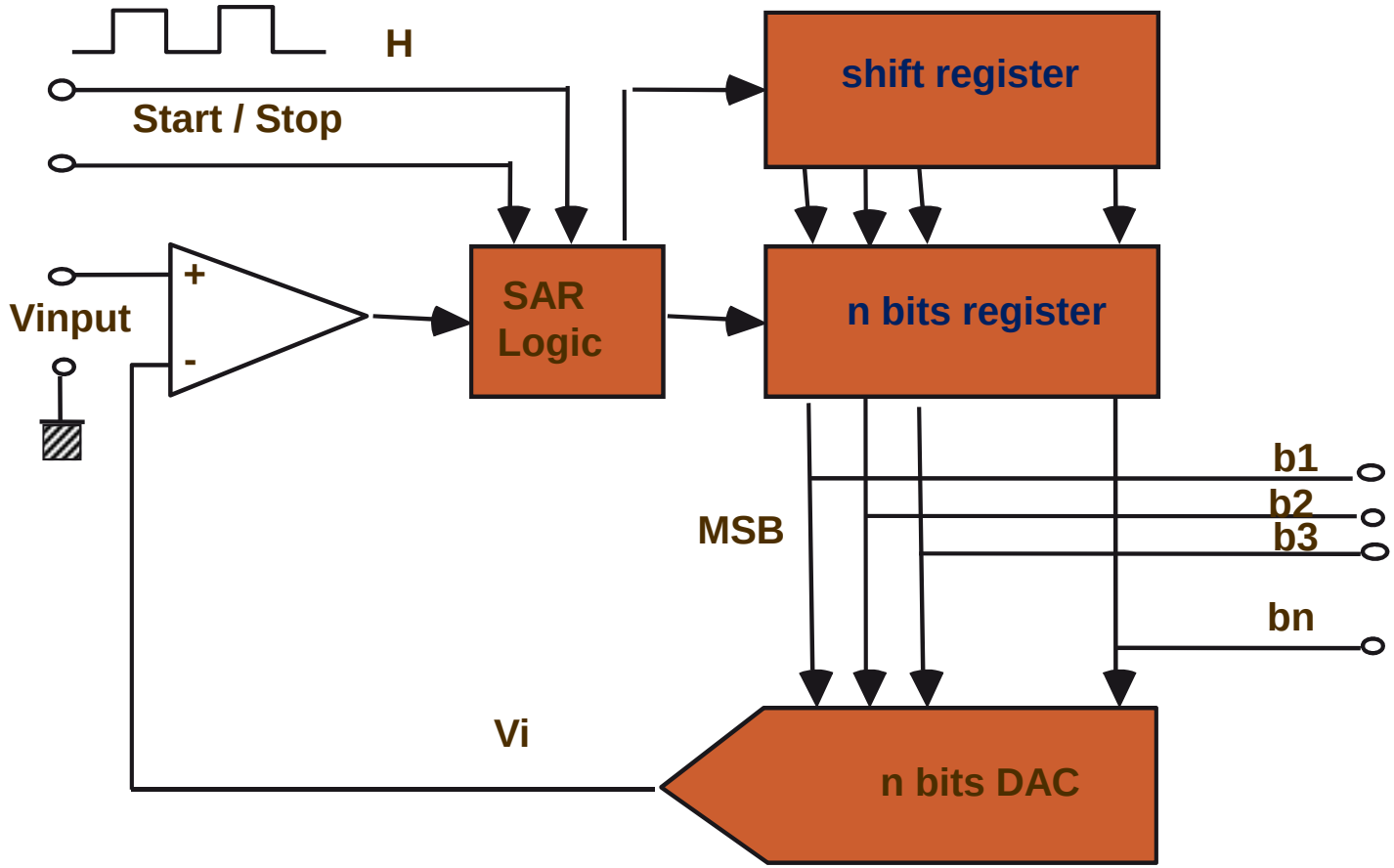


# Exemple d'un convertisseur à deux étages



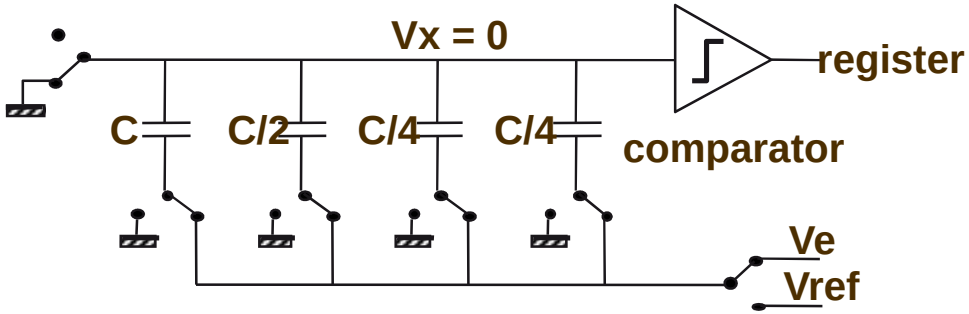

$N_1 = 4$ Vd(1)=1/4.Vref $G_1 = 2^2$ $N_2 = 4$

# Successive-approximation-register (SAR) ADC

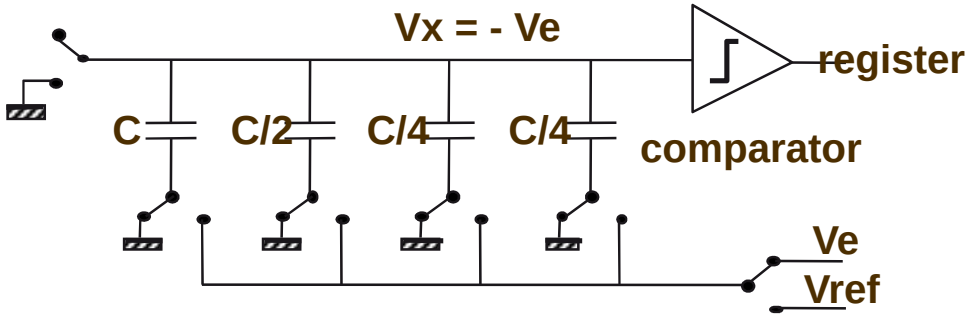


# Charge redistribution ADC

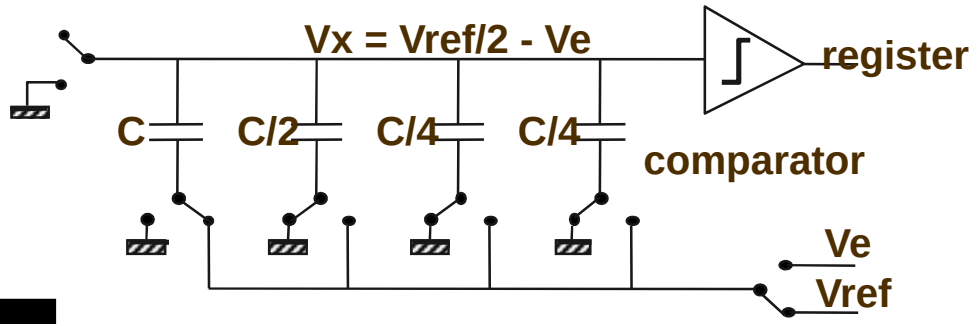
1. Sample mode



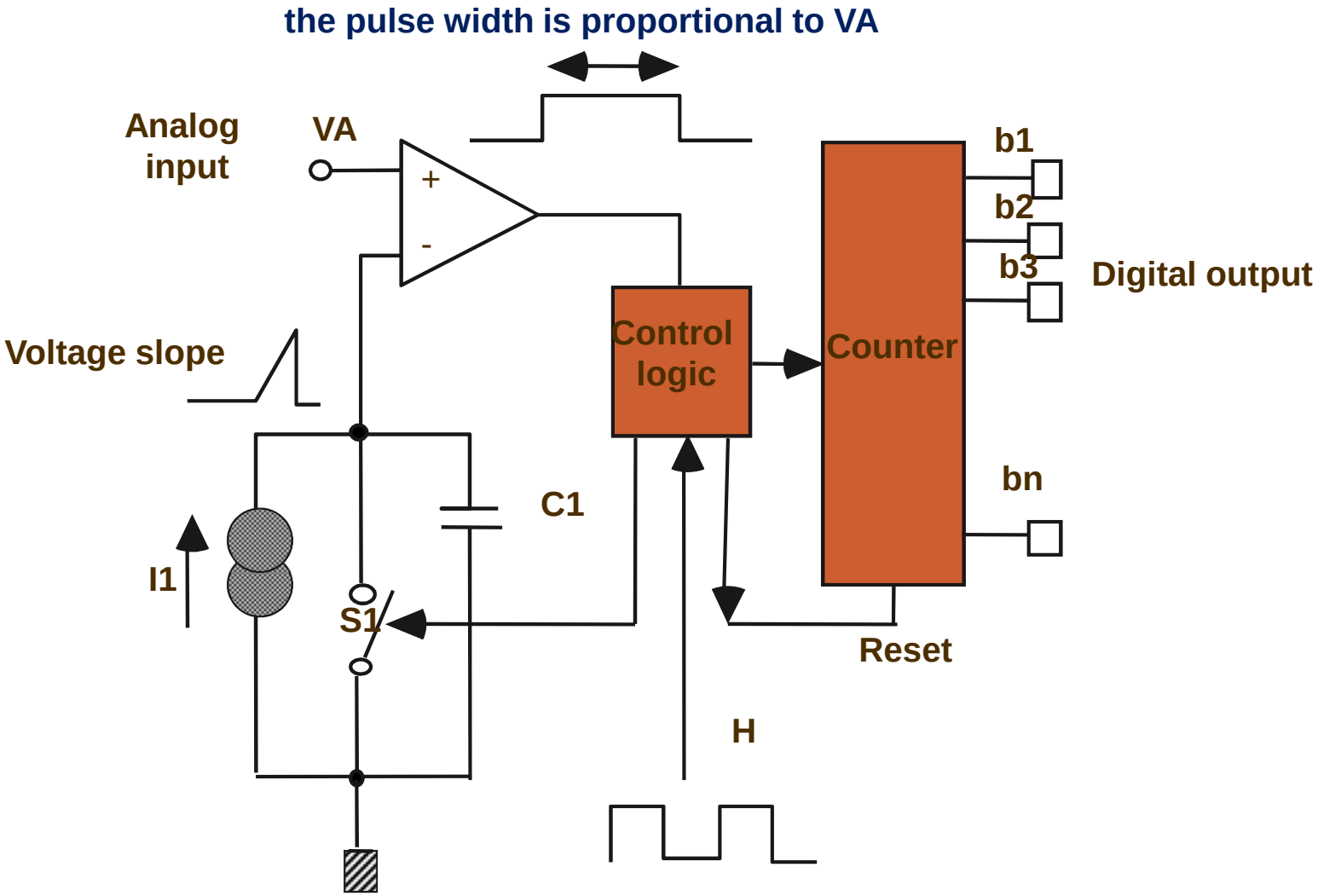

2. Hold mode



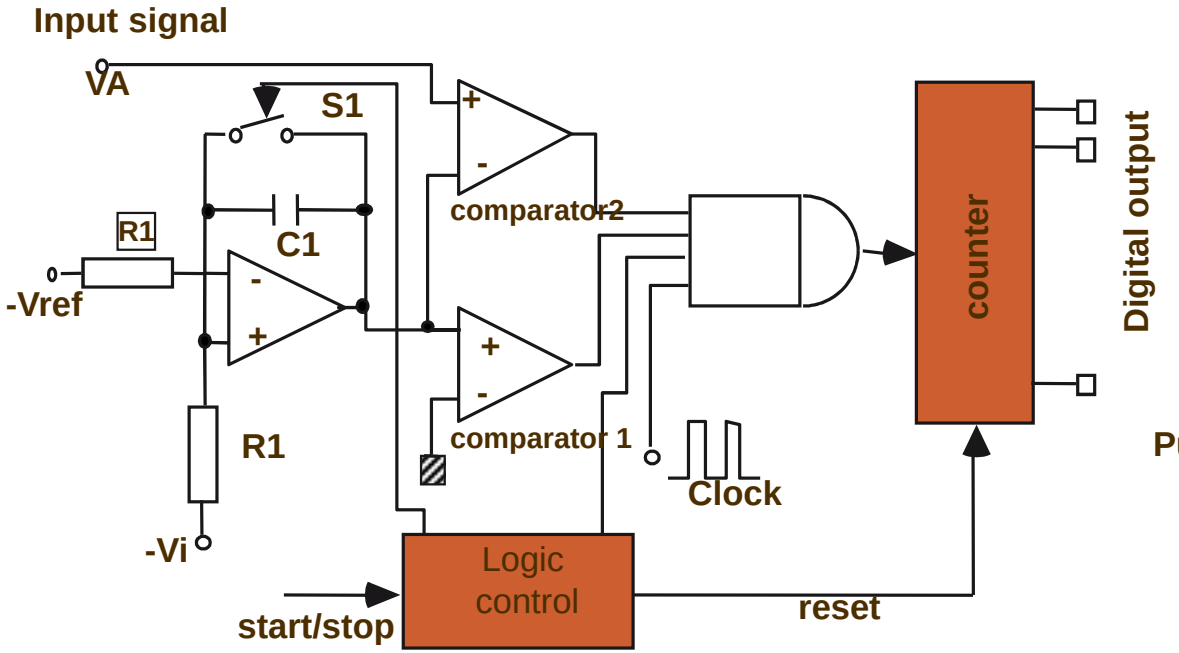

3. Bit cycling

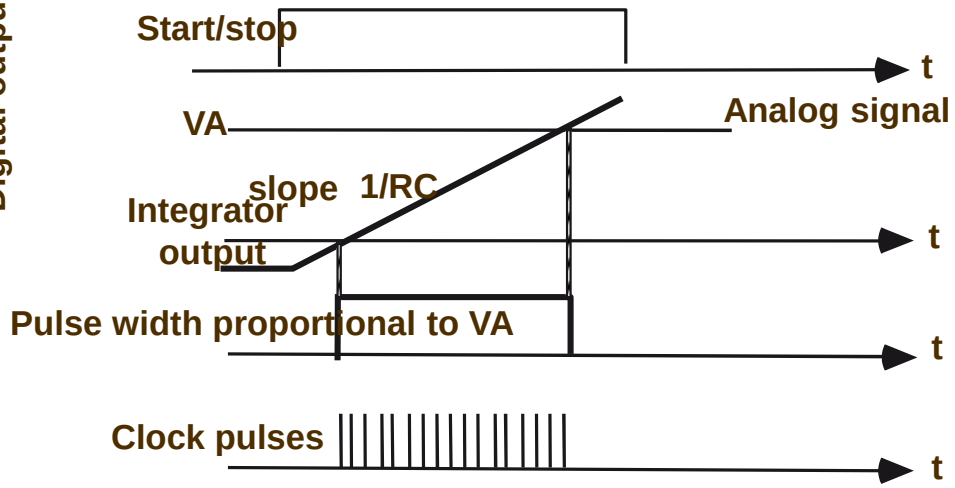


# Integrating ADC

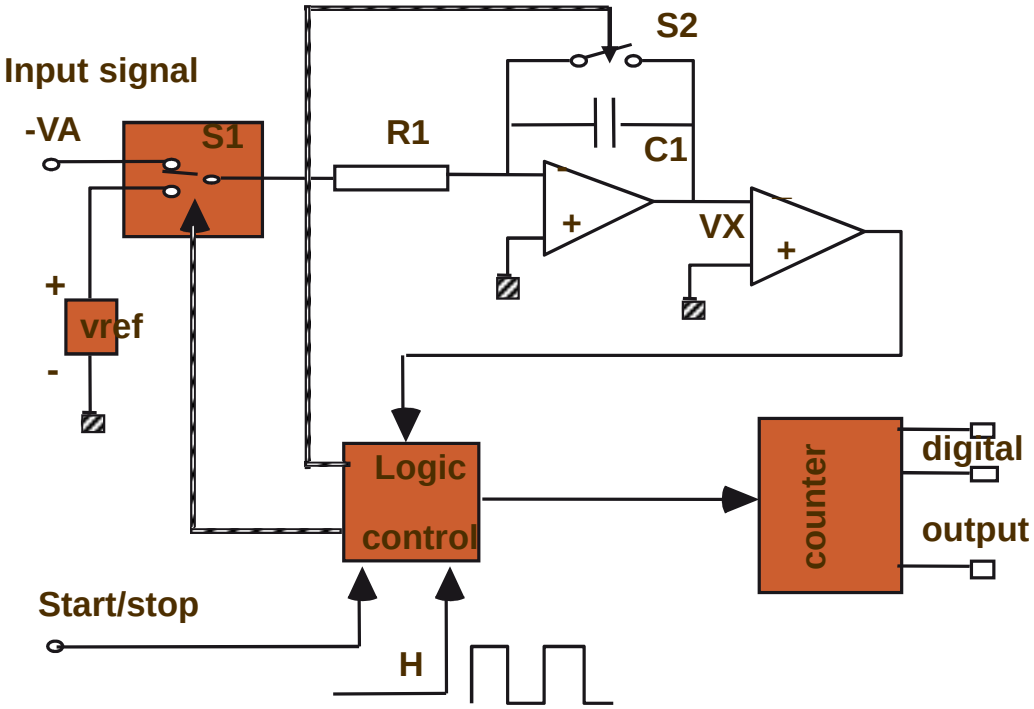


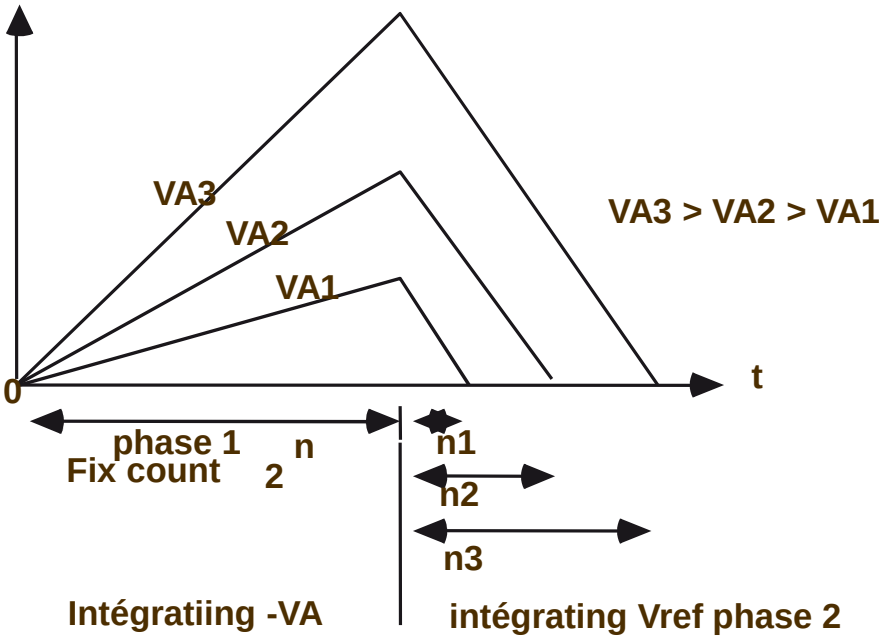
# Single slope ADC



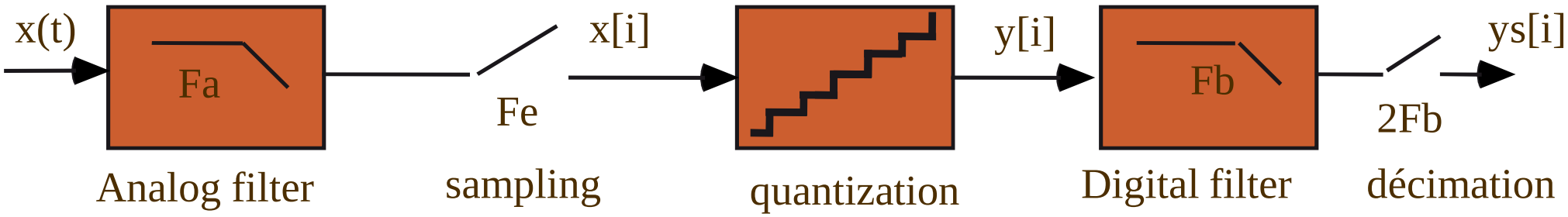



# Dual-slope (integrating) ADC



# Oversampling ADC




Technology evolution →

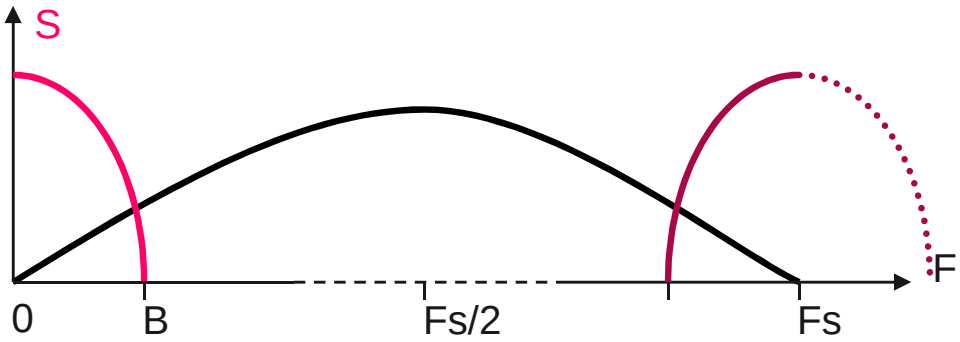
+ speed
+ density
- Dynamic ( 3V, 16 bits → 45 µV )

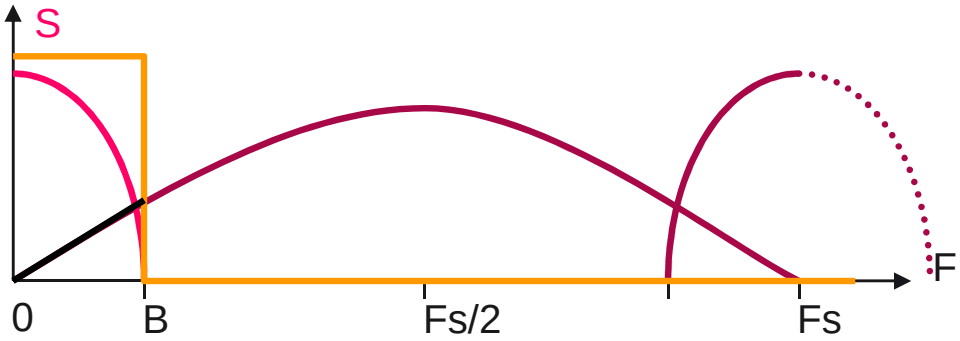
Oversampling →

Exchange :
Amplitude resolution
↓
Digital complexity and resolution in time

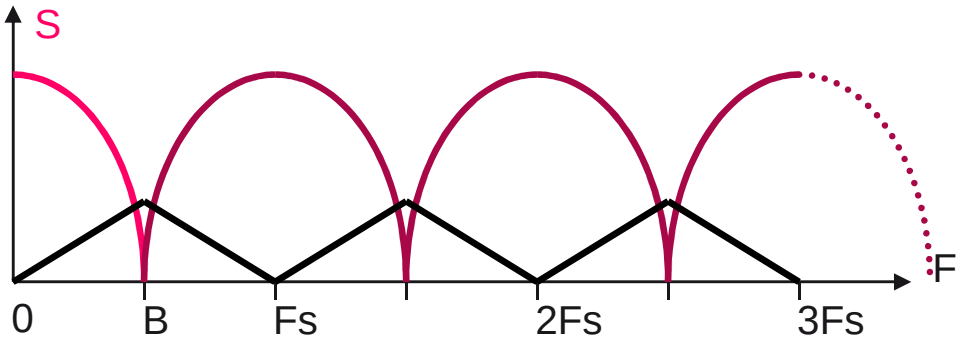
# Decimation and digital filter

- **Filter**
  - *Delete any signal and noise out of band*




- **Decimation**
  - *Reduce the sampling rate to Fs=2×B*

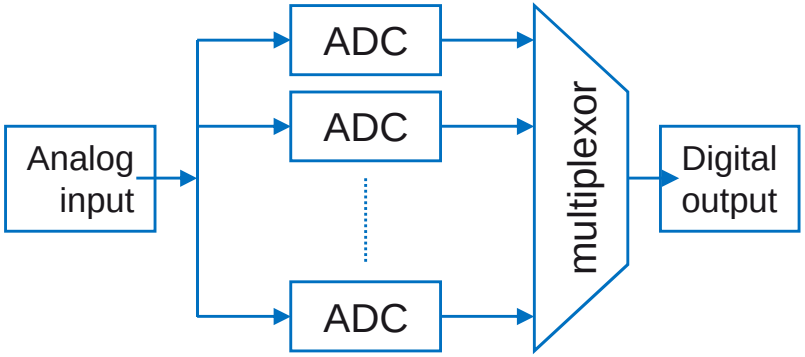


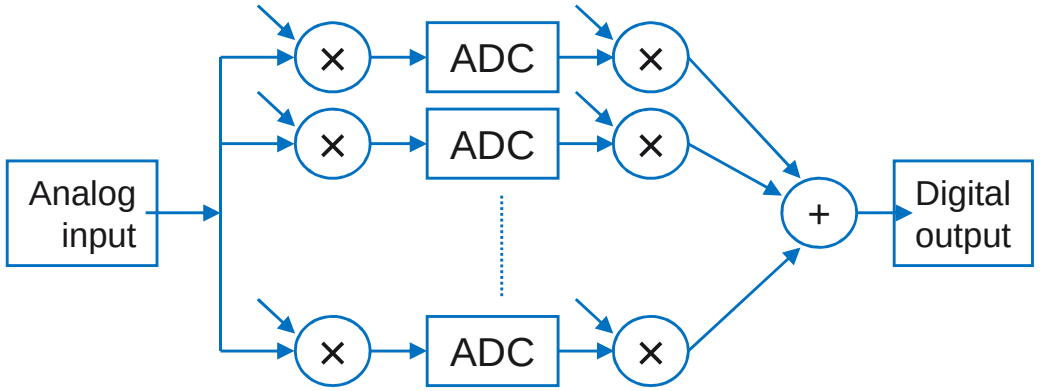
# Parallel ADC

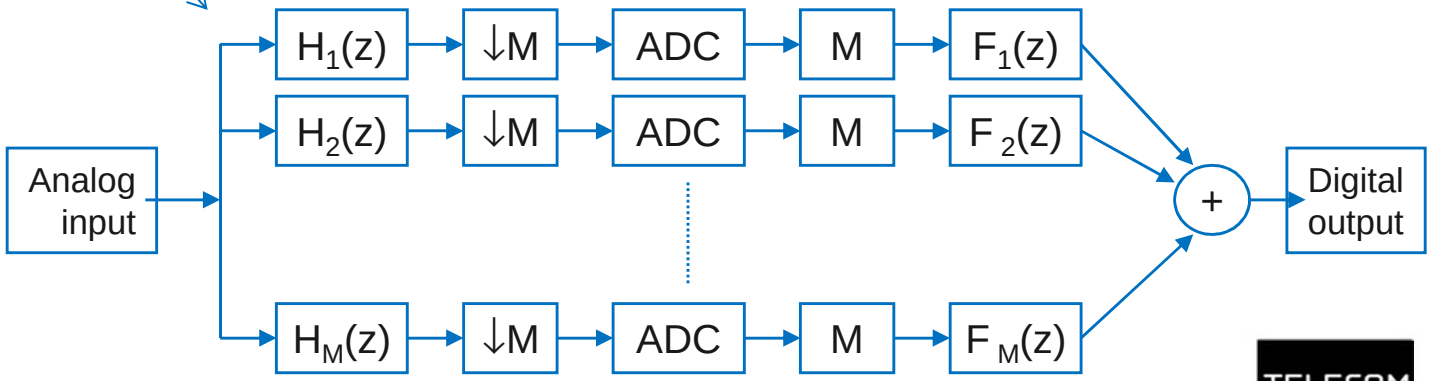
- **Time interleaved**
  - **Pipeline ADC**
  - **SAR ADC**
  - **ΣΔ ADC**
- **Modulated parallel ADC**
- **Hybrid filter bank ADC**

- **Parallel ADC :**

  **the most flexible**
  - **In each channel**
  - **Number of channels**

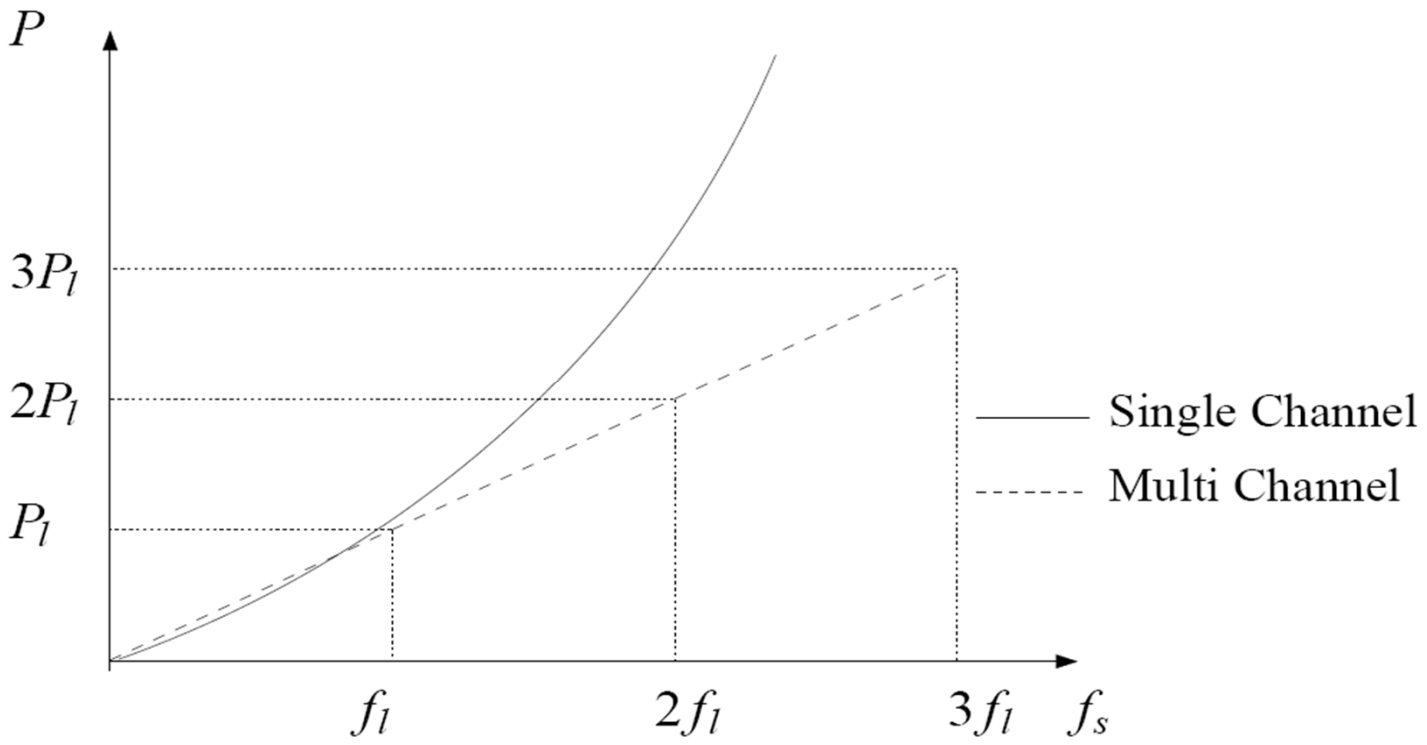


# Parallel ADC : advantages

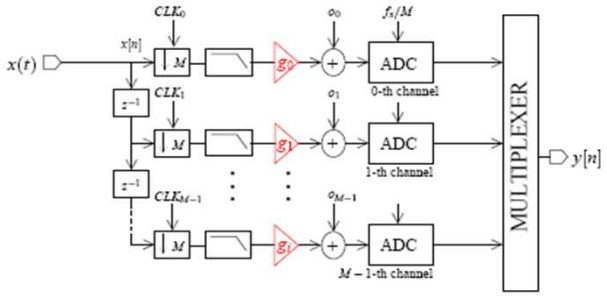
- Speed : multiplied by the number of channels
- Power consumption : linear increase
- Flexibility



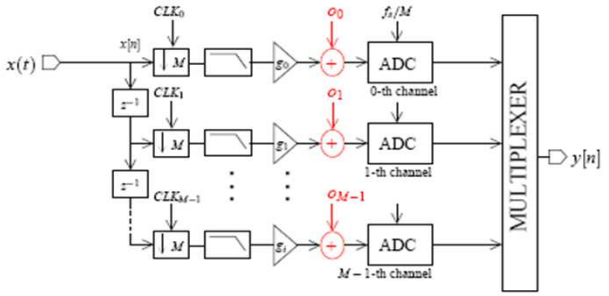
# Parallel ADC : drawbacks

- **Due to circuit imperfections, the channels do not match**

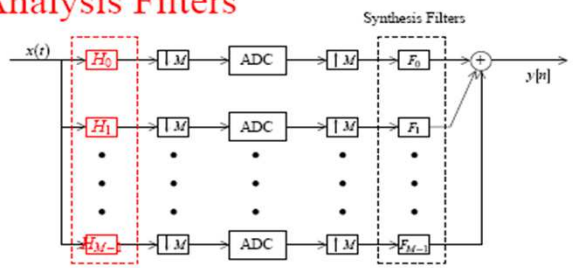
Gain Mismatch



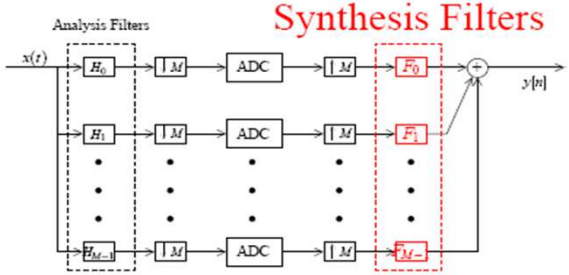

Offset Mismatch



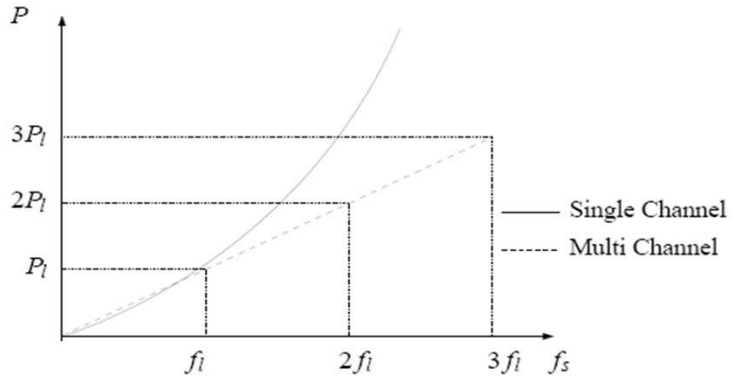

Analysis Filters



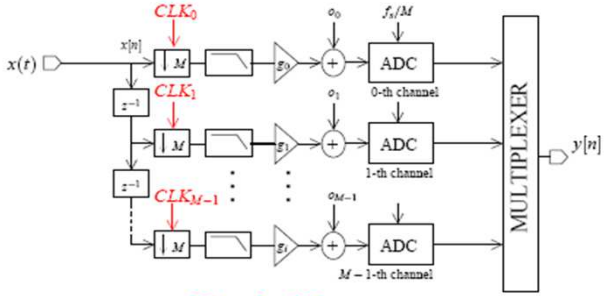

Synthesis Filters



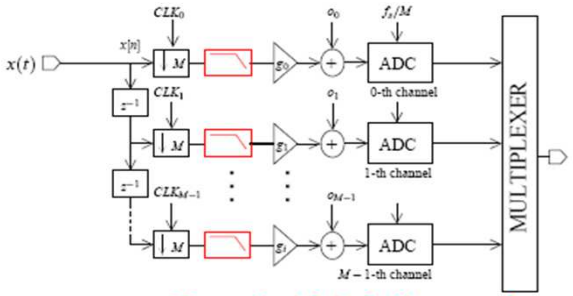

Synthesis Filters



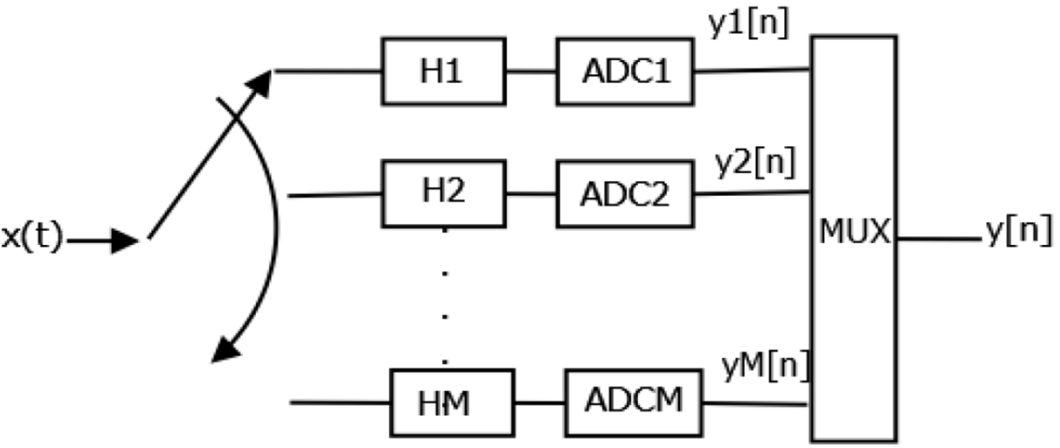

Clock Skew



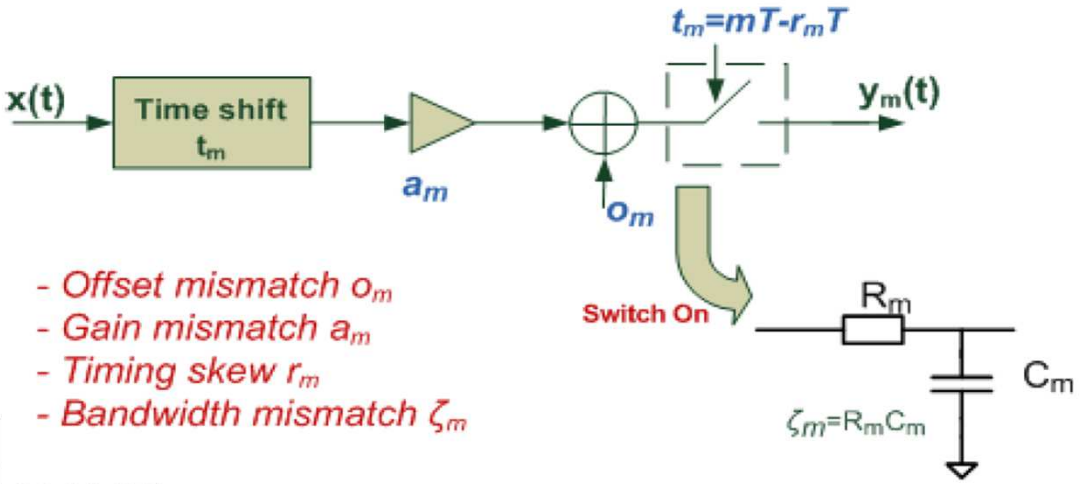

Bandwidth Mismatch



# Parallel implementation



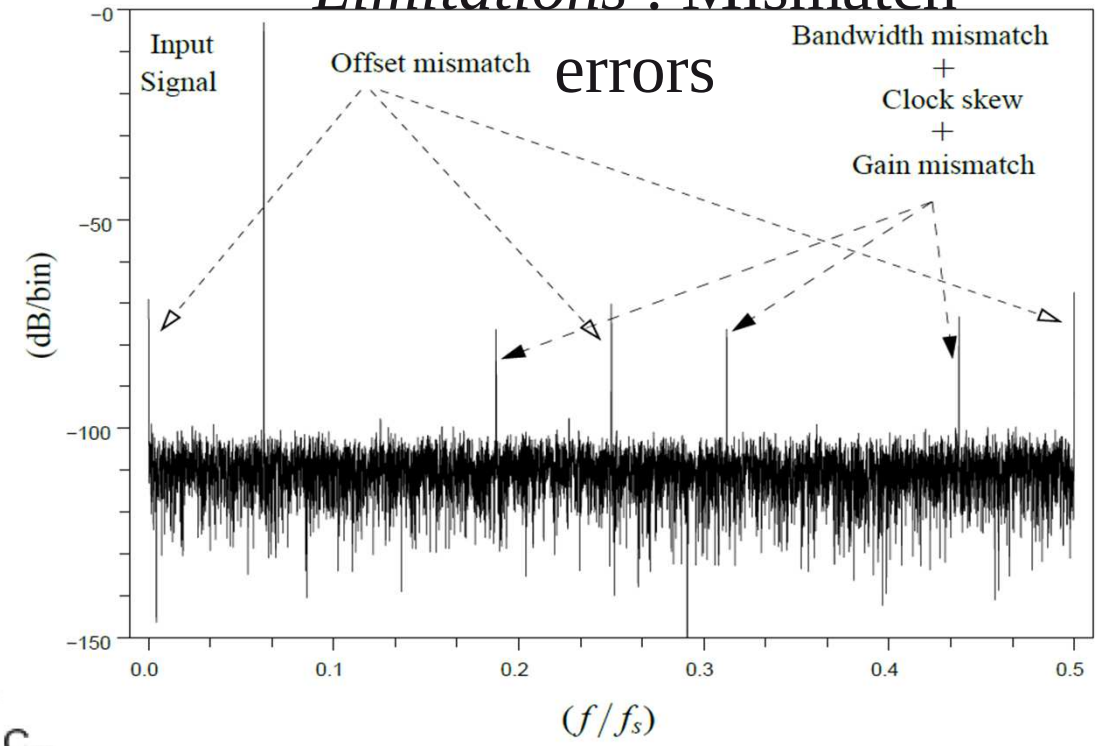

**Time-Interleaved Architecture**




- *Offset mismatch* $o_m$
- *Gain mismatch* $a_m$
- *Timing skew* $r_m$
- *Bandwidth mismatch* $\zeta_m$

*Advantage* : Speed × M

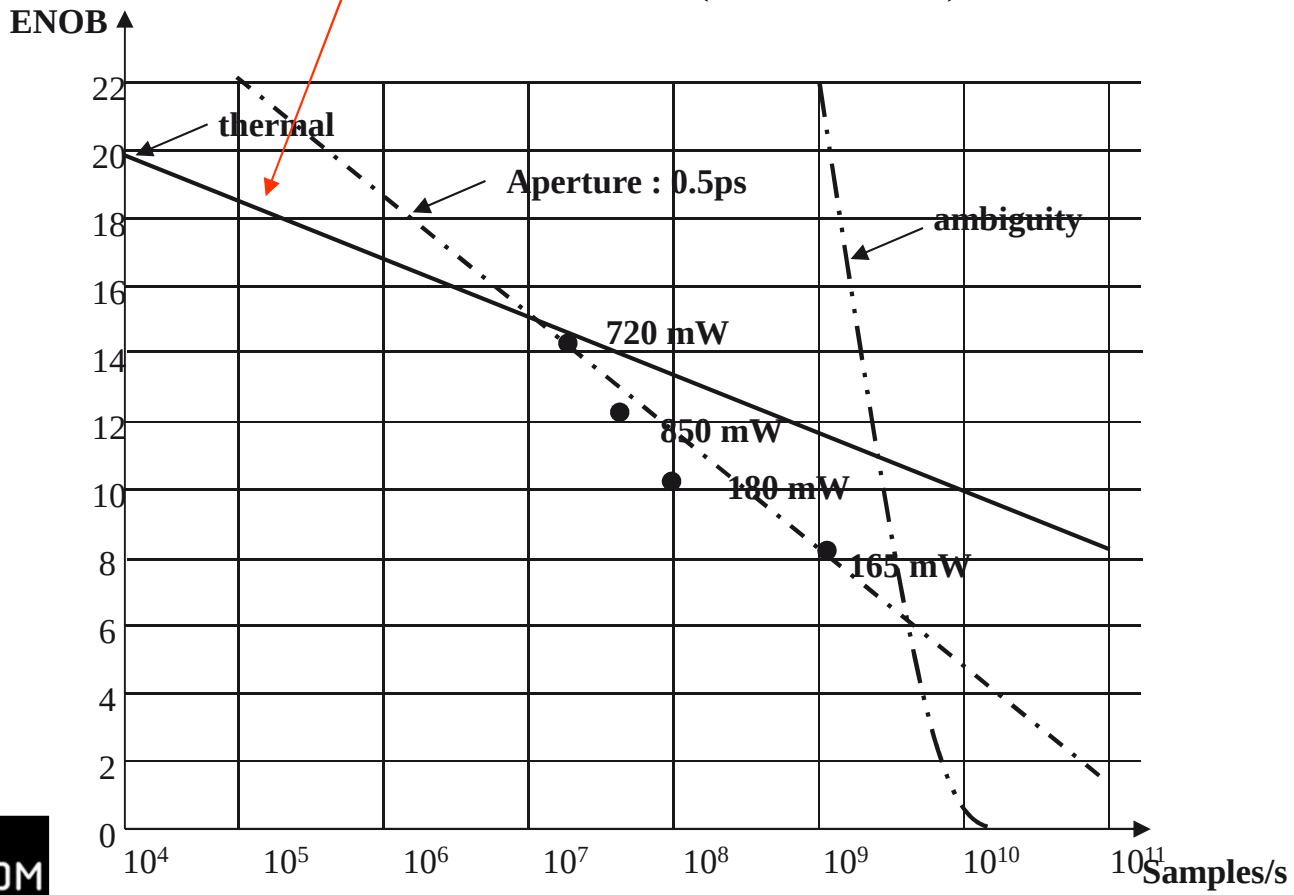
*Limitations* : Mismatch errors




**additional tones caused by the presence of all mismatch errors**

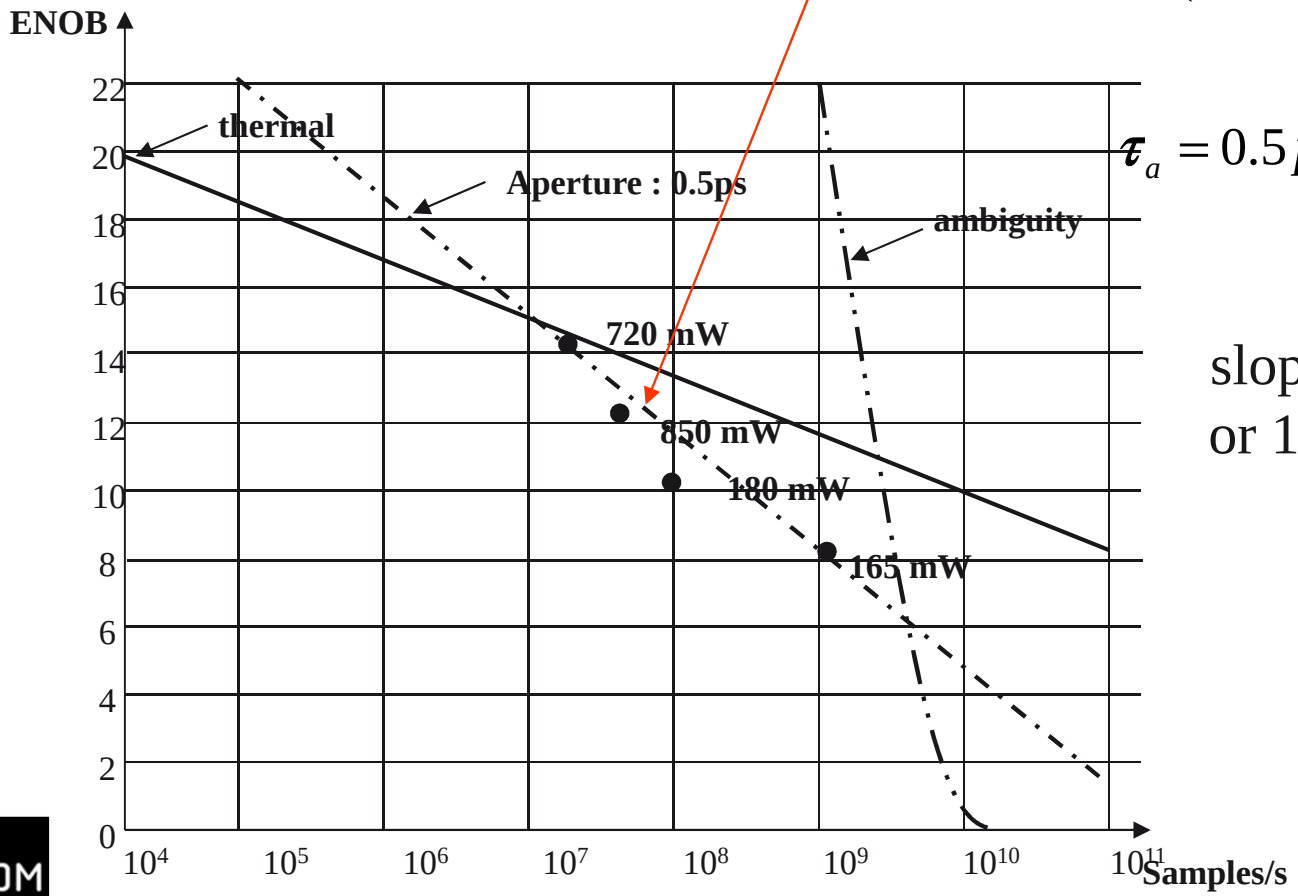
# ADC Effective Resolution versus Sample Rate

Thermal noise: $\log_2\left(\frac{V_{FS}^2}{6kTR_{eff}F_s}\right)^{1/2} - 1.$



# ADC Effective Resolution versus Sample Rate

Aperture uncertainty of the sampling: $\log_2\left(\frac{2}{\sqrt{3}\pi F_s \tau_a}\right) - 1.$



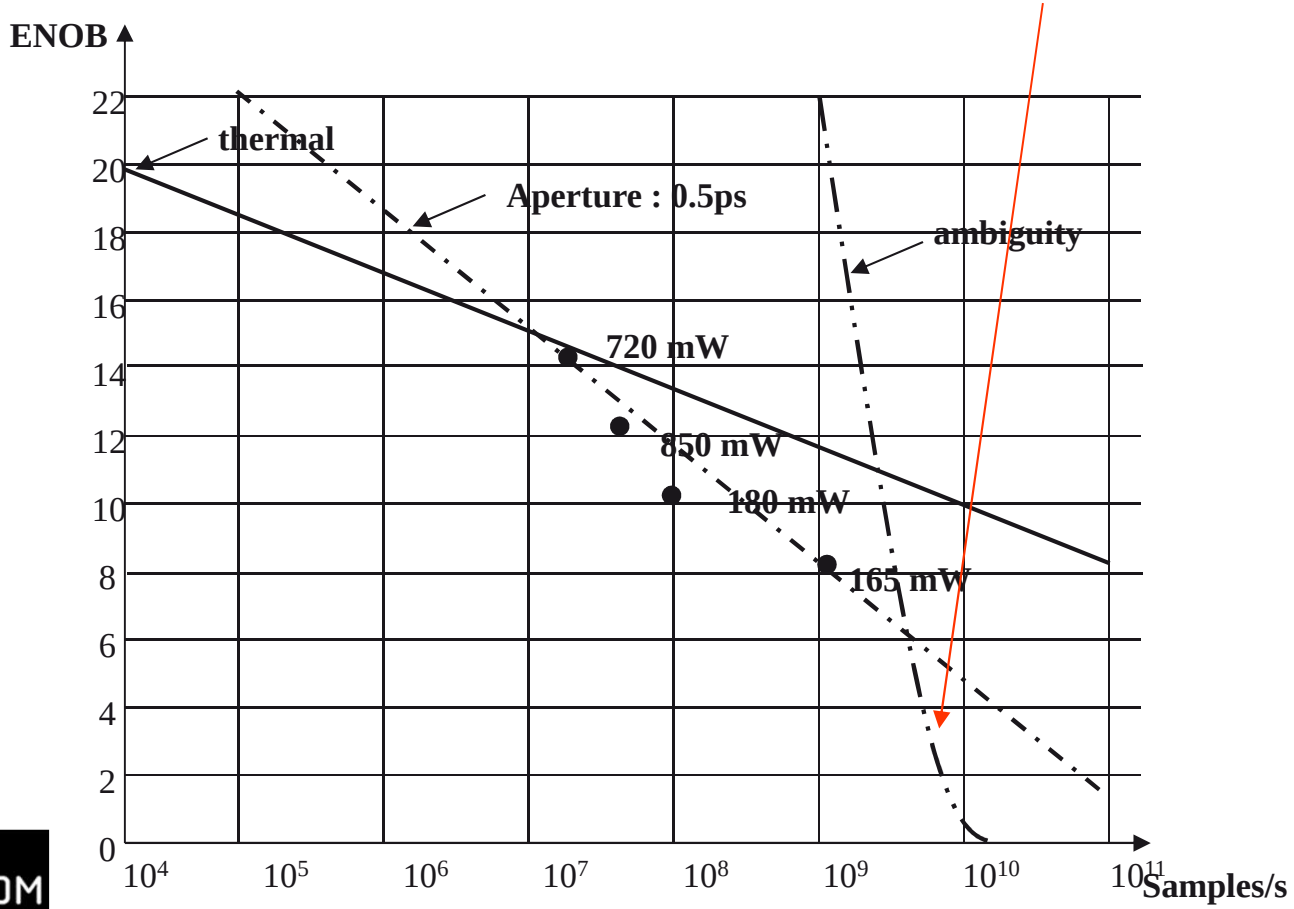

$\tau_a = 0.5\,ps$ : jitter of the clocks

slope : -1 bit / octave
or 10 bits / 3 decades

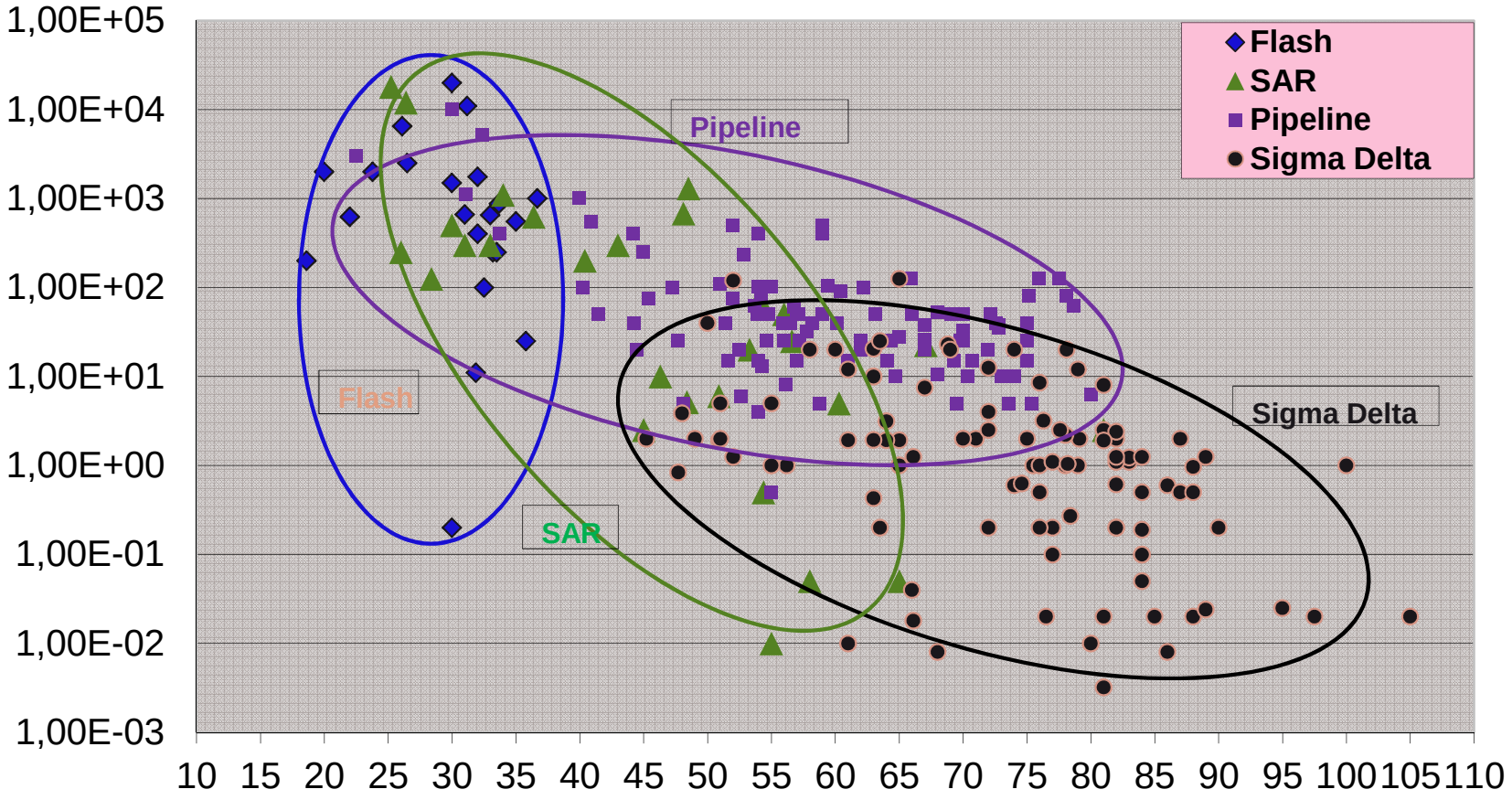
# ADC Effective Resolution versus Sample Rate

Comparator effect:

$$\frac{\pi f_T}{7F_s} - 1.1.$$



# State of the art ADC : 2000 - 2015



# ADC merit factor

- **Limitation with the energy by conversion step :**

**FoM = P / $2^n$ $F_s$**

**Example :**

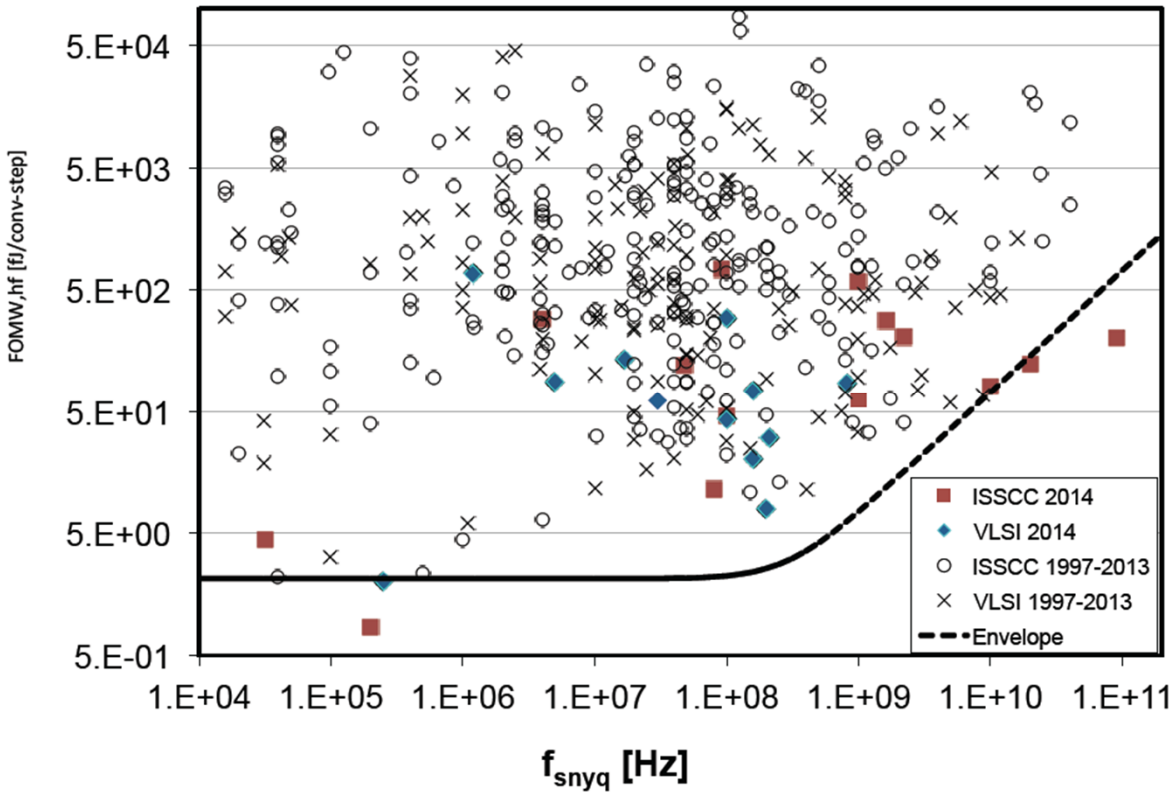
**Fs = 1 GHz**

**FoM = 5 fJ/conv-step**

**ADC 10 bits**

**P = 5 mW**

**in the best case**




B. Murmann, "ADC Performance Survey 1997-2014," [Online] Available: http://web.stanford.edu/~murmann/adcsurvey.html

# Conclusion

- ADC applications ⇒ Mobile phone, base stations, radio receivers
- BiCMOS technology is OK
- FD SOI is starting
- In future : cognitive radio applications
- Superconducting ADC : 5 Kelvin, ΣΔ ADC, Fs=12.8GHz,  OSR=64, 14 bits.