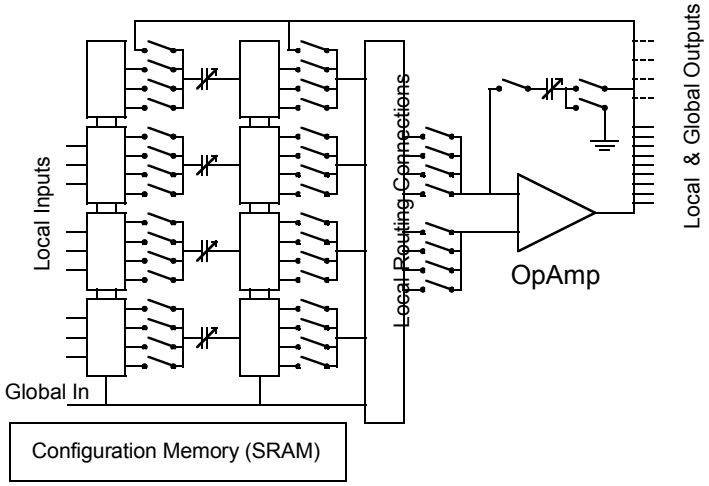
AnadigmDesigner® IPmodule Manual Library - Anadigm® A

Anadigm® is pleased to invite all engineers into a completely new realm of analog circuit design. The three dimensions of this new world are: the AnadigmDesigner® application, the Anadigm® family of Field Programmable Analog Arrays, and the IPmodule library.

AnadigmDesigner® is the software portion of the system in which you capture your design. Anadigm® FPAAs are the physical elements in which your design is realized. The ever growing library of IPmodules are the heart of the system. IPmodules contain building block analog functions in which all the relevant parameters are programmable.

Within an Anadigm® Field Programmable Analog Array (FPAA), there are a finite number of elements, but a nearly infinite number of ways to connect them. As research continues, the IPmodule library continues to grow. With each new array designed, the library doubles again. Exponential growth… exceptional products.

The Configurable Analog Block (CAB) pictured to the right, represents one of many switched capacitor sub-circuits arrayed together to form a complete Anadigm® FPAA device. The available programmable elements include input capacitors, feedback capacitors, voltage references, clock and routing structures. On chip SRAM bits control each of these elements. Further, there are elements which switch dynamically, orchestrated by a sophisticated internal clocking architecture. To add a final layer of flexibility, the user can construct a system in which the FPAA is reprogrammed, rapidly adapting the circuit to new signal environments or system demands, under the control of a host processor.



IPmodules each represent a circuit function, typically with several user programmable parameters, which are realized within one or more CABs. The IPmodules described within this library manual represent only a starting series of foundation class circuits being investigated. It is just the beginning point for this new technology.

As amazing as this new technology is, we at Anadigm® realize that we have only created a context within which even more creative minds can work. We value both our well established and growing base of university, corporate and individual research partners who add regularly to the library of IPmodules and complete circuits. We have taken great care in constructing an open system that allows easy inclusion of these new library elements as they each become available and characterized. This manual contains just the first collection.

Please be sure to register yourself as an AnadigmDesigner® user. We'll be sure to keep you tuned in to all the latest news on our arrays, available circuits and IPmodules. We'll also soon be rolling out a program in which a much broader base of contributors will be invited to add to the already significant pool of knowledge and design experience. We've started an incredible new chapter in circuit design, and we want you to be part of this history.

While every effort is made to ensure that our publications are free from defects, the IPmodule library gets frequent additions. To be sure you are referencing the most current IPmodule information, please use the on-line help files that are distributed with the library itself.

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Introduction

IPmodules are small building-block circuits that can be selected, moved about the screen, placed and wired. You will build your circuits from the IPmodules delivered with AnadigmDesigner®.

There are 6864 electronic switches on the AN10E40 that enable the creation of a broad range of analog functions. Working at the individual switch level can be tedious however so we have created a library of building block circuits in which internal switches have already been set. One of the building blocks, for example, is a gain stage.

There are some 200 switches that need to be set on or off to make one of the chip zones behave as a simple gain stage. Each switch setting is represented by one or more bits. Here are two examples of the hexadecimal (each character represents 4 bits) representations required to express an IPmodule:

IPmodule	**Bytes**
Simple gain stage	**003f c040 0022 ff24 1000 0ff3 fc00 0018 2270 01c0 0805 2090 8000**
Rectifier	**003f c040 0082 ff20 1000 0ff0 0000 0080 2a70 01c0 0000 2090 9500**

By creating the IPmodule library, we have made it easy for you. All you have to do is use AnadigmDesigner® software to select an IPmodule, place it, wire it up, and set its parameters using the “Set IPmodule Parameters” popup window.

VMR vs. AVSS

There is simple point to make about the architecture, but one that on occasion causes a bit of confusion. All analog processing within the AN10E40 is with respect to Voltage Mid-Rail (VMR). VMR is 2.5V above AVSS. (AVSS, SVSS, BVSS, CFG_VSS, ESD_VSS are all at the same 0V potential.) So in the following IPmodule descriptions, a "positive" voltage, implies positive with respect to VMR. Likewise, a "negative" voltage is any potential below VMR.

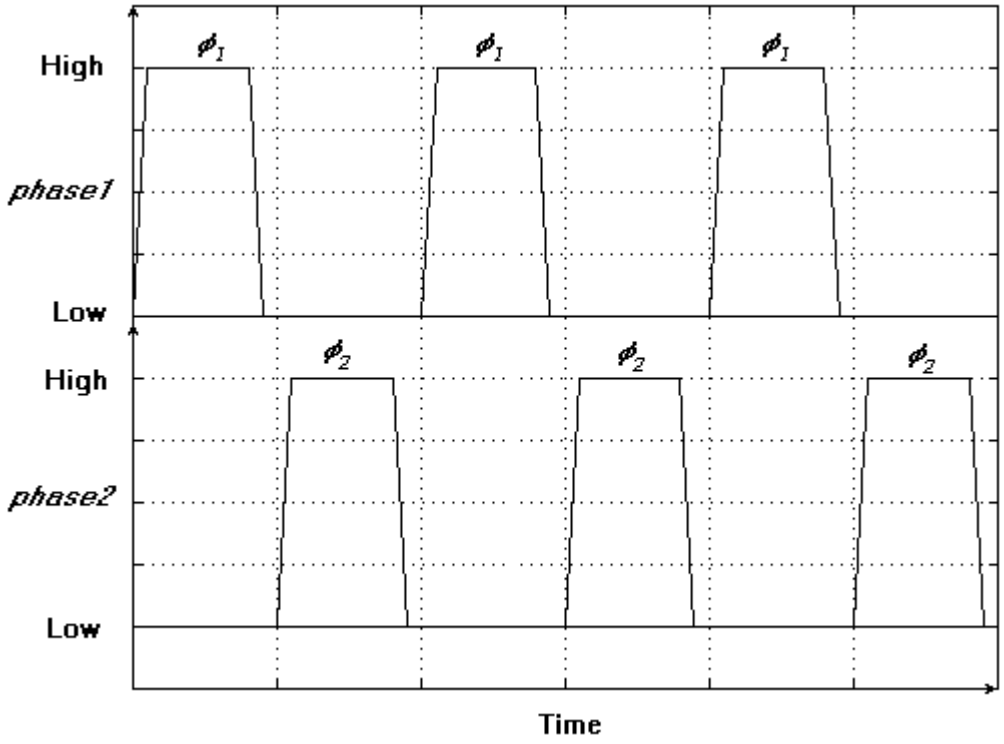
In the unlikely event that your signal processing requirements dictate that VMR be set at some other voltage besides 2.5, the AN10E40 provides an external OpAmpVMR input pin for connection from an external source and a configuration memory bit to disable the on board generator.

Clock Phases

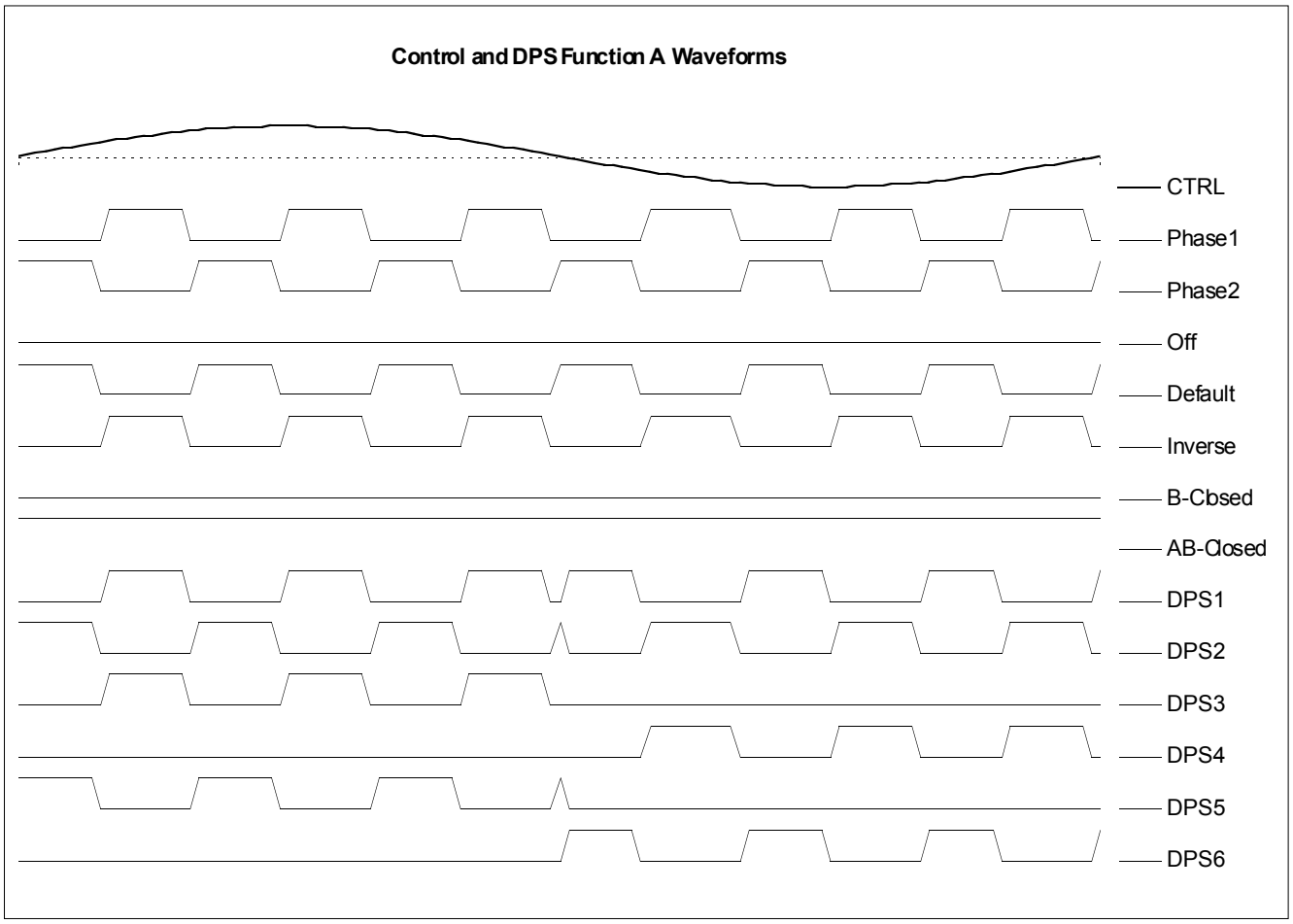
Throughout this manual, you will see references to $\phi 1$ and $\phi 2$ clocks. These are symbols for the two non-overlapping phases of the clock that is driving the IPmodule under study. In any sampled data system, analog signals are broken up in time, and may not be continuously valid. For such IPmodules, the output is defined to be valid in one of these two phases. This is important when wiring up to a downstream IPmodule. Specifically, a circuit in which a valid-in-$\phi 2$ signal feeds an IPmodule which samples only on $\phi 1$ would obviously yield undesirable results.

Digging Deeper

The switched capacitor circuit is controlled with a two phase clock. The high value of the clock signal closes a switch and the low value opens it. The two phases in which the clock has a high value are represented in this documentation with the symbols $\phi 1$ and $\phi 2$. Each dynamic switch of the circuit may be programmed to remain statically open, statically closed or controlled only by one of these phases. The following figure shows the waveforms of $\phi 1$ and $\phi 2$. Note that the phases do not overlap each other (there is a non-overlapping period in which both phases have low value.



Some circuits may require swapping or stopping the controlling clock phases of some switches. This is referred to as Dynamic Phase Swapping or stopping (DPS). This dynamic phase swapping or stopping is represented with special phase names as shown below.



The signals *DPS1* to *DPS4* have a transition point in which the controlling signal (top of the above figure) changes signs. Note that when the controlling signal reaches the value of zero (0) the phase is instantly swapped (signal goes to zero) without waiting for the current phase to terminate. There are four DPS types as depicted on the above figure:

DPS1 - when the controlling signal has a positive value the clock is in phase1 and when the controlling signal has a negative value the clock is in phase2.

DPS2 - when the controlling signal has a positive value the clock is in phase2 and when the controlling signal has a negative value the clock is in phase1.

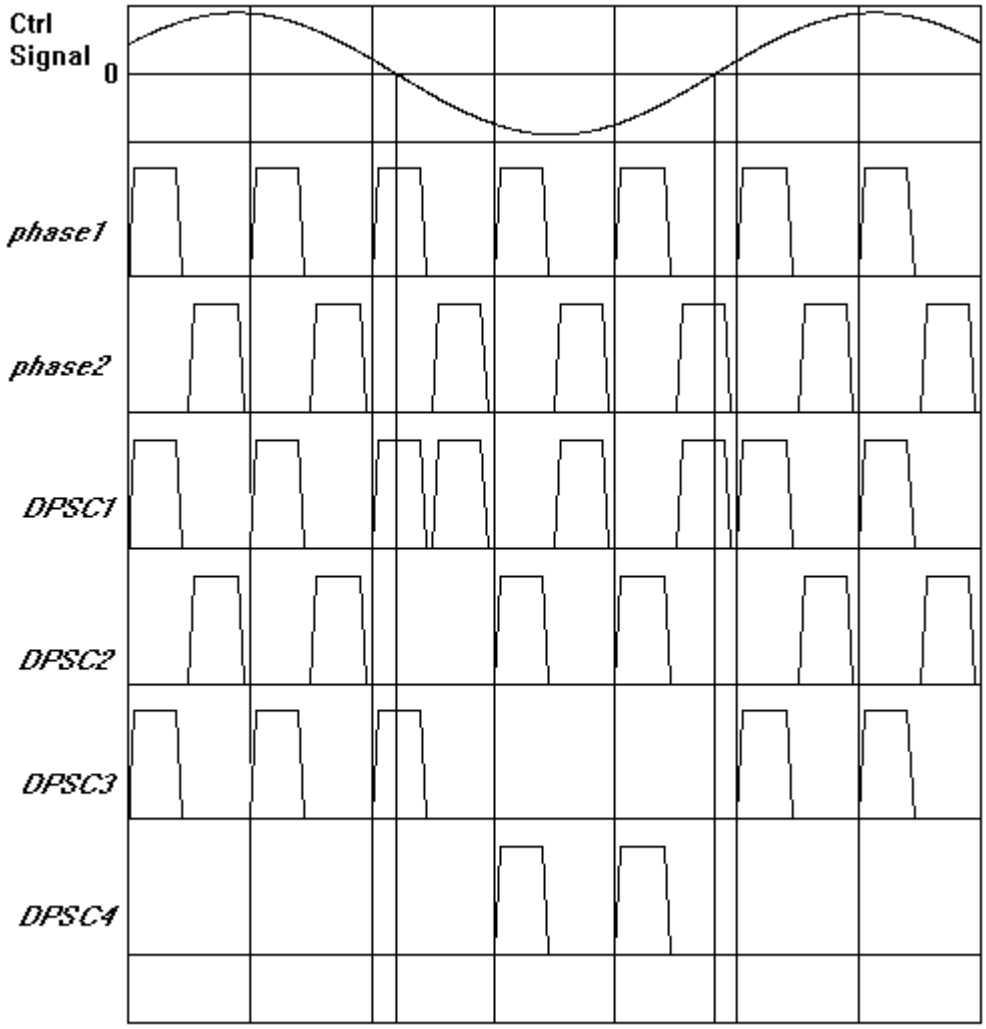
DPS3 - when the controlling signal has a positive value the clock is in phase1 and when the controlling signal has a negative value the clock has a low value (the controlled switch is open).

DPS4 - when the controlling signal has a negative value the clock is in phase1 and when the controlling signal has a positive value the clock has a low value (the controlled switch is open).

DPS5 - when the controlling signal has a positive value the clock is in phase 1 and when the signal has a negative value, the clock for the upper half of the MUX is low (open) and for the lower half of the MUX is high (closed).

DPS6 - when the controlling signal has a negative value the clock is in phase 1 and when the signal has a negative value, the clock for the upper half of the MUX is low (open) and for the lower half of the MUX is high (closed).

Some circuits may require that the active phase is not interrupted when the controlling signal reaches zero as shown above. In those cases the following set of DPS types is applied in which the phase swapping is synchronized with the phase 1. The signals DPSC1 to DPSC6 are synchronized with the controlling signal (Ctrl Signal) in the same way as the DPS types DPS1 to DPS6.



The IPmodule Library

AnadigmDesigner® provides an extensive library of IPmodule functions on install. However, useful new functions are being added on a continual basis. Please be sure and check the Anadigm® Microelectronic's web site for additions to the AnadigmDesigner® libraries. http://www.Anadigm.com.com

The op-amps within the CABs of the AN10E40 have a gain bandwidth limit of approximately 5 MHz. You should anticipate out-of-spec operation if your application intentionally exceeds this parameter.

C01a – Non-Inverting Comparator

This IPmodule is a full cycle non-inverting comparator. It has one input which is connected to the positive terminal of a comparator, while the negative terminal is connected to VMR. If the input is positive, the output is +2.5V, otherwise it is -2.5V. The IPmodule utilizes the CAB's op-amp in comparator mode.

Phase Behavior:

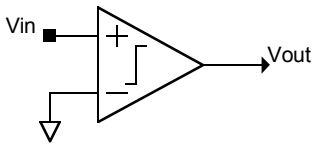
Input sampled on: $\phi 1$ and $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

To be precise, the C01a component uses a conventional analog comparator. It is not a switched capacitor circuit, so the output continuously reflects the input signal.

Programmable Parameters:

none

Circuit Diagram and Controlling Equations:



$$V_{out} = \begin{array}{ll} +2.5V & for \quad V_{in} > 0 \\ -2.5V & for \quad V_{in} < 0 \end{array}$$

C01b – Inverting Comparator

This IPmodule is a full cycle inverting comparator. It has one input which is connected to the negative terminal of a comparator, while the positive terminal is connected to VMR. If the input is negative, the output is +2.5V, otherwise it is -2.5V. The IPmodule utilizes the CAB's op-amp in comparator mode.

Phase Behavior:

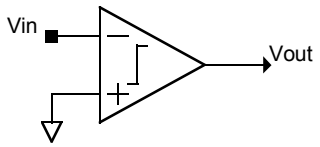
Input sampled on: $\phi 1$ and $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

To be precise, the C01b component uses a conventional analog comparator. It is not a switched capacitor circuit, so the output continuously reflects the input signal.

Programmable Parameters:

none

Circuit Diagram and Controlling Equations:



$$V_{out} = \begin{array}{ll} +2.5V & for \quad V_{in} < 0 \\ -2.5V & for \quad V_{in} > 0 \end{array}$$

C02 – Dual Input Comparator

This IPmodule is a full cycle comparator. It has two inputs which are compared with each other. If the positive input is greater than the negative input the output is +2.5V, otherwise it is -2.5V. The IPmodule utilizes the CAB's op-amp in comparator mode.

Phase Behavior:

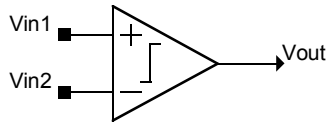
Input sampled on: $\phi 1$ and $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

To be precise, the C02 component uses a conventional analog comparator. It is not a switched capacitor circuit, so the output continuously reflects the input signal.

Programmable Parameters:

none

Circuit Diagram and Controlling Equations:



$$V_{out} = \begin{array}{ll} +2.5V & for \quad V_{in1} > V_{in2} \\ -2.5V & for \quad V_{in1} < V_{in2} \end{array}$$

C03 – Schmitt Trigger

This IPmodule is a Schmitt Trigger (a single input comparator with programmable hysteresis).

Phase Behavior:

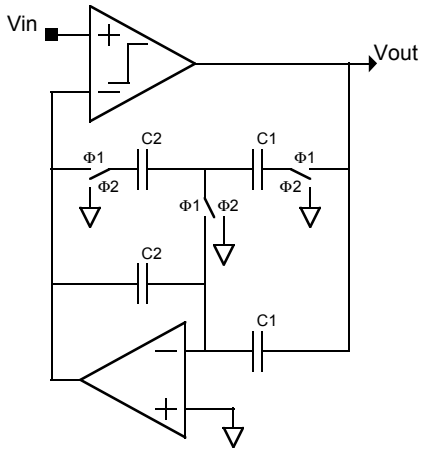
Input sampled on: $\phi 1$ and $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

The trigger voltage is a function of both the Vsch parameter and the current state of the output. If the output is high (+2.5V), it will flip to low only when the input drops below VMR-Vsch. If the output is low (-2.5V), it will flip to high only when the input rises above VMR+Vsch.

Programmable Parameters:

Vsch, Trigger Voltage	0.02 - 2.5 V (default 0.1 V)

Circuit Diagram and Controlling Equations:



$$V_{sch} = \frac{2.5C_1}{C_2}$$

C04b – Fast Inverting Comparator

This IPmodule is a full cycle inverting comparator. It has one input which is connected to the negative terminal of a comparator, while the positive terminal is connected to VMR. If the input is negative, the output is +2.5V, otherwise it is -2.5V. The IPmodule utilizes the CAB's DPS comparator rather than using the opamp in comparator mode. The C04b is faster than the C01b, but has less drive (fan-out).

Phase Behavior:

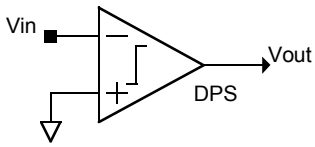
Input sampled on: ϕ1 and ϕ2
Output valid on: ϕ1 and ϕ2

The C04b IPmodule is a conventional, continuous time analog comparator. It is not a switched capacitor circuit, so the output is not synchronous with a sample clock but, rather, continuously reflects the input signal.

Programmable Parameters:

none

Circuit Diagram and Controlling Equations:



$$V_{out} = \begin{cases} +2.5V \ for \ V_{in} < 0 \\ -2.5V \ for \ V_{in} > 0 \end{cases}$$

D01 – Inverting Differentiator

This IPmodule is a full cycle inverting differentiator. The only adjustable parameter is the Differentiation Constant, K. The units of K are μs. Vout is proportional to the slope of Vin. the larger the value of K, the greater Vout will be per slope of Vin.

Phase Behavior:

Input sampled on: $\phi 1$ and $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

The output signal will be slewing to the correct voltage during each phase. It most accurately represents the differentiation function at the end of $\phi 1$ and $\phi 2$.

Programmable Parameters:

Differentiation Constant, K .002/f_c - 25.3 μs (at f_c = 250 kHz)*
(default, 1 μs)

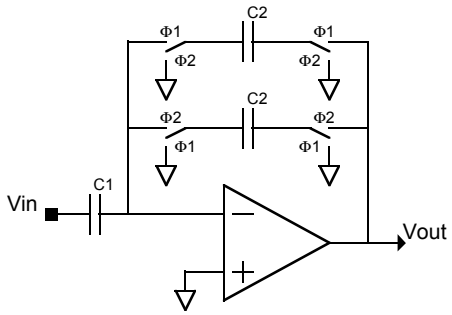
* The maximum K is subject to clock frequency limitations as explained below.

K's limits are a function of the frequency of the IPmodule's sample clock, f_c (expressed in kHz).

Circuit Diagram and Controlling Equations:

The transfer function of this circuit expressed as a difference equation is:

$$V_{out} = K\Delta V_{in}$$



$$K = \frac{C_1}{2C_2 f_c}$$

Limitations on the Maximum Integration Constant (K):

This IPmodule has a clock dependent maximum differentiation constant. The maximum differentiation constant can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a differentiation constant that is higher than the displayed maximum differentiation constant. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum differentiation constant is exceeded, the actual differentiation constant of this IPmodule may not equal the displayed realized value and simulated value, and the actual differentiation constant may not be equal to the actual differentiation constant on another identically programmed array. To avoid these problems, program the differentiation constant between the displayed limits.

D02p1 – Inverting Differentiator with Phase 1 Hold

This IPmodule is a full cycle inverting differentiator. The output slews during ϕ2, and is valid at the end of ϕ2 and throughout ϕ1.

Phase Behavior:

Input sampled on: ϕ2
Output valid on: ϕ1 and ϕ2

The output signal will be slewing to the correct voltage during ϕ2. It most accurately represents the differentiation function at the end of ϕ2 and throughout ϕ1. The output voltage established at the end of ϕ2 is held throughout the following ϕ1.

The only adjustable parameter is the Differentiation Constant, K. The units of K are μs. Vout is proportional to the slope of Vin. The larger the value of K, the greater Vout will be per slope of Vin.

K's limits are a function of the frequency of the IPmodule's sample clock, f_c (expressed in kHz).

Programmable Parameters:

Differentiation Constant, K	.002/f_c - 25.3 μs (at f_c = 250 kHz)* (default, 1 μs)

* The maximum K is subject to clock frequency limitations as explained below.

K's limits are a function of the frequency of the IPmodule's sample clock, f_c (expressed in kHz).

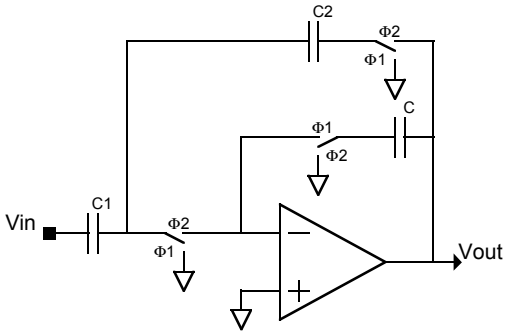
Circuit Diagram and Controlling Equations:

The transfer function of this circuit expressed as a difference equation is:

$$V_{out} = K\Delta V_{in}$$

Where Vout during ϕ1 represents the result of differentiation during the previous ϕ2.

$$K = \frac{C_1}{2C_2 f_c}$$



Limitations on the Maximum Integration Constant (K):

This IPmodule has a clock dependent maximum differentiation constant. The maximum differentiation constant can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a differentiation constant that is higher than the displayed maximum differentiation constant. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum differentiation constant is exceeded, the actual differentiation constant of this IPmodule may not equal the displayed realized value and simulated value, and the actual differentiation constant may not be equal to the actual differentiation constant on another identically programmed array. To avoid these problems, program the differentiation constant between the displayed limits.

D02p2 – Inverting Differentiator with Phase 2 Hold

This IPmodule is a full cycle inverting differentiator. The output slews during ϕ1, and is valid at the end of ϕ1 and throughout ϕ2.

Phase Behavior:

Input sampled on: ϕ1
Output valid on: ϕ1 and ϕ2

The output signal will be slewing to the correct voltage during ϕ1. It most accurately represents the differentiation function at the end of ϕ1 and throughout ϕ2. The output voltage established at the end of ϕ1 is held throughout the following ϕ2.

The only adjustable parameter is the Differentiation Constant, K. The units of K are μs. Vout is proportional to the slope Vin. The larger the value of K, the greater Vout will be per slope of Vin.

Programmable Parameters:

Differentiation Constant, K .002/f_c - 25.3 μs (at f_c = 250 kHz)*
(default, 1 μs)

* The maximum K is subject to clock frequency limitations as explained below.

K's limits are a function of the frequency of the IPmodule's sample clock, f_c (expressed in kHz).

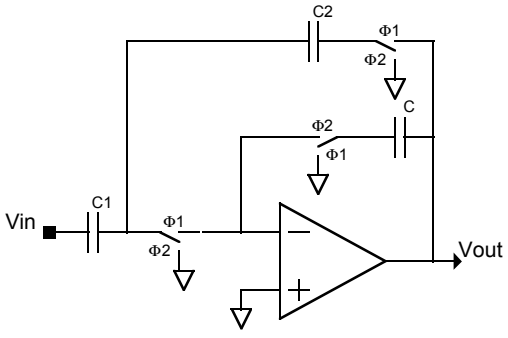
Circuit Diagram and Controlling Equations:

The transfer function of this circuit expressed as a difference equation is:

$$V_{out} = K\Delta V_{in}$$

Where Vout during ϕ2 represents the result of differentiation during the previous ϕ1.

$$K = \frac{C_1}{2C_2 f_c}$$



Limitations on the Maximum Integration Constant (K):

This IPmodule has a clock dependent maximum differentiation constant. The maximum differentiation constant can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a differentiation constant that is higher than the displayed maximum differentiation constant. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum differentiation constant is exceeded, the actual differentiation constant of this IPmodule may not equal the displayed realized value and simulated value, and the actual differentiation constant may not be equal to the actual differentiation constant on another identically programmed array. To avoid these problems, program the differentiation constant between the displayed limits.

F01 – Low Pass Biquad Filter (low Q)

This IPmodule is a full cycle low pass filter based on a biquadratic transfer function. It is designed for low Q (pole quality factor) values.

Phase Behavior:

Input sampled on: $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Corner Frequency	0.10 – 25 kHz (default 5 kHz)
G -- Pass Band Gain	0.01 – 20.0 V/V (default 1.0 V/V)
Q -- Pole Quality Factor	0.1 – 1.5 (default 0.707)

The corner frequency f_o, is the frequency at which the filter's gain is equal to GQ [$^{V}/_{V}$].

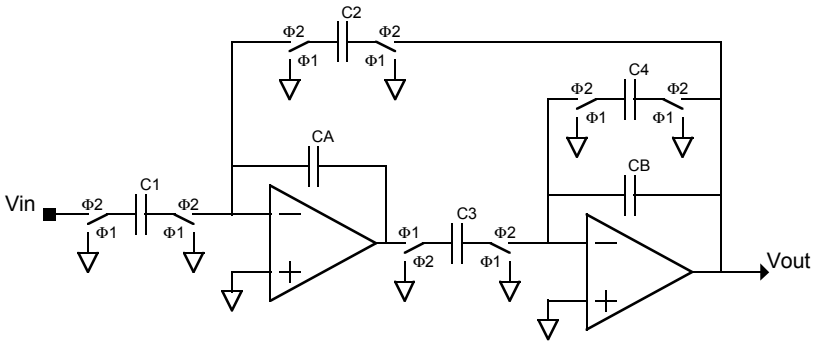
The corner frequency range of 0.10 – 25 kHz assumes the default clock frequency of 250 kHz. If you divide down the input clock to this IPmodule, then corner frequencies are divided down by the same factor.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{4\pi^2 f_0^2 G}{s^2 + \frac{2\pi f_0}{Q} s + 4\pi^2 f_0^2}$$

where G is the pass-band gain (DC gain), f_o is the corner frequency, and Q is the quality factor. The circuit realizing this IPmodule is shown in the following figure:



The capacitor values will be chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{2\pi}\sqrt{\frac{C_2}{C_A}\frac{C_3}{C_B}} \qquad G = \frac{C_1}{C_2} \qquad Q = \frac{C_B}{C_4}\sqrt{\frac{C_2}{C_A}\frac{C_3}{C_B}}$$

Example Usage:

This IPmodule cell may be utilized in realization of higher order filters with different approximation methods. For example, in order to realize a low pass filter with 0.3dB ripple, 10kHz pass frequency edge, 50kHz stop frequency edge, and 60dB attenuation using Chebyshev approximation, the following cells are used:

Low Pass Biquad	Low Q = 0.668	f_o = 6.535 kHz	G = 0.983
Low Pass Biquad	High Q = 2.628	f_o = 10.652 kHz	G = 0.983

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

F02 – Low Pass Biquad Filter (high Q)

This IPmodule is a full cycle low pass filter based on a biquadratic transfer function. It is designed for high Q (pole quality factor) values.

Phase Behavior:

Input sampled on: $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Corner Frequency	0.10 – 25 kHz (default 5 kHz)
Pass Band Gain	0.01 – 20.0 V/V (default 1.0 V/V)
Q -- Pole Quality Factor	1.0 – 100 (default 1.0)

The corner frequency f_o, is the frequency at which the filter's gain is equal to GQ [$^{V}/_{V}$].

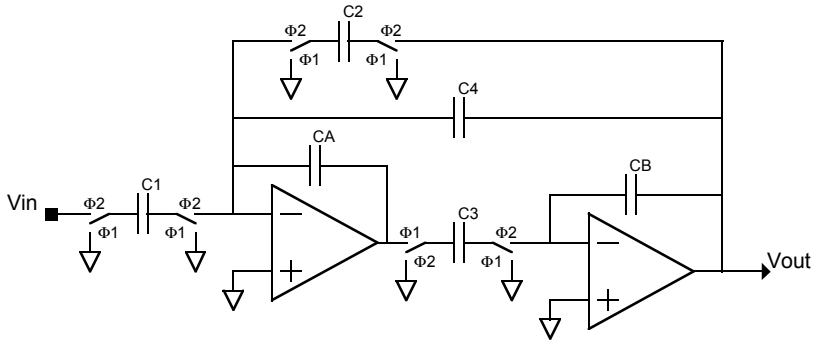
The corner frequency range of 0.10 – 25 kHz assumes the default clock frequency of 250 kHz. If you divide down the input clock to this IPmodule, then corner frequencies are divided down by the same factor.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{4\pi^2 f_0^2 G}{s^2 + \frac{2\pi f_0}{Q} s + 4\pi^2 f_0^2}$$

where G is the pass-band gain (DC gain), f_o is the corner frequency, and Q is the quality factor. The circuit realizing this IPmodule is shown in the following figure:



The capacitor values will be chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{2\pi}\sqrt{\frac{C_2}{C_A}\frac{C_3}{C_B}} \qquad G = \frac{C_1}{C_2} \qquad Q = \frac{C_B}{C_4}\sqrt{\frac{C_A C_B C_2}{C_3}}$$

Example Usage:

This IPmodule cell may be utilized in realization of higher order filters with different approximation methods. For example, in order to realize a low pass filter with 0.3dB ripple, 10kHz pass frequency edge, 50kHz stop frequency edge, and 60dB attenuation using Chebyshev approximation, the following cells are used:

Low Pass Biquad	Low Q = 0.668	f_o = 6.535 kHz	G = 0.983
Low Pass Biquad	High Q = 2.628	f_o = 10.652 kHz	G = 0.983

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

F03 – High Pass Biquad Filter (low Q)

This IPmodule is a full cycle high pass filter based on a biquadratic transfer function. It is designed for low Q (pole quality factor) values.

Phase Behavior:

Input sampled on: ϕ1 and ϕ2
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

Corner Frequency	0.11 – 25 kHz (default 5 kHz)
Pass Band Gain	0.01 – 20.0 V/V (default 1.0 V/V)
Q -- Pole Quality Factor	0.1 – 1.5 (default 0.707)

The corner frequency f_o, is the frequency at which the filter's gain is equal to GQ [$^{V}/_{V}$].

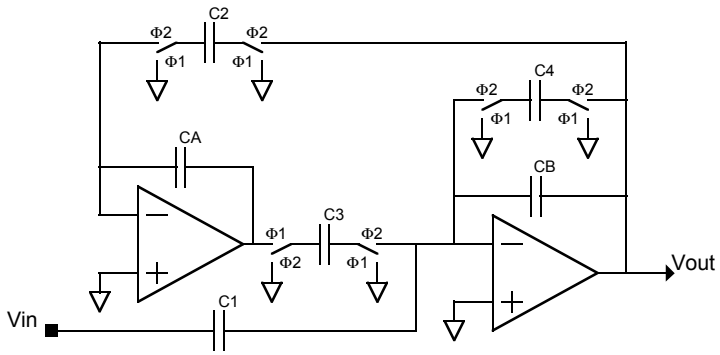
The corner frequency range of 0.11 – 25 kHz assumes the default clock frequency of 250 kHz. If you divide down the input clock to this IPmodule, then corner frequencies are divided down by the same factor.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{Gs^2}{s^2 + \frac{2\pi f_0}{Q}s + 4\pi^2 f_0}$$

where G is the pass-band gain (DC gain), f_o is the corner frequency, and Q is the quality factor. The circuit realizing



this IPmodule is shown in the following figure:

The capacitor values will be chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{2\pi}\sqrt{\frac{C_2}{C_A}\frac{C_3}{C_B}} \qquad G = \frac{C_1}{C_B} \qquad Q = \frac{C_B}{C_4}\sqrt{\frac{C_2 C_3}{C_A C_B}}$$

Example Usage:

This IPmodule cell may be utilized in realization of higher order filters with different approximation methods. For example, in order to realize a high pass filter with 0.3dB ripple, 10kHz stop frequency edge, 50kHz pass frequency edge, and 60dB attenuation using Chebyshev approximation, the following cells are used:

High Pass Biquad	Low Q = 0.668	f_o = 77.17 kHz	G = 0.983
High Pass Biquad	High Q = 2.628	f_o = 47.35 kHz	G = 0.983

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

Limitations due to Gain Bandwidth:

The high frequency gain of this IPmodule is subject to the gain bandwidth constraints of the amplifier. Using this IPmodule with higher frequency signals may result in actual gains that do not equal the displayed realized value and will not be consistent from part to part. Filter corner frequency or pass band gain measurements may be complicated by this effect. This will most likey be noticeable when a higher gain is requested.

F04 – High Pass Biquad Filter (high Q)

This IPmodule is a full cycle high pass filter based on a biquadratic transfer function. It is designed for high Q (pole quality factor) values.

Phase Behavior:

Input sampled on: ϕ1 and ϕ2
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

Corner Frequency	0.10 – 25 kHz (default 5 kHz)
Pass Band Gain	0.01 – 20.0 V/V (default 1.0 V/V)
Q -- Pole Quality Factor	1.0 – 100.0 (default 1.0)

The corner frequency f_o, is the frequency at which the filter's gain is equal to GQ [$^{V}/_{V}$].

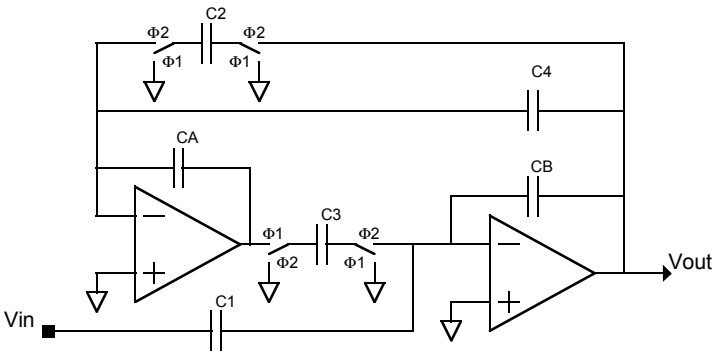
The corner frequency range of 0.10 – 25 kHz assumes the default clock frequency of 250 kHz. If you divide down the input clock to this IPmodule, then corner frequencies are divided down by the same factor.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{Gs^2}{s^2 + \frac{2\pi f_0}{Q}s + 4\pi^2 f_0}$$

where G is the pass-band gain (high frequency gain), f_o is the corner frequency, and Q is the quality factor. The circuit realizing this IPmodule is shown in the following figure:



The capacitor values will be chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{2\pi}\sqrt{\frac{C_2}{C_A}\frac{C_3}{C_B}} \qquad G = \frac{C_1}{C_B} \qquad Q = \frac{1}{C_4}\sqrt{\frac{C_A C_B C_2}{C_3}}$$

Example Usage:

This IPmodule cell may be utilized in realization of higher order filters with different approximation methods. For example, in order to realize a high pass filter with 0.3dB ripple, 10kHz stop frequency edge, 50kHz pass frequency edge, and 60dB attenuation using Chebyshev approximation, the following cells are used:

High Pass Biquad	Low Q = 0.668	f_o = 77.17 kHz	G = 0.983
High Pass Biquad	High Q = 2.628	f_o = 47.35 kHz	G = 0.983

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

Limitations due to Gain Bandwidth:

The high frequency gain of this IPmodule is subject to the gain bandwidth constraints of the amplifier. Using this IPmodule with higher frequency signals may result in actual gains that do not equal the displayed realized value and will not be consistent from part to part. Filter corner frequency or pass band gain measurements may be complicated by this effect. This will most likey be noticeable when a higher gain is requested.

F05 – Band Pass Biquad Filter (low Q)

This IPmodule is a full cycle band pass filter based on a biquadratic transfer function. It is designed for low Q (pole quality factor) values.

Phase Behavior:

Input sampled on: $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Center Frequency	0.11 – 25 kHz (default 5 kHz)
Pass Band Gain	0.01 – 20.0 V/V (default 1.0 V/V)
Q -- Pole Quality Factor	0.1 – 1.5 (default 0.707)

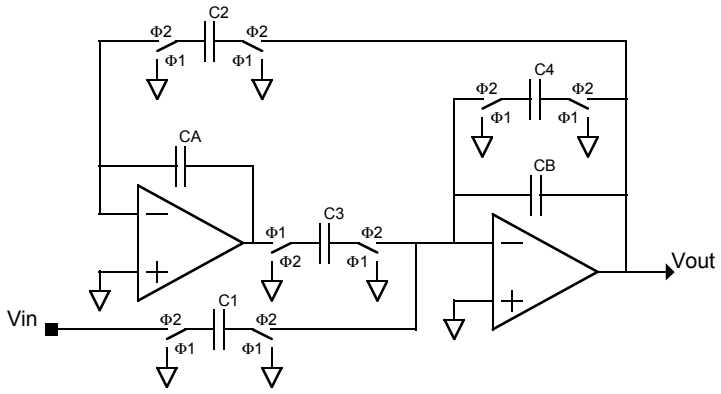
The center frequency range of 0.11 – 25 kHz assumes the default clock frequency of 250 kHz. If you divide down the input clock to this IPmodule, then center frequencies are divided down by the same factor.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{2\pi f_0 \frac{G}{Q} s}{s^2 + \frac{2\pi f_0}{Q} s + 4\pi^2 f_0^2}$$

where G is the pass-band gain (center frequency gain), f_o is the center frequency, and Q is the quality factor. The circuit realizing this IPmodule is shown in the following figure:



The capacitor values will be chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{2\pi}\sqrt{\frac{C_2}{C_A}\frac{C_3}{C_B}} \qquad G = \frac{C_1}{C_4} \qquad Q = \frac{C_B}{C_4}\sqrt{\frac{C_2 C_3}{C_A C_B}}$$

The bandwidth for this filter given as:

$$3\text{-dB bandwidth} = \frac{\omega_0}{Q} = f_c \frac{C_4}{C_B}$$

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

F06 – Band Pass Biquad Filter (high Q)

This IPmodule is a full cycle band pass filter based on a biquadratic transfer function. It is designed for high Q (pole quality factor) values.

Phase Behavior:

Input sampled on: $\phi 1$ and $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Center Frequency	0.1 - 25 kHz (default 5 kHz)
Pass Band Gain	0.01 – 20.0 V/V (default 1.0 V/V)
Q -- Pole Quality Factor	1.0 – 100.0 (default 1.0)

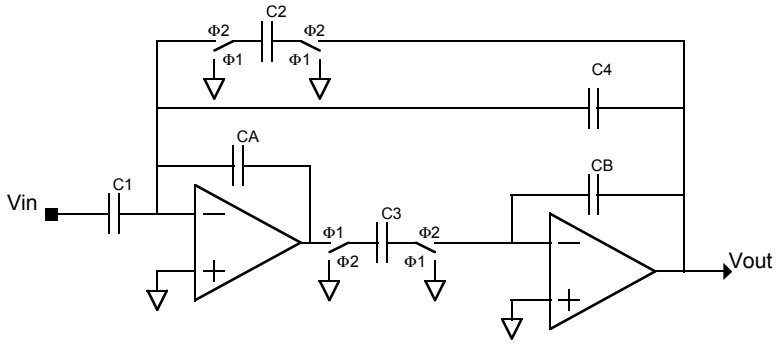
The center frequency range of 0.1 - 25 kHz assumes the default clock frequency of 250 kHz. If you divide down the input clock to this IPmodule, then center frequencies are divided down by the same factor.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{2\pi f_0 \frac{G}{Q} s}{s^2 + \frac{2\pi f_0}{Q} s + 4\pi^2 f_0^2}$$

where G is the pass-band gain (center frequency gain), f_o is the center frequency, and Q is the quality factor. The circuit realizing this IPmodule is shown in the following figure:



The capacitor values will be chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{2\pi}\sqrt{\frac{C_2}{C_A}\frac{C_3}{C_B}} \qquad G = \frac{C_1}{C_4} \qquad Q = \frac{1}{C_4}\sqrt{\frac{C_A C_B C_2}{C_3}}$$

The -3dB bandwidth for this filter given as:

$$\frac{\omega_0}{Q} = f_c \frac{C_3 C_4}{C_A C_B}$$

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

F07 – Band Stop Biquad Filter (low Q)

This IPmodule is a full cycle band pass filter based on a biquadratic transfer function. It is designed for low Q (pole quality factor) values.

Phase Behavior:

Input sampled on: $\phi 1$ and $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Center Frequency	0.11 – 25 kHz (default 5 kHz)
GainLO low frequency (DC) gain, G_L	0.01 – 20.0 V/V (default 1.0 V/V)
GainHI high frequency gain, G_H	0.01 – 20.0 V/V (default 1.0 V/V)
Q -- Pole Quality Factor	0.1 – 1.5 (default 0.707)

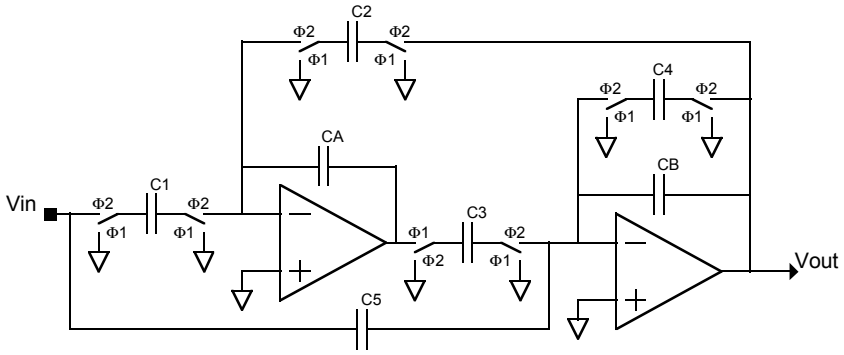
The center frequency range of 0.11 – 25 kHz assumes the default clock frequency of 250 kHz. If you divide down the input clock to this IPmodule, then center frequencies are divided down by the same factor. Setting GainLO equal to GainHI assures that the Center Frequency notch will be where specified. Setting GainLO and GainHI to unequal values will shift the notch off the specified frequency.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{G_H s^2 + 4\pi^2 f_0^2 G_L}{s^2 + \frac{2\pi f_0}{Q} s + 4\pi^2 f_0^2}$$

where G_L is the low frequency pass-band gain, G_H is the high frequency pass-band gain, f_o is the center frequency,



and Q is the quality factor. The circuit realizing this IPmodule is shown in the following figure:

The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{2\pi}\sqrt{\frac{C_2}{C_A}\frac{C_3}{C_B}} \qquad G_L = \frac{C_1}{C_2} \qquad G_H = \frac{C_5}{C_B} \qquad Q = \frac{C_B}{C_4}\sqrt{\frac{C_2 C_3}{C_A C_B}}$$

The notch frequency for this filter is given as:

$$\text{Notch frequency } = 2\pi f_0 \sqrt{\frac{G_L}{G_H}} = 2\pi f_0 \sqrt{\frac{C_1 C_B}{C_2 C_5}}$$

Example Usage:

This IPmodule cell may be utilized in realization of higher order filters with different approximation methods. For example, in order to realize a band pass filter with 0.1dB ripple, 1kHz and 20kHz pass frequency edges, 2kHz and 10kHz stop frequency edges, and 40dB attenuation using elliptic approximation, the following cells are used:

Band Stop Biquad	Low Q = 0.96	f_o = 7.48 kHz	G_L = 10.34	G_H = 0.25
Band Stop Biquad	Low Q = 0.96	f_o = 2.68 kHz	G_L = 0.006	G_H = 0.25
Band Stop Biquad	High Q = 3.44	f_o = 10.9 kHz	G_L = 0.962	G_H = 0.25
Band Stop Biquad	High Q = 3.44	f_o = 1.84 kHz	G_L = 0.065	G_H = 0.25

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

Limitations due to Gain Bandwidth:

The high frequency gain of this IPmodule is subject to the gain bandwidth constraints of the amplifier. Using this IPmodule with higher frequency signals may result in actual gains that do not equal the displayed realized value and will not be consistent from part to part. Filter corner frequency or pass band gain measurements may be complicated by this effect. This will most likey be noticeable when a higher gain is requested.

F08 – Band Stop Biquad Filter (high Q)

This IPmodule is a full cycle band pass filter based on a biquadratic transfer function. It is designed for high Q (pole quality factor) values.

Phase Behavior:

Input sampled on: ϕ1 and ϕ2
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

Center Frequency	0.1 – 25 kHz (default 5 kHz)
GainLO low frequency (DC) gain, G_L	0.01 – 20.0 V/V (default 1.0 V/V)
GainHI high frequency gain, G_H	0.01 – 20.0 V/V (default 1.0 V/V)
Q -- Pole Quality Factor	1.0 - 100 (default 1.0)

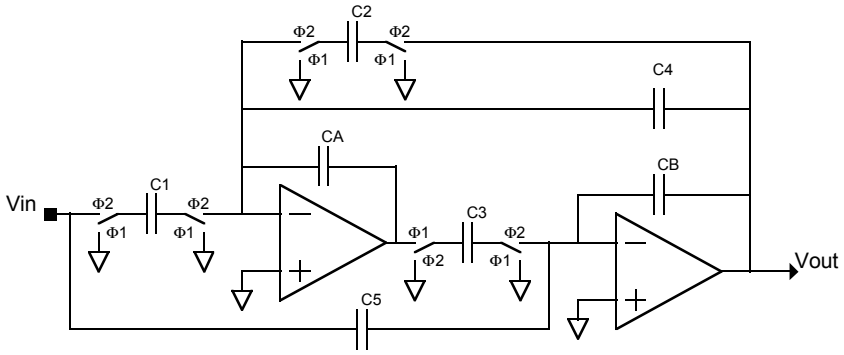
The center frequency range of 0.10 – 25 kHz assumes the default clock frequency of 250 kHz. If you divide down the input clock to this IPmodule, then corner frequencies are divided down by the same factor. Setting GainLO equal to GainHI assures that the Center Frequency notch will be where specified. Setting GainLO and GainHI to unequal values will shift the notch off the specified frequency.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{G_H s^2 + 4\pi^2 f_0^2 G_L}{s^2 + \frac{2\pi f_0}{Q} s + 4\pi^2 f_0^2}$$

where G_L is the low frequency pass-band gain, G_H is the high frequency pass-band gain, f_o is the center frequency,



and Q is the quality factor. The circuit realizing this IPmodule is shown in the following figure:

The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{2\pi}\sqrt{\frac{C_2}{C_A}\frac{C_3}{C_B}} \qquad G_L = \frac{C_1}{C_2} \qquad G_H = \frac{C_5}{C_B} \qquad Q = \frac{1}{C_4}\sqrt{\frac{C_A C_B C_2}{C_3}}$$

The notch frequency for this filter is given as:

$$\text{Notch frequency } = 2\pi f_0 \sqrt{\frac{G_L}{G_H}} = 2\pi f_0 \sqrt{\frac{C_1 C_B}{C_2 C_5}}$$

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

Limitations due to Gain Bandwidth:

The high frequency gain of this IPmodule is subject to the gain bandwidth constraints of the amplifier. Using this IPmodule with higher frequency signals may result in actual gains that do not equal the displayed realized value and will not be consistent from part to part. Filter corner frequency or pass band gain measurements may be complicated by this effect. This will most likey be noticeable when a higher gain is requested.

F09 – Low Pass Single Pole Filter

This IPmodule is a full cycle low pass single pole filter.

Phase Behavior:

Input sampled on: $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Corner Frequency	0.17 – 12.5 kHz (default 5 kHz)
Pass Band Gain	0.01 – 20.0 V/V (default 1.0 V/V)

The corner frequency f_o is the frequency at which the gain is $-3+20LogG$ dB, where G is the pass band gain.

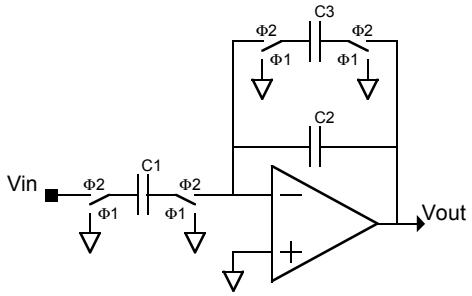
The corner frequency range of 0.17 – 12.5 kHz assumes the default clock frequency of 250 kHz. If you divide down the input clock to this IPmodule, then center frequencies are divided down by the same factor.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{2\pi f_0 G}{s + 2\pi f_0}$$

where G is the pass-band gain and f_o is the corner frequency. The circuit realizing this IPmodule is shown in the following figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{\pi}\frac{C_3}{(2C_2 + C_3)} \qquad G = \frac{C_1}{C_3}$$

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

F10 – High Pass Single Pole Filter

This IPmodule is a full cycle high pass single pole filter.

Phase Behavior:

Input sampled on: ϕ1 and ϕ2
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

Corner Frequency	0.17 – 12.5 kHz (default 5 kHz)
Pass Band Gain	0.01 – 20.0 V/V (default 1.0 V/V)

The corner frequency f_o is the frequency at which the gain is $-3+20LogG$ dB, where G is the pass band gain.

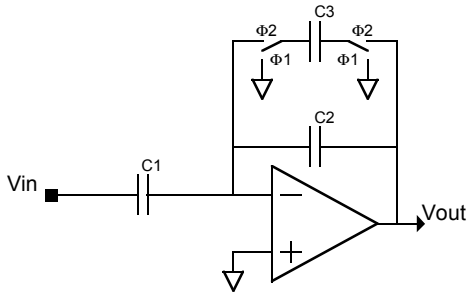
The corner frequency range of 0.17 – 12.5 kHz assumes the default clock frequency of 250 kHz. If you divide down the input clock to this IPmodule, then center frequencies are divided down by the same factor.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{Gs}{s+2\pi f_0}$$

where G is the pass-band gain and f_o is the corner frequency. The circuit realizing this IPmodule is shown in the following figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{\pi}\frac{C_3}{(2C_2+C_3)} \qquad G = \frac{2C_1}{(2C_2+C_3)}$$

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

Limitations due to Gain Bandwidth:

The high frequency gain of this IPmodule is subject to the gain bandwidth constraints of the amplifier. Using this IPmodule with higher frequency signals may result in actual gains that do not equal the displayed realized value and will not be consistent from part to part. Filter corner frequency or pass band gain measurements may be complicated by this effect. This will most likey be noticeable when a higher gain is requested.

G01 – Inverting Gain Stage

This IPmodule is a full cycle (output is valid in both phases of the clock) inverting gain stage. The input voltage is scaled by the value of the specified gain, G. The sign of the output voltage is opposite to the sign of the input voltage.

Phase Behavior:

Input sampled on: ϕ1 and ϕ2
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

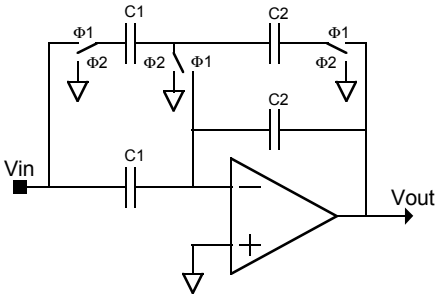
Voltage Gain	0.01 – 100.0 V/V (default 1.0 V/V)

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2} = -G$$

where C_1 and C_2 are the input and feedback capacitors respectively as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relation:

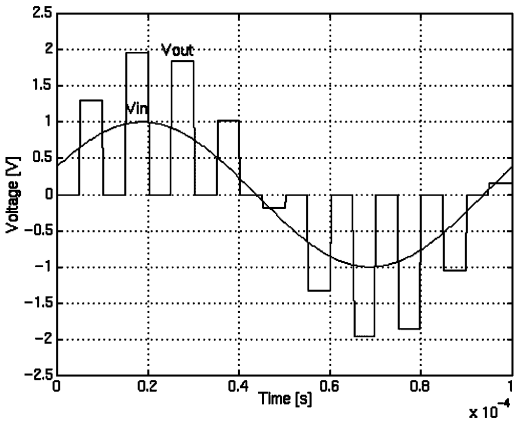
$$G = \frac{C_1}{C_2}$$

Limitations due to Gain Bandwidth:

The high frequency gain of this IPmodule is subject to the gain bandwidth constraints of the amplifier. Using this IPmodule with higher frequency signals may result in actual gains that do not equal the displayed realized value and will not be consistent from part to part. This will most likey be noticeable when a higher gain is requested.

G03a – Half Cycle Gain Stage (with offset compensation)

This IPmodule is a half cycle non-inverting gain stage. The input voltage is scaled by the value of the specified gain, G. The sign of the output voltage is the same as the sign of the input voltage (non-inverting gain stage). An example of input and output signals for gain, G=2.



Phase Behavior:

Input sampled on: ϕ1
Output valid on: ϕ2

Programmable Parameters:

Voltage Gain	0.01 – 12.7 V/V (at f_c = 250 kHz)* (default 1.0 V/V)

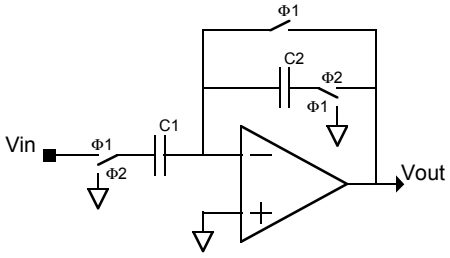
* The maximum G is subject to clock frequency limitations as explained below.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit in phase 2 is:

$$\frac{V_{out}}{V_{in}} = \frac{C_1}{C_2} = G$$

where C_1 and C_2 are the input and feedback capacitors respectively as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relation:

$$G = \frac{C_1}{C_2}$$

Example Usage:

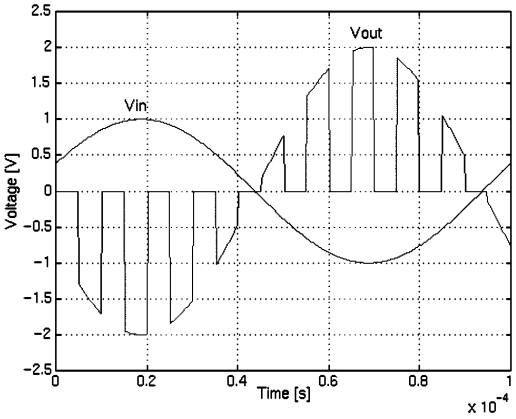
The advantage of this circuit over the gain stage G01 is that the output of this circuit is offset compensated. This module will also have less 1/f noise then the G01. In order to produce output valid in both phases, the output of this circuit should be conditioned with the sample-and-hold circuit S01p2.

Limitations on the Maximum Gain (G):

This IPmodule has a clock dependent maximum gain. The maximum gain can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a gain that is higher than the displayed maximum gain. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum gain is exceeded, the actual gain of this IPmodule may not equal the displayed realized value and simulated value, and the actual gain may not be equal to the actual gain on another identically programmed array. To avoid these problems, program the gain between the displayed limits.

G03b – Half Cycle Inverting Gain Stage (with offset compensation)

This IPmodule is a half cycle inverting gain stage. The input voltage is scaled by the value of the specified gain, G. The sign of the output voltage is opposite to the sign of the input voltage (inverting gain stage). An example of input and output signals for gain, Gain = 2 is shown in the following figure:



Phase Behavior:

Input sampled on: $\phi 2$
Output valid on: $\phi 2$

Programmable Parameters:

Voltage Gain	0.01 – 12.7 V/V (at f_c = 250 kHz)* (default 1.0 V/V)

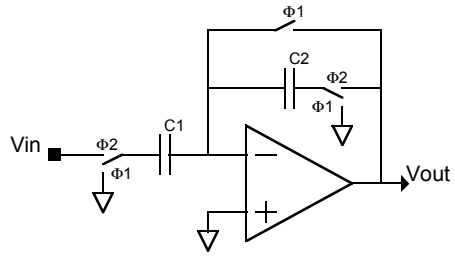
* The maximum G is subject to clock frequency limitations as explained below.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit in phase 2 is

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2} = -G$$

where C_1 and C_2 are the input and feedback capacitors respectively as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relation:

$$G = \frac{C_1}{C_2}$$

Example Usage:

The advantage of this circuit over the gain stage G01 is that the output of this circuit is offset compensated. In order to produce output valid in both phases, the output of this circuit should be conditioned with the sample-and-hold circuit S01p2.

Limitations on the Maximum Gain (G):

This IPmodule has a clock dependent maximum gain. The maximum gain can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a gain that is higher than the displayed maximum gain. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum gain is exceeded, the actual gain of this IPmodule may not equal the displayed realized value and simulated value, and the actual gain may not be equal to the actual gain on another identically programmed array. To avoid these problems, program the gain between the displayed limits.

G04 – Inverting Gain Stage (with offset compensation in one phase)

This IPmodule is a full cycle (output is valid in both clock phases) inverting gain stage. The input voltage is scaled by the value of the specified gain, G. The sign of the output voltage is opposite to the sign of the input voltage. In phase 2 the op-amp's offset is compensated.

Phase Behavior:

Input sampled on: $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$
(compensated $\phi 2$)

Programmable Parameters:

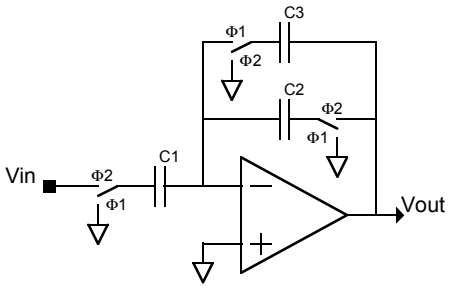
Voltage Gain	0.01 – 100.0 V/V (default 1.0 V/V)

Circuit Diagram and Controlling Equations:

The transfer function of this circuit in phase 2 is:

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2} = -G$$

where C_1 and C_2 are the input and feedback capacitors respectively as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relation:

$$G = \frac{C_1}{C_2}$$

Example Usage:

The advantage of this circuit over the gain stage G01 is that the output of this circuit is offset compensated during phase 2.

G05 – Inverting Sum Amplifier

This IPmodule is a full cycle (output is valid in both phases) inverting sum amplifier. It has two inputs. Both input voltages are scaled by the values of the specified gains, Gain1 and Gain2.

Phase Behavior:

Inputs sampled on: $\phi 1$ and $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

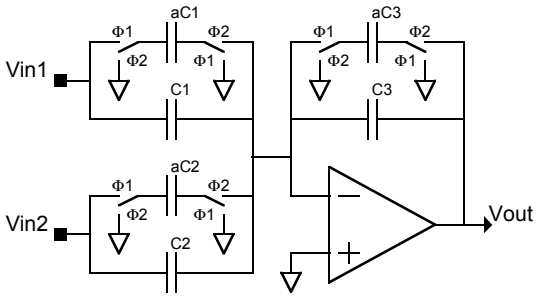
Gain1	0.067 – 15.0 V/V (default 1.0 V/V)
Gain2	0.067 – 15.0 V/V (default 1.0 V/V)

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$V_{out} = -\frac{C_1}{C_3}V_{in1} - \frac{C_2}{C_3}V_{in2}$$
$$= -G_1V_{in1} - G_2V_{in2}$$

where C_1 and C_2 are the input capacitors, and C_3 is the feedback capacitor as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relation:

$$G_1 = \frac{C_1}{C_3} \qquad G_2 = \frac{C_2}{C_3}$$

Limitations due to Gain Bandwidth:

The high frequency gain of this IPmodule is subject to the gain bandwidth constraints of the amplifier. Using this IPmodule with higher frequency signals may result in actual gains that do not equal the displayed realized value and will not be consistent from part to part. This will most likey be noticeable when a higher gain is requested.

G06a – Half Cycle Summing Amplifier (with offset compensation)

This IPmodule is a half cycle non-inverting summing amplifier. It has two inputs. Both input voltages are scaled by the values of the specified gains, Gain1 and Gain2.

Phase Behavior:

Inputs sampled on: IN1: ϕ1
IN2: ϕ2
Output valid on: ϕ2

Programmable Parameters:

Voltage Gain1	0.067 – 12.7 V/V (at f_c = 250 kHz)* (default 1.0 V/V)
Voltage Gain2	0.067 – 12.7 V/V (at f_c = 250 kHz)* (default 1.0 V/V)

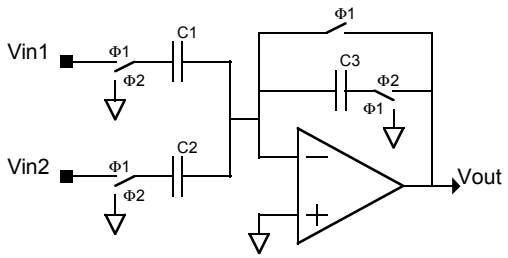
* The Gains are subject to clock frequency limitations as explained below.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$V_{out} = \frac{C_1}{C_3}V_{in1} + \frac{C_2}{C_3}V_{in2}$$
$$= G_1V_{in1} + G_2V_{in2}$$

where C_1 and C_2 are the input capacitors, and C_3 is the feedback capacitor as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relation:

$$G_1 = \frac{C_1}{C_3} \qquad G_2 = \frac{C_2}{C_3}$$

Example Usage:

One advantage of this circuit over the gain stage G05 is that the output of this circuit is offset compensated. In order to produce output valid in both phases, the output of this circuit should be conditioned with the sample-and-hold circuit S01p2

Limitations on the Maximum Gain (G1, G2):

This IPmodule has clock dependent maximum gains. The maximum gain can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a gain that is higher than the displayed maximum gain. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum gain is exceeded, the actual gain of this IPmodule may not equal the displayed realized value and simulated value, and the actual gain may not be equal to the actual gain on another identically programmed array. To avoid these problems, program the gain between the displayed limits.

G06ab – Half Cycle Subtracting Amplifier (with offset compensation)

This IPmodule is a half cycle non-inverting subtracting amplifier. It has two inputs. Both input voltages are scaled by the values of the specified gains, Gain1 and Gain2.

Phase Behavior:

Inputs sampled on: IN1: ϕ1
IN2: ϕ2
Output valid on: ϕ2

Programmable Parameters:

Voltage Gain1	0.067 – 12.7 V/V (at f_c = 250 kHz)* (default 1.0 V/V)
Voltage Gain2	0.067 – 12.7 V/V (at f_c = 250 kHz)* (default 1.0 V/V)

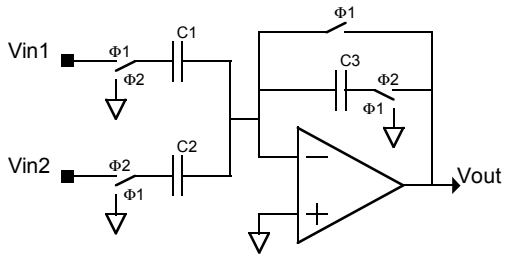
* The Gains are subject to clock frequency limitations as explained below.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$V_{out} = \frac{C_1}{C_3}V_{in1} - \frac{C_2}{C_3}V_{in2}$$
$$= G_1 V_{in1} + G_2 V_{in2}$$

where C_1 and C_2 are the input capacitors, and C_3 is the feedback capacitor as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relation:

$$G_1 = \frac{C_1}{C_3} \qquad G_2 = -\frac{C_2}{C_3}$$

Example Usage:

One advantage of this circuit over the gain stage G05 is that the output of this circuit is offset compensated. In order to produce output valid in both phases, the output of this circuit should be conditioned with the sample-and-hold circuit S01p2

Limitations on the Maximum Gain (G1, G2):

This IPmodule has clock dependent maximum gains. The maximum gain can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a gain that is higher than the displayed maximum gain. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum gain is exceeded, the actual gain of this IPmodule may not equal the displayed realized value and simulated value, and the actual gain may not be equal to the actual gain on another identically programmed array. To avoid these problems, program the gain between the displayed limits.

G06b – Half Cycle Subtracting Amplifier (with offset compensation)

This IPmodule is a half cycle non-inverting subtracting amplifier. It has two inputs. Both input voltages are scaled by the values of the specified gains, Gain1 and Gain2.

Phase Behavior:

Inputs sampled on: IN1: ϕ1
IN2: ϕ2
Output valid on: ϕ2

Programmable Parameters:

Voltage Gain1 0.067 – 12.7 V/V (at f_c = 250 kHz)*
(default 1.0 V/V)
Voltage Gain2 0.067 – 12.7 V/V (at f_c = 250 kHz)*
(default 1.0 V/V)

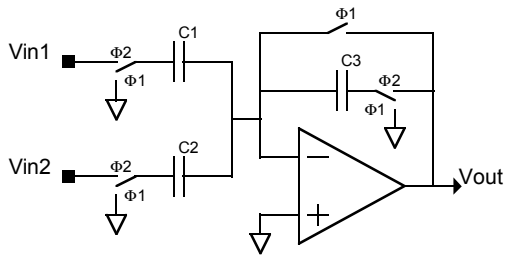
* The Gains are subject to clock frequency limitations as explained below.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$V_{out} = -\frac{C_1}{C_3}V_{in1} - \frac{C_2}{C_3}V_{in2}$$
$$= -G_1V_{in1} - G_2V_{in2}$$

where C_1 and C_2 are the input capacitors, and C_3 is the feedback capacitor as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relation:

$$G_1 = \frac{C_1}{C_3} \qquad G_2 = \frac{C_2}{C_3}$$

Example Usage:

One advantage of this circuit over the gain stage G05 is that the output of this circuit is offset compensated. In order to produce output valid in both phases, the output of this circuit should be conditioned with the sample-and-hold circuit S01p2

Limitations on the Maximum Gain (G1, G2):

This IPmodule has clock dependent maximum gains. The maximum gain can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a gain that is higher than the displayed maximum gain. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum gain is exceeded, the actual gain of this IPmodule may not equal the displayed realized value and simulated value, and the actual gain may not be equal to the actual gain on another identically programmed array. To avoid these problems, program the gain between the displayed limits.

I01a – Integrator

This IPmodule is a full cycle integrator. The single adjustable parameter is the Integration Constant, K. During every $\phi 2$ sample clock period, Vin is sampled. The Vin sample is scaled by K, to produce a change in output voltage, ΔVout. The higher the value of K, the greater the change in output voltage.

The units of K are 10^6/s.

K's limits are a function of the frequency of the IPmodule's sample clock, f_c.

Phase Behavior:

Input sampled on: $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Integration Constant, K $f_c/10^8$ - 3.16 (at f_c = 250 kHz)*
(default 0.25 [10^6/s])

* The maximum K is subject to clock frequency limitations as explained below.

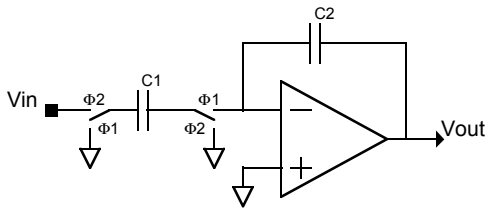
Circuit Diagram and Controlling Equations:

The transfer function of this as expressed by a difference equation is:

$$\Delta V_{out} = KV_{in}$$

The transfer function expressed in the s domain is:

$$\frac{V_{out}(s)}{V_{in}(s)} = H(s) = \frac{f_c C_1}{sC_2}$$



Example:

Assume the following conditions:
Vin = 0.3 VDC
fc = 1MHz
K = 10^{-2} 10^6/S

Vout would be an increasing ramp voltage with a slope (a ΔVout) of:
0.3x10^{-2} 10^6V/s or 3 kV/S or 0.3 V/mS.

In actual practice of course, continuously integrating a DC input voltage would soon result in a railed output. To generate an actual ramp wave form, the input waveform would be a square wave, fed into a integrator with reset, such as an I02a.

Limitations on the Maximum Integration Constant (K):

This IPmodule has a clock dependent maximum integration constant. The maximum integration constant can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with an integration constant that is higher than the displayed maximum integration constant. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum integration constant is exceeded, the actual integration constant of this IPmodule may not equal the displayed realized value and simulated value, and the actual integration constant may not be equal to the actual integration constant on another identically programmed array. To avoid these problems, program the integration constant between the displayed limits.

I01b – Inverting Integrator

This IPmodule is a full cycle inverting integrator. The single adjustable parameter is the Integration Constant, K. During every $\phi 2$ sample clock period, Vin is sampled. The Vin sample is scaled by K, to produce a change in output voltage, ΔVout. The higher the value of K, the greater the change in output voltage.

The units of K are 10^6/s.

K's limits are a function of the frequency of the IPmodule's sample clock, f_c.

Phase Behavior:

Input sampled on: $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Integration Constant, K $f_c/10^8$ - 3.16 (at f_c = 250 kHz)*
(default 0.25 [10^6/s])

* The maximum K is subject to clock frequency limitations as explained below.

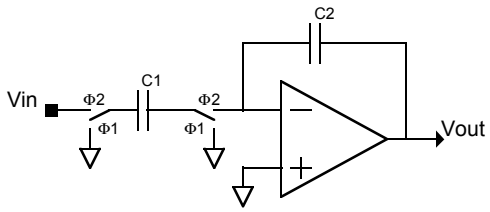
Circuit Diagram and Controlling Equations:

The transfer function of this as expressed by a difference equation is:

$$\Delta V_{out} = -KV_{in}$$

The transfer function expressed in the s domain is:

$$\frac{V_{out}(s)}{V_{in}(s)} = H(s) = -\frac{f_c C_1}{sC_2}$$



Example:

Assume the following conditions:
Vin = 0.3 VDC
fc = 1MHz
K = 10^{-2} 10^6/S

Vout would be a decreasing ramp voltage with a slope (a ΔVout) of:
-0.3x10^{-2} 10^6V/s or -3 kV/S or -0.3 V/mS.

In actual practice of course, continuously integrating a DC input voltage would soon result in a railed output. To generate an actual ramp wave form, the input waveform would be a square wave, fed into a integrator with reset, such as an I02a.

Limitations on the Maximum Integration Constant (K):

This IPmodule has a clock dependent maximum integration constant. The maximum integration constant can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with an integration constant that is higher than the displayed maximum integration constant. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum integration constant is exceeded, the actual integration constant of this IPmodule may not equal the displayed realized value and simulated value, and the actual integration constant may not be equal to the actual integration constant on another identically programmed array. To avoid these problems, program the integration constant between the displayed limits.

I02a – Integrator with Reset

This IPmodule is a full cycle integrator with a reset. When the input voltage is positive (greater than VMR) the circuit performs integration and when the input is negative (less than VMR) the integrating capacitor is discharged (in one cycle).

The single adjustable parameter is the Integration Constant, K. During every $\phi 2$ sample clock period, Vin is sampled. The Vin sample is scaled by K, to produce a change in output voltage, ΔVout. The higher the value of K, the greater the change in output voltage.

The units of K are 10^6/s.

K's limits are a function of the frequency of the IPmodule's sample clock, f_c.

Phase Behavior:

Input sampled on: $\phi 2$, if Vin > VMR
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Integration Constant, K $f_c/10^8$ - 3.16 (at f_c = 250 kHz)*
(default 0.25 [10^6/s])

* The maximum K is subject to clock frequency limitations as explained below.

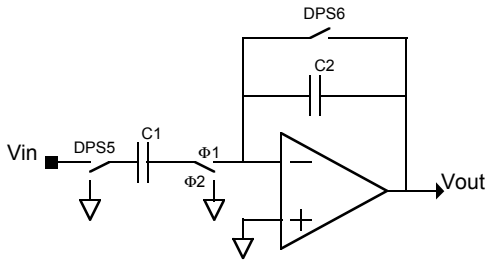
Circuit Diagram and Controlling Equations:

The transfer function of this as expressed by a difference equation is:

$$while\ V_{in} > VMR, \Delta V_{out} = KV_{in}$$
$$while\ V_{in} < VMR, V_{out} = VMR$$

The transfer function (when Vin > VMR) expressed in the s domain is:

$$\frac{V_{out}(s)}{V_{in}(s)} = H(s) = \frac{f_c C_1}{sC_2}$$



Example:

Assume the following conditions:
Vin = Square wave symmetric about VMR with Vpp = ± 0.3 VDC
fc = 1MHz
K = 10^{-2} 10^6/S

When Vin > VMR, Vout would be an increasing ramp voltage with a slope (a ΔVout) of:
0.3x10^{-2} 10^6V/s or 3 kV/S or 0.3 V/mS. When Vin < VMR, Vout =VMR.

Limitations on the Maximum Integration Constant (K):

This IPmodule has a clock dependent maximum integration constant. The maximum integration constant can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with an integration constant that is higher than the displayed maximum integration constant. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum integration constant is exceeded, the actual integration constant of this IPmodule may not equal the displayed realized value and simulated value, and the actual integration constant may not be equal to the actual integration constant on another identically programmed array. To avoid these problems, program the integration constant between the displayed limits.

I02b – Inverting Integrator with Reset

This IPmodule is a full cycle inverting integrator with a reset. When the input voltage is positive (greater than VMR) the circuit performs integration and when the input is negative (less than VMR) the integrating capacitor is discharged (in one cycle).

The single adjustable parameter is the Integration Constant, K. During every $\phi 2$ sample clock period, Vin is sampled. The Vin sample is scaled by K, to produce a change in output voltage, ΔVout. The higher the value of K, the greater the change in output voltage.

The units of K are 10^6/s.

K's limits are a function of the frequency of the IPmodule's sample clock, f_c.

Phase Behavior:

Input sampled on: $\phi 2$, if Vin > VMR
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Integration Constant, K $f_c/10^8$ - 3.16 (at f_c = 250 kHz)*
(default 0.25 [10^6/s])

* The maximum K is subject to clock frequency limitations as explained below.

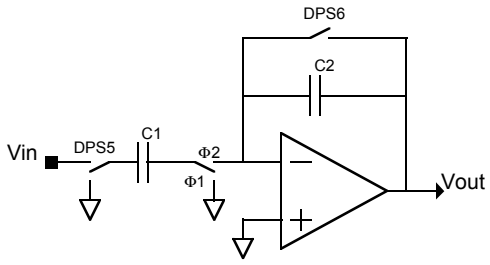
Circuit Diagram and Controlling Equations:

The transfer function of this as expressed by a difference equation is:

$$while\ V_{in} > VMR, \Delta V_{out} = -KV_{in}$$
$$while\ V_{in} < VMR, V_{out} = VMR$$

The transfer function (when Vin > VMR) expressed in the s domain is:

$$\frac{V_{out}(s)}{V_{in}(s)} = H(s) = -\frac{f_c C_1}{sC_2}$$



Example:

Assume the following conditions:
Vin = Square wave symmetric about VMR with Vpp = ± 0.3 VDC
fc = 1MHz
K = 10^{-2} 10^6/S

When Vin > VMR, Vout would be a decreasing ramp voltage with a slope (a ΔVout) of:
-0.3x10^{-2} 10^6V/s or -3 kV/S or -0.3 V/mS. When Vin < VMR, Vout =VMR.

Limitations on the Maximum Integration Constant (K):

This IPmodule has a clock dependent maximum integration constant. The maximum integration constant can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with an integration constant that is higher than the displayed maximum integration constant. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum integration constant is exceeded, the actual integration constant of this IPmodule may not equal the displayed realized value and simulated value, and the actual integration constant may not be equal to the actual integration constant on another identically programmed array. To avoid these problems, program the integration constant between the displayed limits.

I02c – Negative Integrator with Reset

This IPmodule is a full cycle negative integrator with a reset. When the input voltage is negative (less than VMR) the circuit performs integration and when the input is positive (greater than VMR) the integrating capacitor is discharged (in one cycle).

The single adjustable parameter is the Integration Constant, K. During every $\phi 2$ sample clock period, Vin is sampled. The Vin sample is scaled by K, to produce a change in output voltage, ΔVout. The higher the value of K, the greater the change in output voltage.

The units of K are 10^6/s.

K's limits are a function of the frequency of the IPmodule's sample clock, f_c.

Phase Behavior:

Input sampled on: $\phi 2$, if Vin < VMR
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Integration Constant, K $f_c/10^8$ - 3.16 (at f_c = 250 kHz)*
(default 0.25 [10^6/s])

* The maximum K is subject to clock frequency limitations as explained below.

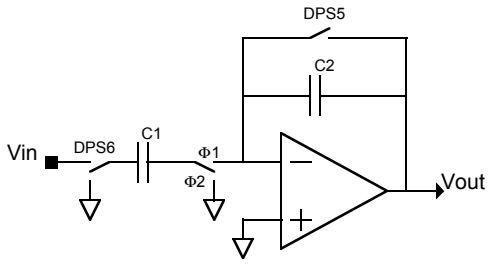
Circuit Diagram and Controlling Equations:

The transfer function of this as expressed by a difference equation is:

$$while\ V_{in} < VMR, \Delta V_{out} = KV_{in}$$
$$while\ V_{in} > VMR, V_{out} = VMR$$

The transfer function (when Vin < VMR) expressed in the s domain is:

$$\frac{V_{out}(s)}{V_{in}(s)} = H(s) = \frac{f_c C_1}{sC_2}$$



Example:

Assume the following conditions:
Vin = Square wave symmetric about VMR with Vpp = ± 0.3 VDC
fc = 1MHz
K = 10^{-2} 10^6/S

When Vin < VMR, Vout would be a decreasing ramp voltage with a slope (a ΔVout) of:
-0.3x10^{-2} 10^6V/s or -3 kV/S or -0.3 V/mS. When Vin > VMR, Vout =VMR.

Limitations on the Maximum Integration Constant (K):

This IPmodule has a clock dependent maximum integration constant. The maximum integration constant can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with an integration constant that is higher than the displayed maximum integration constant. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum integration constant is exceeded, the actual integration constant of this IPmodule may not equal the displayed realized value and simulated value, and the actual integration constant may not be equal to the actual integration constant on another identically programmed array. To avoid these problems, program the integration constant between the displayed limits.

I02d – Negative Inverting Integrator with Reset

This IPmodule is a full cycle negative inverting integrator with a reset. When the input voltage is negative (less than VMR) the circuit performs integration and when the input is positive (greater than VMR) the integrating capacitor is discharged (in one cycle).

The single adjustable parameter is the Integration Constant, K. During every $\phi 2$ sample clock period, Vin is sampled. The Vin sample is scaled by K, to produce a change in output voltage, ΔVout. The higher the value of K, the greater the change in output voltage.

The units of K are 10^6/s.

K's limits are a function of the frequency of the IPmodule's sample clock, f_c.

Phase Behavior:

Input sampled on: $\phi 2$, if Vin < VMR
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Integration Constant, K $f_c/10^8$ - 3.16 (at f_c = 250 kHz)*
(default 0.25 [10^6/s])

* The maximum K is subject to clock frequency limitations as explained below.

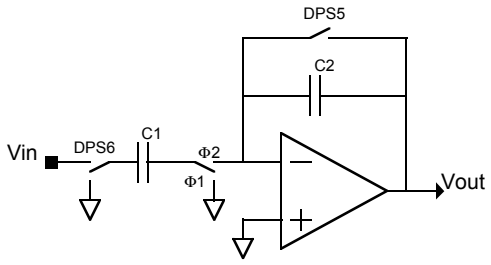
Circuit Diagram and Controlling Equations:

The transfer function of this as expressed by a difference equation is:

$$while\ V_{in} < VMR, \Delta V_{out} = -KV_{in}$$
$$while\ V_{in} > VMR, V_{out} = VMR$$

The transfer function (when Vin < VMR) expressed in the s domain is:

$$\frac{V_{out}(s)}{V_{in}(s)} = H(s) = -\frac{f_c C_1}{sC_2}$$



Example:

Assume the following conditions:
Vin = Square wave symmetric about VMR with Vpp = ± 0.3 VDC
fc = 1MHz
K = 10^{-2} 10^6/S

When Vin < VMR, Vout would be an increasing ramp voltage with a slope (a ΔVout) of:
0.3x10^{-2} 10^6V/s or 3 kV/S or 0.3 V/mS. When Vin > VMR, Vout =VMR.

Limitations on the Maximum Integration Constant (K):

This IPmodule has a clock dependent maximum integration constant. The maximum integration constant can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with an integration constant that is higher than the displayed maximum integration constant. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum integration constant is exceeded, the actual integration constant of this IPmodule may not equal the displayed realized value and simulated value, and the actual integration constant may not be equal to the actual integration constant on another identically programmed array. To avoid these problems, program the integration constant between the displayed limits.

M01 – Limiter

This IPmodule is a full cycle limiter. The output voltage will be limited (clamped) to the voltage specified by the Vlimit parameter.

Phase Behavior:

Input sampled on: ϕ1 and ϕ2
Output valid on: ϕ1 and ϕ2

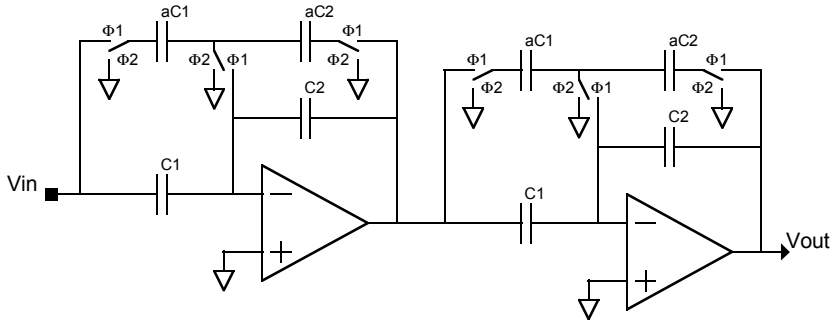
Programmable Parameters:

Vlimit, V_L	0.1 – 2.5 Vpk (default 1.0)
Gain, G	0.01 – 5.0 V/V (default 1 V/V)

Circuit Diagram and Controlling Equations:

$$\frac{2.5G}{V_L} = \frac{C_1}{C_2}$$

$$\frac{V_L}{2.5} = \frac{C'_1}{C'_2}$$



Limitations due to Gain Bandwidth:

The high frequency gain of this IPmodule is subject to the gain bandwidth constraints of the amplifier. Using this IPmodule with higher frequency signals may result in actual gains that do not equal the displayed realized value and will not be consistent from part to part. This will most likely be noticeable when a higher gain is requested.

M04 – Wire

This IPmodule is a simple wire, i.e. the input of the cell is shorted to the output. It may be useful in cases where there are not enough resources to make a connection or for probe calibration purposes (to take into account all the chip/pin connections). There are no user adjustable parameters in this IPmodule.

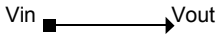
Phase Behavior:

Input sampled on: ϕ1 and ϕ2
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

none

Circuit Diagram and Controlling Equations:



O01 – Sine Wave Oscillator

This IPmodule generates a sinusoid, centered around the mid-rail 0V reference at the chosen amplitude and frequency. Based on a low-Q biquad filter structure, the biquad oscillates at its own resonant frequency.

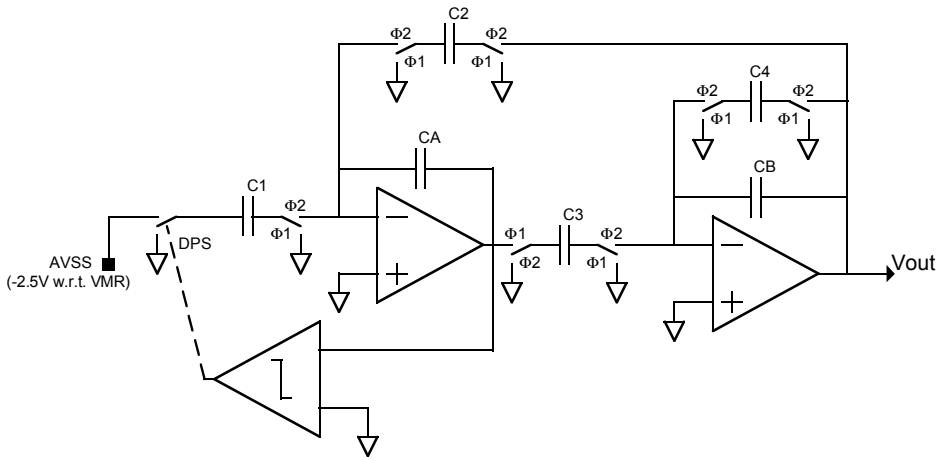
Phase Behavior:

Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Oscillator Frequency	3.73 – 50 kHz (default 6 kHz)
Amplitude (to peak)	0.4 – 2.5V

The oscillator frequency range of 3.73 – 50 kHz assumes the default clock frequency of 250 kHz. This range will scale with changes to the clock frequency setting.



Circuit Diagram and Controlling Equations:

DPS (Dynamic Phase Swap) is a level-dependent switch clock phase controller
The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_{osc} = \frac{C_2}{C_A} ? \frac{f_c}{2\pi} = \frac{C_3}{C_B} ? \frac{f_c}{2\pi}$$

$$V_{pk} = \frac{300}{\pi} ? \frac{C_1}{C_2}$$

A Note on Oscillator Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual oscillator performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher amplitude is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the amplitude or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

Rectifier Selector Guide

With the remarkable flexibility of the programmable analog array, there are many types of rectifiers to offer. This selector guide introduces you to the various rectifiers you can choose from.

Full Wave vs. Half Wave

This is probably the most familiar of the rectifier parameters. A full wave rectifier presents the rectified version of the entire input waveform to the output. A half wave rectifier, will only present either the portion of the input waveform which is above VMR or the portion which is below VMR to the output.

Integrated Filter

The flexibility of the CABs allows the inclusion of a low pass filter in the rectifier for no additional cost in CAB real estate.

Inverting vs. Non-Inverting

An inverting rectifier presents all rectified portions of the input waveform with a negative gain. Conversely, the non-inverting rectifiers present all rectified portions of the input waveform with a positive gain.

Positive vs. Negative

For half wave rectifiers, the CAB needs to know which "half" of the input waveform to rectify. Positive rectifiers will rectify only that portion of the input waveform that is above VMR. Negative rectifiers will rectify the portion of the input waveform that is below VMR.

Input Sample Phase

This specifies which phase of the sample clock that the input is sampled on. If fed by a continuous time signal, then this parameter is of little concern. If on the other hand, the input to the rectifier happens to come from another IPmodule in which the output is not continuously valid, then care must be taken to ensure that the input sample phase of the rectifier selected matches the output valid phase of the driving signal.

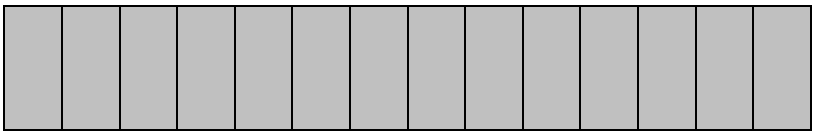
Output Valid Phase

Not all of the rectifiers are constructed with outputs that are always valid. This parameter shows which phases of the sample clock the rectifier outputs are valid on.

Available Rectifiers

	R0 1a	R0 1b	R0 2a	R0 2b	R0 2c	R0 2d	R0 3a	R0 3b	R0 4a	R0 4b	R0 4c	R0 4d	R0 5b	R0 5d
Low Pass Filter	•	•	•	•	•	•								
Full Wave	•	•					•	•						
Half Wave			•	•	•	•			•	•	•	•	•	•
Inverting		•		•		•		•		•		•	•	•
Non-Inverting	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Positive Sample														
Negative Sample														
Input Sampled on ϕ1														
Input Sampled on ϕ2														
Output														

Valid in ϕ1□•□•□•□•□•□□□□□□□•□•□□Output Valid in ϕ2



R01a – Full Wave Rectifier with Low Pass Filter

This IPmodule is a full wave rectifier with positive output voltage. The rectified waveform is passed through a single pole low pass filter. The default parameter values disable this feature by moving the corner frequency to the highest possible value.

Phase Behavior:

Input sampled on: ϕ1, if Vin < VMR
ϕ2, if Vin > VMR
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

Corner Frequency 0.25 - 50.0 kHz
(default 50.0 kHz)

Pass Band Gain 0.1 – 10.0 V/V
(default 1.0 V/V)

The corner frequency f_o is the frequency at which the gain is $-3+20LogG$ dB, where G is the pass band gain.

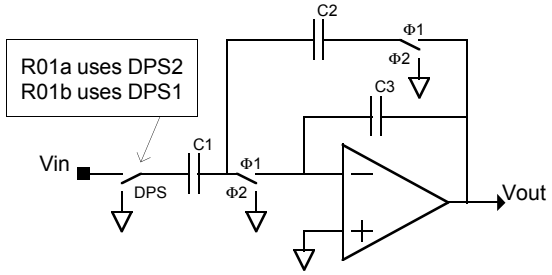
The corner frequency range of 0.25 – 50.0 kHz assumes the default clock frequency of 250 kHz. If you change the input clock to this IPmodule, then center frequencies are changed by the same factor.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit (working as rectifier) is:

$$V_{out} = |V_{in}| \frac{C_1}{C_2} = |V_{in}| G$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



DPS2 is a Dynamic Phase Swapper and is not under direct user control.

The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{\pi} \frac{C_2}{(2C_3 + C_2)} \qquad G = \frac{C_1}{C_2}$$

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

R01b – Inverting Full Wave Rectifier with Low Pass Filter

This IPmodule is a full wave rectifier with negative output voltage. The rectified waveform is passed through a single pole low pass filter. The default parameter values disable this feature by moving the corner frequency to the highest possible value.

Phase Behavior:

Input sampled on: ϕ1, if Vin > VMR
ϕ2, if Vin < VMR
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

Corner Frequency 0.25 - 50.0 kHz
(default 50.0 kHz)

Pass Band Gain 0.1 – 10.0 V/V
(default 1.0 V/V)

The corner frequency f_o is the frequency at which the gain is $-3+20LogG$ dB, where G is the pass band gain.

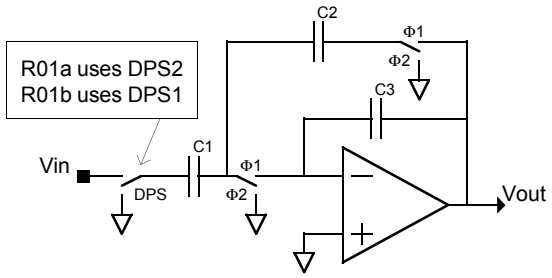
The corner frequency range of 0.25 – 50.0 kHz assumes the default clock frequency of 250 kHz. If you change the input clock to this IPmodule, then center frequencies are changed by the same factor.

Circuit Diagram and Controlling Equations:

The transfer function of this circuit (working as rectifier) is:

$$V_{out} = -|V_{in}|\frac{C_1}{C_2} = -|V_{in}|G$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



DPS1 is a Dynamic Phase Swapper and is not under direct user control.

The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{\pi}\frac{C_2}{(2C_3 + C_2)} \qquad G = \frac{C_1}{C_2}$$

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

R02a – Half Wave Rectifier with Low Pass Filter

This IPmodule is a half wave rectifier with positive output voltage. The rectified waveform is passed through a single pole low pass filter. The default parameter values disable this feature by moving the corner frequency to the highest possible value. Any portion of the input waveform above VMR is rectified to a positive signal. Any portion of the input waveform below VMR is simply clamped to VMR.

Phase Behavior:

Input sampled on: $\phi 2$, if Vin > VMR
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Corner Frequency	0.25 - 50.0 kHz (default 50.0 kHz)
Pass Band Gain	0.1 – 10.0 V/V (default 1.0 V/V)

The corner frequency f_o is the frequency at which the gain is $-3+20LogG$ dB, where G is the pass band gain.

The corner frequency range of 0.25 – 50.0 kHz assumes the default clock frequency of 250 kHz. If you change the input clock to this IPmodule, then center frequencies are changed by the same factor.

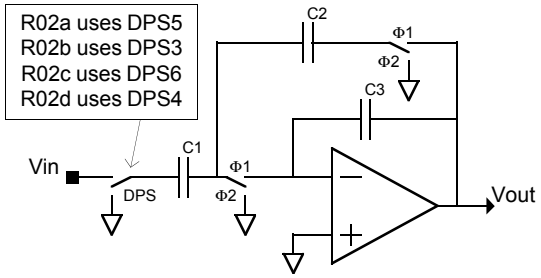
Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$if\ V_{in} > VMR, V_{out} = V_{in}\frac{C_1}{C_2} = V_{in}G$$

$$if\ V_{in} < VMR, V_{out} = VMR$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{\pi}\frac{C_2}{(2C_3 + C_2)} \qquad G = \frac{C_1}{C_2}$$

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

R02b – Inverting Half Wave Rectifier with Low Pass Filter

This IPmodule is an inverting half wave rectifier with negative output voltage. The rectified waveform is passed through a single pole low pass filter. The default parameter values disable this feature by moving the corner frequency to the highest possible value. Any portion of the input waveform above VMR is rectified to a negative signal. Any portion of the input waveform below VMR is simply clamped to VMR.

Phase Behavior:

Input sampled on: ϕ1, if Vin > VMR
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

Corner Frequency	0.25 - 50.0 kHz (default 50.0 kHz)
Pass Band Gain	0.1 – 10.0 V/V (default 1.0 V/V)

The corner frequency f_o is the frequency at which the gain is $-3+20LogG$ dB, where G is the pass band gain.

The corner frequency range of 0.25 – 50.0 kHz assumes the default clock frequency of 250 kHz. If you change the input clock to this IPmodule, then center frequencies are changed by the same factor.

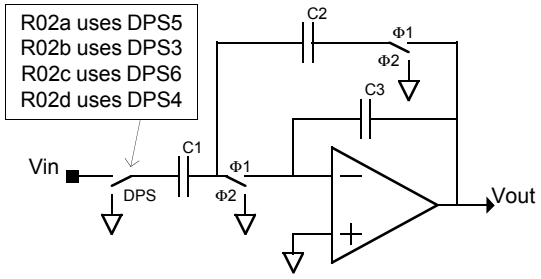
Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$if\ V_{in} > VMR, V_{out} = -V_{in}\frac{C_1}{C_2} = -V_{in}G$$

$$if\ V_{in} < VMR, V_{out} = VMR$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{\pi}\frac{C_2}{(2C_3 + C_2)} \qquad G = \frac{C_1}{C_2}$$

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

R02c – Negative Half Wave Rectifier with Low Pass Filter

This IPmodule is a negative half wave rectifier with negative output voltage. The rectified waveform is passed through a single pole low pass filter. The default parameter values disable this feature by moving the corner frequency to the highest possible value. Any portion of the input waveform below VMR is rectified to a negative signal. Any portion of the input waveform above VMR is simply clamped to VMR.

Phase Behavior:

Input sampled on: $\phi 2$, if Vin < VMR
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

Corner Frequency	0.25 – 50.0 kHz (default 50.0 kHz)
Pass Band Gain	0.1 – 10.0 V/V (default 1.0 V/V)

The corner frequency f_o is the frequency at which the gain is $-3+20LogG$ dB, where G is the pass band gain.

The corner frequency range of 0.25 – 50.0 kHz assumes the default clock frequency of 250 kHz. If you change the input clock to this IPmodule, then center frequencies are changed by the same factor.

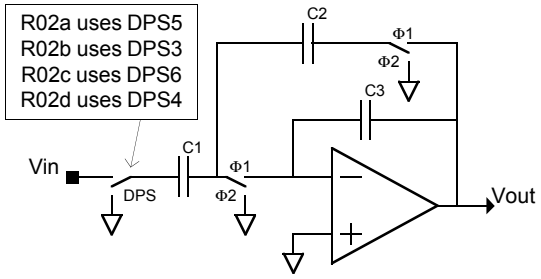
Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$if\ V_{in} < VMR, V_{out} = V_{in}\frac{C_1}{C_2} = V_{in}G$$

$$if\ V_{in} > VMR, V_{out} = VMR$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{\pi}\frac{C_2}{(2C_3 + C_2)} \qquad G = \frac{C_1}{C_2}$$

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

R02d – Inverting Negative Half Wave Rectifier with Low Pass Filter

This IPmodule is an inverting negative half wave rectifier with positive output voltage. The rectified waveform is passed through a single pole low pass filter. The default parameter values disable this feature by moving the corner frequency to the highest possible value. Any portion of the input waveform below VMR is rectified to a positive signal. Any portion of the input waveform above VMR is simply clamped to VMR.

Phase Behavior:

Input sampled on: ϕ1, if Vin < VMR
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

Corner Frequency	0.25 – 50.0 kHz (default 50.0 kHz)
Pass Band Gain	0.1 – 10.0 V/V (default 1.0 V/V)

The corner frequency f_o is the frequency at which the gain is $-3+20LogG$ dB, where G is the pass band gain.

The corner frequency range of 0.25 – 50.0 kHz assumes the default clock frequency of 250 kHz. If you change the input clock to this IPmodule, then center frequencies are changed by the same factor.

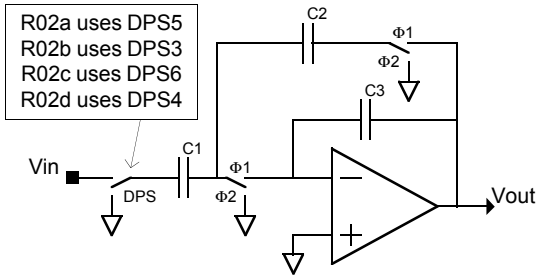
Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$if\ V_{in} < VMR, V_{out} = -V_{in}\frac{C_1}{C_2} = -V_{in}G$$

$$if\ V_{in} > VMR, V_{out} = VMR$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$f_0 = \frac{f_c}{\pi}\frac{C_2}{(2C_3 + C_2)} \qquad G = \frac{C_1}{C_2}$$

(1) A Note on IPmodule Parameter Limits:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. While most parameters will be implemented with values very close to those requested, it is possible to request combinations of parameters that cannot be realized. This will most likely occur when you request parameter values that are at or near the extreme ends of their allowable ranges. When this occurs, the realized values may differ significantly from the desired values, and will have a note attached that refers you to this help. In these cases, it is usually possible to obtain acceptable values by either changing the clock frequency and/or making tradeoffs among the parameter values. It is often possible, for example, to change the gain parameter to something nearer the middle of the range, and make up the difference in a following IPmodule. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

(2) A Note on Filter Performance:

The programmable parameters for this IPmodule are interrelated, and are also functions of the sample clock. Due to gain bandwidth limitations of the amplifier, some combinations of parameters will result in actual filter performance that does not match the displayed realized values and simulated performance, and the actual performance may not match the actual performance on another identically programmed array. When this problem is likely, the realized values will have a note attached that refers you to this help. This will most often occur when a higher gain is requested and is more likely at higher clock frequencies. Although all parameters are involved, it is usually easiest to reduce the gain or clock frequency to find acceptable values. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path.

R03a – Half Cycle Full Wave Rectifier

This IPmodule is a half cycle full wave rectifier with positive output voltage. The entire input waveform is rectified to a positive signal. The output is valid on $\phi 2$ and clamped to VMR during $\phi 1$.

Phase Behavior:

Input sampled on: $\phi 2$, if Vin < VMR
$\phi 1$, if Vin > VMR
Output valid on: $\phi 2$ (compensated)

Programmable Parameters:

Pass Band Gain 0.01 – 12.7 V/V (at f_c = 250 kHz)*
(default 1.0 V/V)

* The maximum G is subject to clock frequency limitations as explained below.

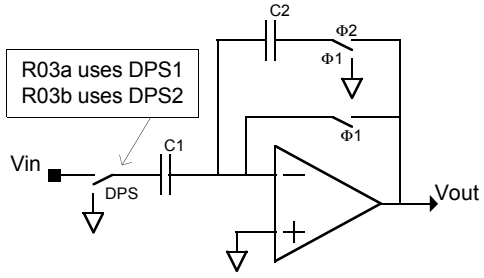
Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$during\ \phi 2, V_{out} = |V_{in}| \frac{C_1}{C_2} = |V_{in}| G$$

$$during\ \phi 1, V_{out} = VMR$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



$$G = \frac{C_1}{C_2}$$

Limitations on the Maximum Gain (G):

This IPmodule has a clock dependent maximum gain. The maximum gain can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a gain that is higher than the displayed maximum gain. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum gain is exceeded, the actual gain of this IPmodule may not equal the displayed realized value and simulated value, and the actual gain may not be equal to the actual gain on another identically programmed array. To avoid these problems, program the gain between the displayed limits.

R03b – Inverting Half Cycle Full Wave Rectifier

This IPmodule is an inverting half cycle full wave rectifier with negative output voltage. The entire input waveform is rectified to a negative signal. The output is valid on $\phi 2$ and clamped to VMR during $\phi 1$.

Phase Behavior:

Input sampled on: $\phi 1$, if Vin < VMR
$\phi 2$, if Vin > VMR
Output valid on: $\phi 2$ (compensated)

Programmable Parameters:

Pass Band Gain 0.01 – 12.7 V/V (at f_c = 250 kHz)*
(default 1.0 V/V)

* The maximum G is subject to clock frequency limitations as explained below.

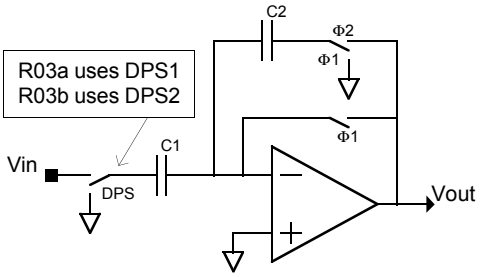
Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$during\ \phi 2, V_{out} = -|V_{in}|\frac{C_1}{C_2} = -|V_{in}|G$$

$$during\ \phi 1, V_{out} = VMR$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



$$G = \frac{C_1}{C_2}$$

Limitations on the Maximum Gain (G):

This IPmodule has a clock dependent maximum gain. The maximum gain can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a gain that is higher than the displayed maximum gain. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum gain is exceeded, the actual gain of this IPmodule may not equal the displayed realized value and simulated value, and the actual gain may not be equal to the actual gain on another identically programmed array. To avoid these problems, program the gain between the displayed limits.

R04a – Half Cycle Half Wave Rectifier

This IPmodule is a half cycle half wave rectifier with positive output voltage. Any portion of the input waveform above VMR is rectified to a positive signal. The output is valid on $\phi 2$ and clamped to VMR during $\phi 1$.

Phase Behavior:

Input sampled on: $\phi 1$, if Vin > VMR
Output valid on: $\phi 2$ (compensated)

Programmable Parameters:

Pass Band Gain 0.01 – 12.7 V/V (at f_c = 250 kHz)*
(default 1.0 V/V)

* The maximum G is subject to clock frequency limitations as explained below.

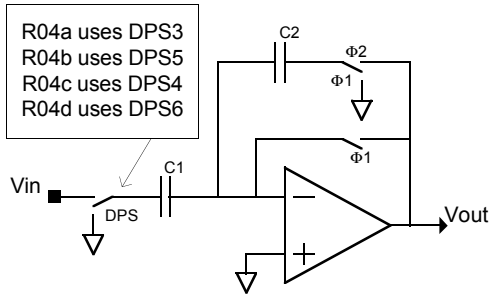
Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$if\ Vin > VMR\ and\ during\ \phi 2, V_{out} = Vin\frac{C_1}{C_2} = VinG$$

$$if\ Vin < VMR\ or\ during\ \phi 1, V_{out} = VMR$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



Limitations on the Maximum Gain (G):

This IPmodule has a clock dependent maximum gain. The maximum gain can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a gain that is higher than the displayed maximum gain. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum gain is exceeded, the actual gain of this IPmodule may not equal the displayed realized value and simulated value, and the actual gain may not be equal to the actual gain on another identically programmed array. To avoid these problems, program the gain between the displayed limits.

R04b – Half Cycle Inverting Half Wave Rectifier

This IPmodule is a half cycle inverting half wave rectifier with negative output voltage. Any portion of the input waveform above VMR is rectified to a negative signal. The output is valid on $\phi 2$ and clamped to VMR during $\phi 1$.

Phase Behavior:

Input sampled on: $\phi 2$, if Vin > VMR
Output valid on: $\phi 2$ (compensated)

Programmable Parameters:

Pass Band Gain 0.01 – 12.7 V/V (at f_c = 250 kHz)*
(default 1.0 V/V)

* The maximum G is subject to clock frequency limitations as explained below.

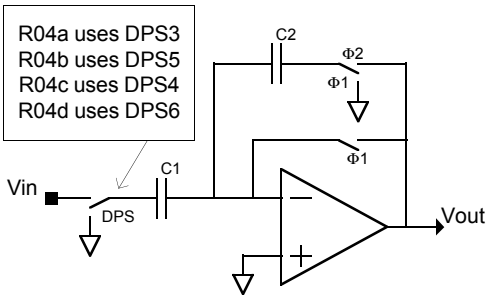
Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$if\ Vin > VMR\ and\ during\ \phi 2, V_{out} = -Vin\frac{C_1}{C_2} = -VinG$$

$$if\ Vin < VMR\ or\ during\ \phi 1, V_{out} = VMR$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



Limitations on the Maximum Gain (G):

This IPmodule has a clock dependent maximum gain. The maximum gain can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a gain that is higher than the displayed maximum gain. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum gain is exceeded, the actual gain of this IPmodule may not equal the displayed realized value and simulated value, and the actual gain may not be equal to the actual gain on another identically programmed array. To avoid these problems, program the gain between the displayed limits.

R04c – Half Cycle Negative Half Wave Rectifier

This IPmodule is a half cycle negative wave rectifier with negative output voltage. Any portion of the input waveform below VMR is rectified to a negative signal. The output is valid on $\phi 2$ and clamped to VMR during $\phi 1$.

Phase Behavior:

Input sampled on: $\phi 1$, if Vin < VMR
Output valid on: $\phi 2$ (compensated)

Programmable Parameters:

Pass Band Gain 0.01 – 12.7 V/V (at f_c = 250 kHz)*
(default 1.0 V/V)

* The maximum G is subject to clock frequency limitations as explained below.

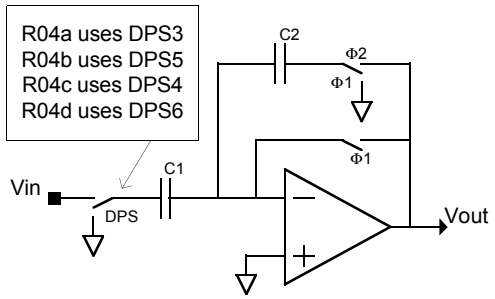
Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$if\ Vin < VMR\ and\ during\ \phi 2, V_{out} = Vin\frac{C_1}{C_2} = VinG$$

$$if\ Vin > VMR\ or\ during\ \phi 1, V_{out} = VMR$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



Limitations on the Maximum Gain (G):

This IPmodule has a clock dependent maximum gain. The maximum gain can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a gain that is higher than the displayed maximum gain. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum gain is exceeded, the actual gain of this IPmodule may not equal the displayed realized value and simulated value, and the actual gain may not be equal to the actual gain on another identically programmed array. To avoid these problems, program the gain between the displayed limits.

R04d – Half Cycle Inverting Negative Half Wave Rectifier

This IPmodule is a half cycle inverting negative wave rectifier with positive output voltage. Any portion of the input waveform below VMR is rectified to a positive signal. The output is valid on $\phi 2$ and clamped to VMR during $\phi 1$.

Phase Behavior:

Input sampled on: $\phi 2$, if Vin < VMR
Output valid on: $\phi 2$ (compensated)

Programmable Parameters:

Pass Band Gain 0.01 – 12.7 V/V (at f_c = 250 kHz)*
(default 1.0 V/V)

* The maximum G is subject to clock frequency limitations as explained below.

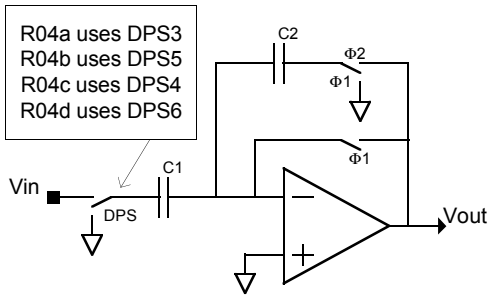
Circuit Diagram and Controlling Equations:

The transfer function of this circuit is:

$$if\ Vin < VMR\ and\ during\ \phi 2, V_{out} = -Vin\frac{C_1}{C_2} = -VinG$$

$$if\ Vin > VMR\ or\ during\ \phi 1, V_{out} = VMR$$

where C_1 and C_2 are the input and feedback capacitors as depicted in the figure:



Limitations on the Maximum Gain (G):

This IPmodule has a clock dependent maximum gain. The maximum gain can be increased by decreasing the clock frequency. When changing clock frequencies, it is usually best to change the divisor for the clock rather than which clock is used, so that the change will be applied to all IPmodules in the signal path. The IPmodule can be programmed with a gain that is higher than the displayed maximum gain. In this case, the realized values will have a note attached that refers you to this help. Due to gain bandwidth limitations of the amplifier, when the displayed maximum gain is exceeded, the actual gain of this IPmodule may not equal the displayed realized value and simulated value, and the actual gain may not be equal to the actual gain on another identically programmed array. To avoid these problems, program the gain between the displayed limits.

R05b – Inverting Half Wave Rectifier

This IPmodule is an inverting half wave rectifier. Any portion of the input waveform greater than VMR, is rectified with gain to a negative signal.

Phase Behavior:

Input sampled on: ϕ2, if Vin > VMR
Output valid on: ϕ1 and ϕ2
(compensated in ϕ2)

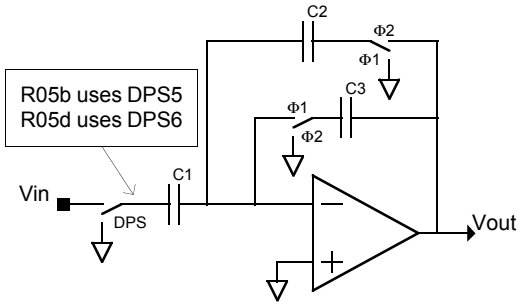
Programmable Parameters:

Pass Band Gain 0.01 – 100.0 V/V
(default 1.0 V/V)

Circuit Diagram and Controlling Equations:

$$if\ V_{in} > VMR, V_{out} = -\frac{C_1}{C_2}V_{in} = -GV_{in}$$

$$if\ V_{in} < VMR, V_{out} = VMR$$



R05d – Inverting Negative Half Wave Rectifier

This IPmodule is an negative inverting half wave rectifier. Any portion of the input waveform less than VMR, is rectified with gain to a positive signal.

Phase Behavior:

Input sampled on: $\phi 2$, if Vin < VMR
Output valid on: $\phi 1$ and $\phi 2$
(compensated in $\phi 2$)

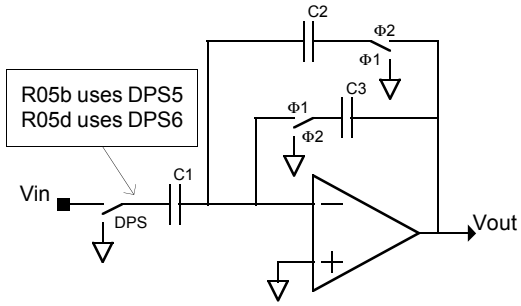
Programmable Parameters:

Pass Band Gain	0.01 – 100.0 V/V (default 1.0 V/V)

Circuit Diagram and Controlling Equations:

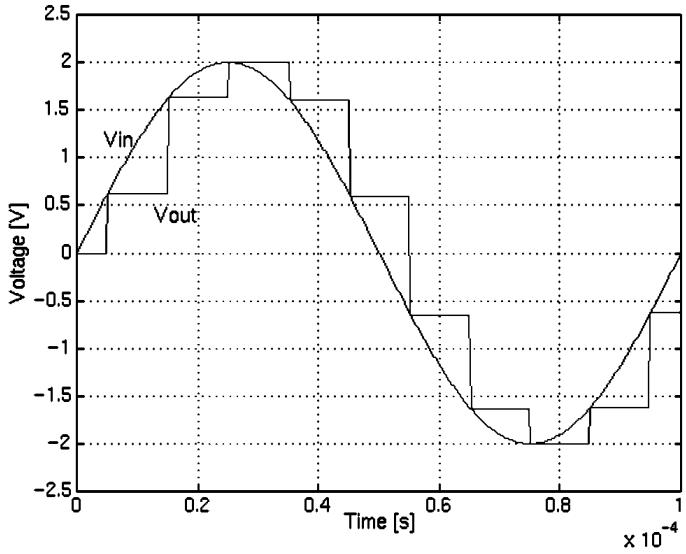
$$if\ V_{in} < VMR, V_{out} = -\frac{C_1}{C_2} V_{in} = -GV_{in}$$

$$if\ V_{in} > VMR, V_{out} = VMR$$



S01p1 – Sample and Hold

This IPmodule is a sample-and-hold stage. There are no programmable parameters for this IPmodule. The input waveform is conditioned to produce the following output:



Some IPmodules produce output that is valid only in phase 1. This circuit may be used to create a valid signal in phase 2 by holding the voltage value at the end of phase 1. It may also be used to change the track-type signal in phase 1 to a hold-type signal.

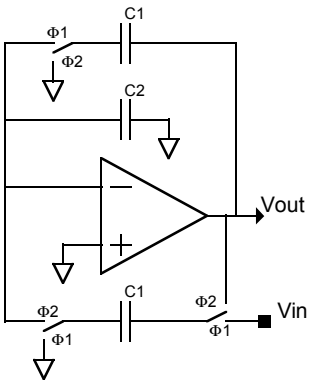
Phase Behavior:

Input sampled on: $\phi 1$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

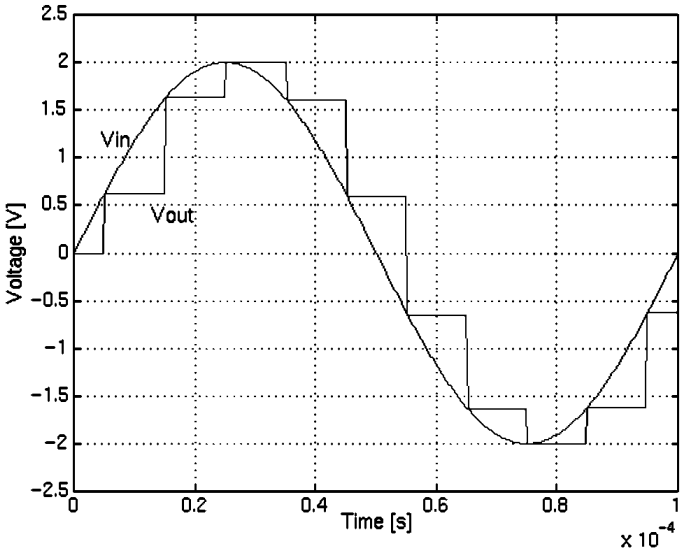
none

Circuit Diagram and Controlling Equations:



S01p2 – Sample and Hold

This IPmodule is a sample-and-hold stage. There are no programmable parameters for this IPmodule. The input waveform is conditioned to produce the following output:



Some IPmodules produce output that is valid only in phase 2. This circuit may be used to create a valid signal in phase 1 by holding the voltage value at the end of phase 2. It may also be used to change the track-type signal in phase 2 to a hold-type signal.

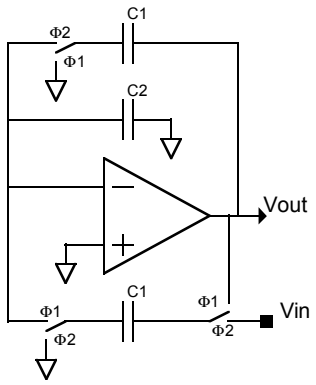
Phase Behavior:

Input sampled on: $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

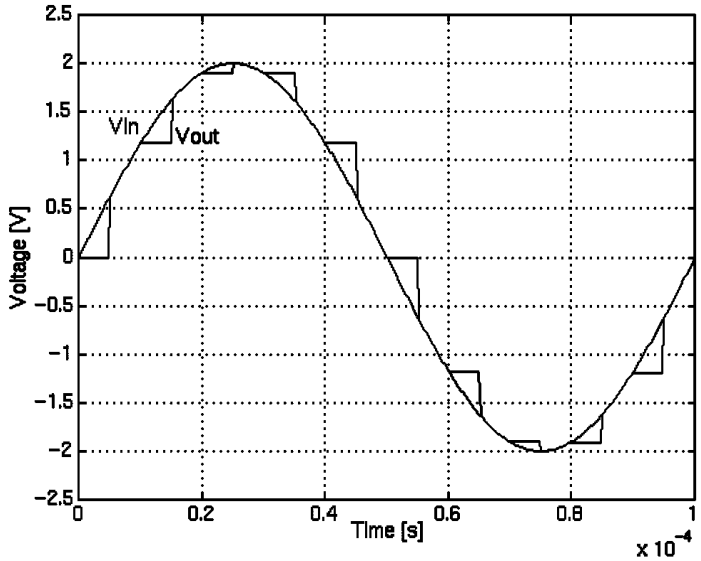
none

Circuit Diagram and Controlling Equations:



S02p1 – Track and Hold

This IPmodule is a track-and-hold stage. The input is sampled (tracked) in phase 1. There are no programmable parameters associated with this circuit. The input waveform is conditioned to produce the following output:



Some IPmodules produce output that is valid only in phase 1. This circuit may be used to create a valid signal in phase 2 by holding the voltage value at a constant level sampled at the end of phase 1.

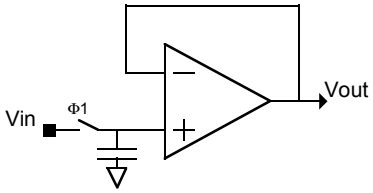
Phase Behavior:

Input sampled on: $\phi 1$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

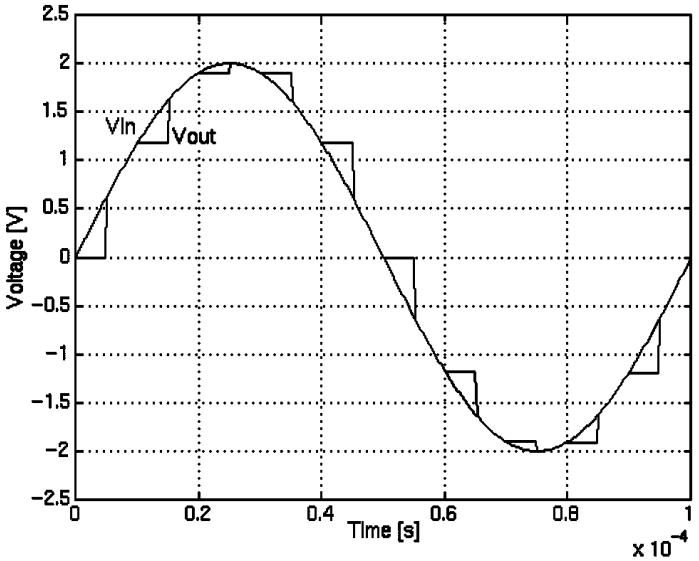
none

Circuit Diagram and Controlling Equations:



S02p2 – Track and Hold

This IPmodule is a track-and-hold stage. The input is sampled (tracked) in phase 2. There are no programmable parameters associated with this circuit. The input waveform is conditioned to produce the following output:



Some IPmodules produce output that is valid only in phase 2. This circuit may be used to create a valid signal in phase 1 by holding the voltage value at a constant level sampled at the end of phase 2.

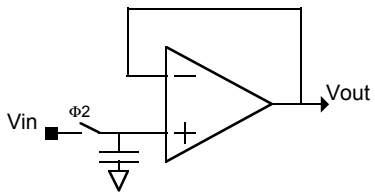
Phase Behavior:

Input sampled on: $\phi 2$
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

none

Circuit Diagram and Controlling Equations:



V01a – Voltage Source, +2.5 VDC

This full cycle IPmodule supplies a DC reference voltage of +2.5 V. There are no user programmable parameters.

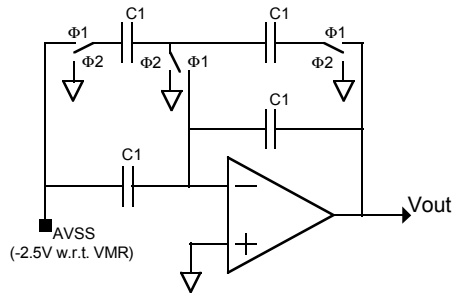
Phase Behavior:

Input sampled on: none
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

none

Circuit Diagram and Controlling Equations:



This is basically a G01 equivalent stage with the gain set to -1 and the input tied to AVSS. AVSS is -2.5V with respect to VMR.

V01b – Voltage Source, -2.5 VDC

This full cycle IPmodule supplies a DC reference voltage of -2.5 V. There are no user programmable parameters.

Phase Behavior:

Input sampled on: none
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

none

Circuit Diagram and Controlling Equations:

The output of the V01b IPmodule is tied to AVSS, which is -2.5V with respect to VMR.

V02a – Positive DC Voltage Source

This full cycle IPmodule supplies a DC positive reference voltage.

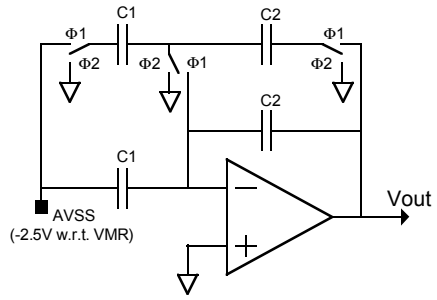
Phase Behavior:

Input sampled on: none
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

DC Voltage	0.01 – 2.5 V (default 1.0 V)

Circuit Diagram and Controlling Equations:



The V02a IPmodule is a combination of a -2.5V source followed by an inverting programmable gain stage.

The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relation:

$$\frac{V}{2.5} = \frac{C_1}{C_2}$$

V02b – Negative DC Voltage Source

This full cycle IPmodule supplies a DC negative reference voltage.

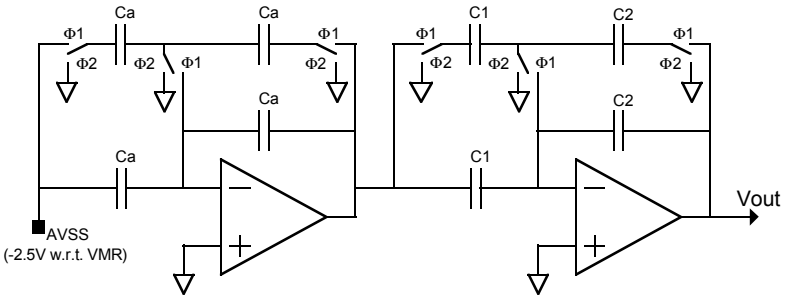
Phase Behavior:

Input sampled on: none
Output valid on: $\phi 1$ and $\phi 2$

Programmable Parameters:

DC Voltage	-2.5 – -0.01 V (default -1.0 V)

Circuit Diagram and Controlling Equations:



The V02b IPmodule is a combination of a +2.5V source (V01a) followed by an inverting programmable gain stage.

The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relation:

$$\frac{V}{2.5} = \frac{C_1}{C_2}$$

V03 – Voltage Source, 0.0 V

This full cycle IPmodule supplies a DC reference voltage 0.0V (VMR). There are no user programmable parameters.

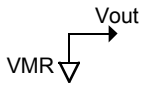
Phase Behavior:

Input sampled on: none
Output valid on: ϕ1 and ϕ2

Programmable Parameters:

none

Circuit Diagram and Controlling Equations:



The output of the VO3 IPmodule is simply connected to the VMR signal available within the CAB.

Anadigm® is pleased to offer our
customers direct access to the following offices:

WEB
http://www.Anadigm.com/

USA
Anadigm® Inc.
21615 Stevens Creek Blvd
Cupertino
CA 95014

Tel: +1 408 996 2091
Fax: +1 408 996 2093

Anadigm® Inc.
7855 South River Parkway
Suite 205
Tempe
AZ 85284

Tel: +1 480 344 5271
Fax: +1 480 344 5277

UK
Anadigm® Ltd.
3-5 Mallard Court
Mallard Way
Crewe
CW1 6ZG

Tel: +44 (0) 1270 531990
Fax: +44 (0) 1270 531999

GERMANY
Anadigm® Ltd.
Gottlieb-Daimler Str. 6
82140 Olching

Tel: +49 (0) 8142 4485830
Fax: +49 (0) 8142 4485840