

## Timing Speculation in FPGAs: Probabilistic Inference of Data Dependent Failure Rates

Sumanta Chaudhuri, Justin S. J. Wong & Peter Y. K. Cheung

October 20, 2013



- ▶ Problem Formulation/Introduction
- ▶ Inference Method
- ▶ Experimental Setup & Results
- ▶ Conclusion

# Problem Statement

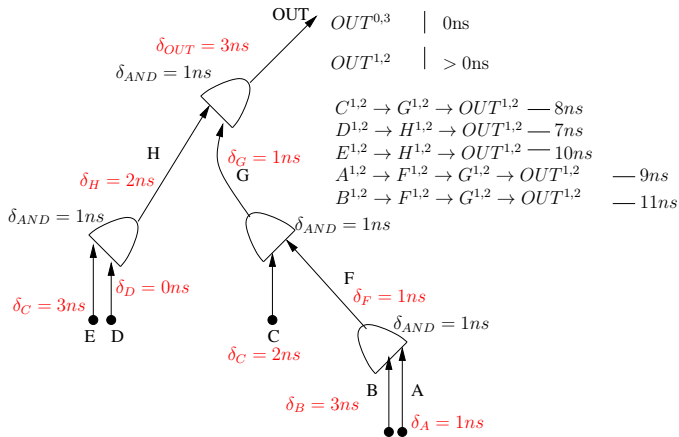


Figure 1: Data Dependent Path Excitation

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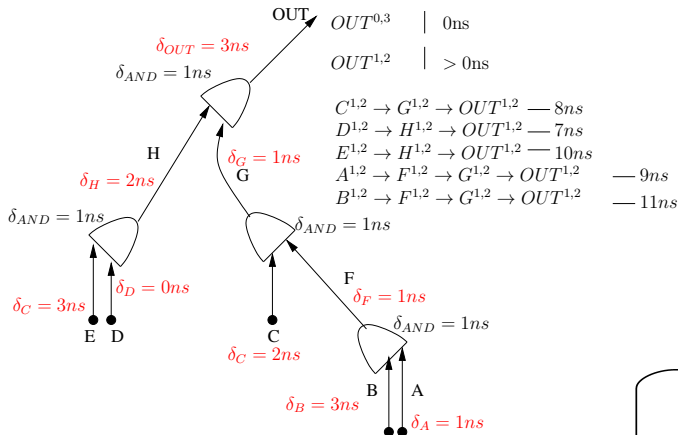


Figure 2: Data Dependent Path Excitation

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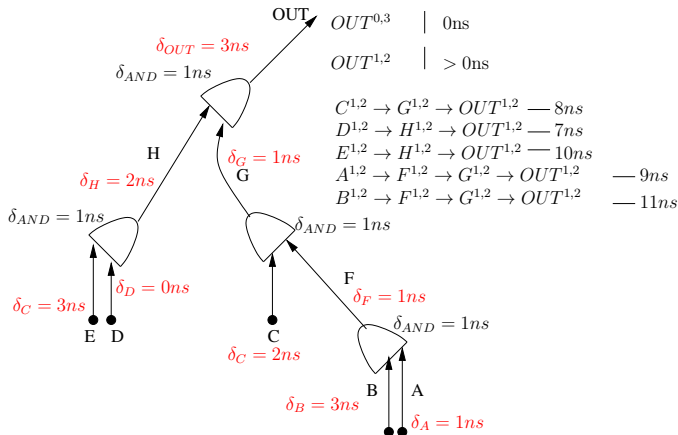


Figure 3: Data Dependent Path Excitation

We would like to find the probabilities of excitation of each path.

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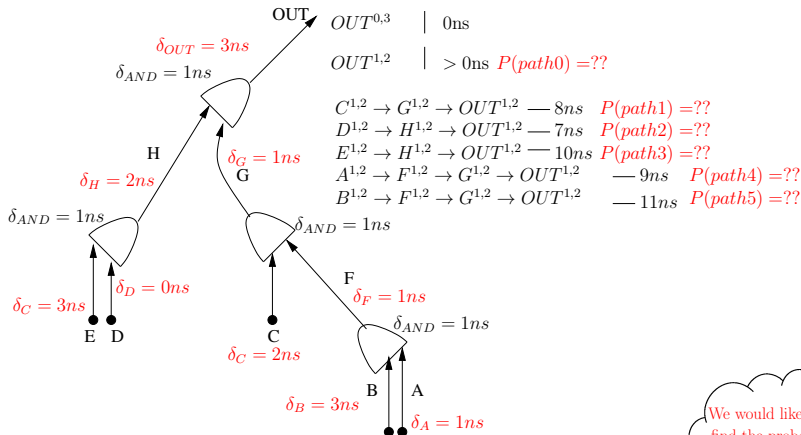


Figure 4: Data Dependent Path Excitation

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Taken from: [Razor, Dan Ernst et. al. MICRO 36 2003](#)

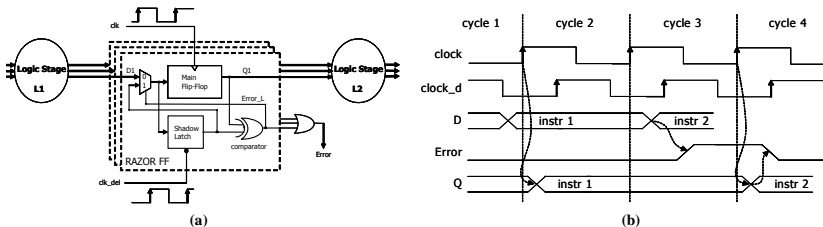


Figure 1. Pipeline augmented with Razor latches and control lines.

Throughput:

$$\frac{1}{(1 - P_{err}) \times T_{clk} + 2 \times P_{err} \times T_{clk}}$$

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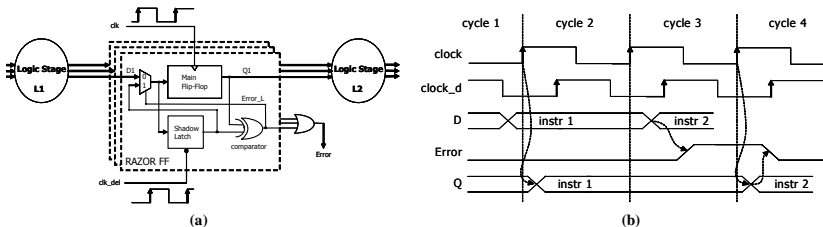


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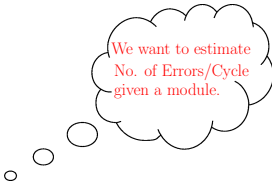
We want to find  $P_{err}$  given a Logic Stage.



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Implements 3 of the Intel RMS Benchmark Suite in presence of  $3 \times 10^{-4}$  errors/cycle, with reasonable accuracy (90 %).  
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We want to estimate  
No. of Errors/Cycle  
given a module.

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- ▶ In this work we investigate the **data-dependence** of timing errors.
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- ▶ Our method is geared towards **FPGA Implementations**.

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- ▶ Can be used for symbolic calculation of probabilities instead of exhaustive Monte-Carlo simulation.

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  - ▶ Associated with each node  $X_i$ , there is a Conditional Probability Distribution

$$P(X_i | Pa_{X_i}^G)$$

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- ▶ **Probability Queries.**

- ▶ Collection of methods to infer the marginal(joint) probabilities of a set of event(s).

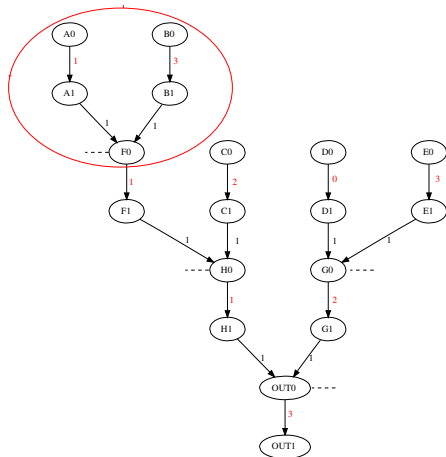
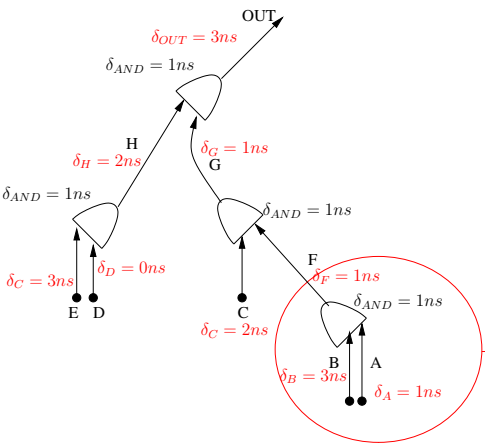


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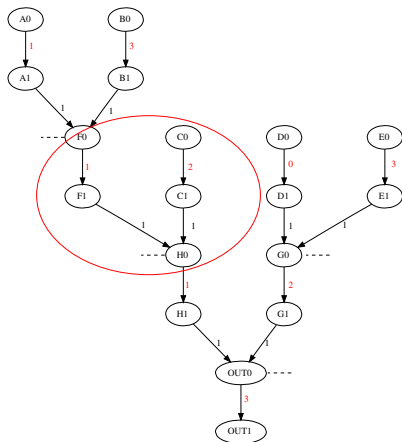
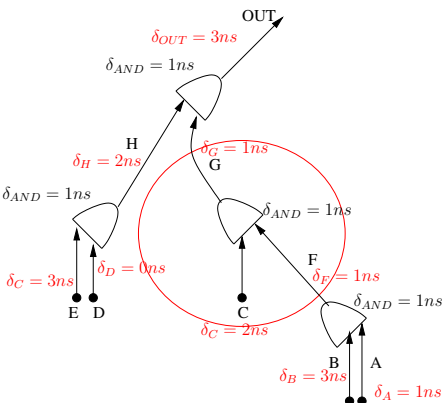
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- ▶ some example events:
  - $X^{1,2}$ : either of transition 1 or transition 2 on  $X$ .
  - $(X^1, Y^1, Z^2)$ : transition 1 on  $X$ , transition 1 on  $Y$  and transition 2 on  $Z$ .

# Bayesian Networks: Structure



Nodes (RVs) corresp. to each terminal of nets in the circuit.  
Edges for causal influence.

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Table 1: Derivation of Transition Tables from Truth Tables.

Binary Format					Decimal Format																																																						
<table border="1" style="display: inline-table; margin-right: 20px;"> <tr><th><math>a \backslash b</math></th><th>0</th><th>1</th></tr> <tr><th>0</th><td>0</td><td>0</td></tr> <tr><th>1</th><td>0</td><td>1</td></tr> </table> <span style="font-size: 2em; vertical-align: middle;">⊗</span> <table border="1" style="display: inline-table; margin-left: 20px;"> <tr><th><math>a \backslash b</math></th><th>0</th><th>1</th></tr> <tr><th>0</th><td>0</td><td>0</td></tr> <tr><th>1</th><td>0</td><td>1</td></tr> </table> <span style="font-size: 2em; vertical-align: middle;">=</span>					$a \backslash b$	0	1	0	0	0	1	0	1	$a \backslash b$	0	1	0	0	0	1	0	1																																					
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CPD size =  $4 \times 4^{N_{inputs}}$

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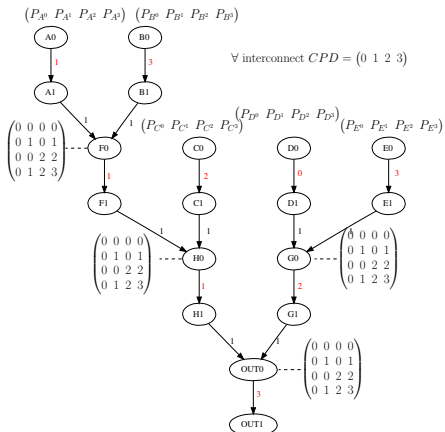
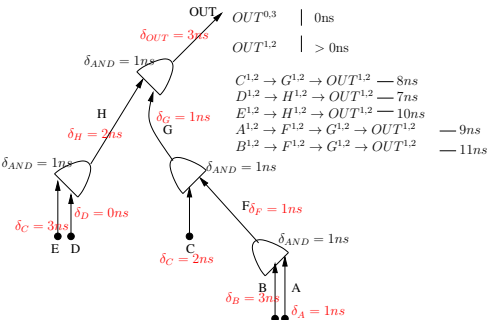
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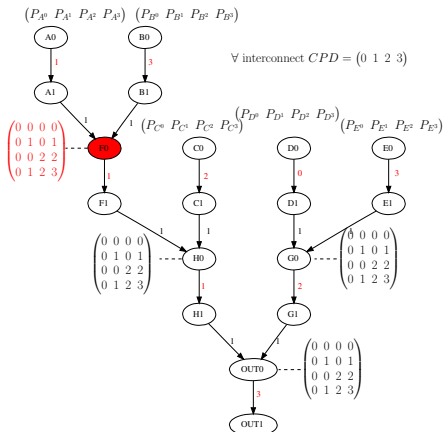
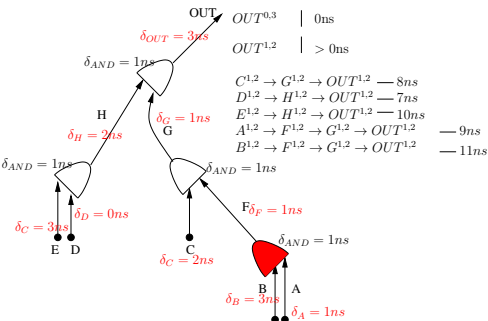
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# Bayesian Networks: Local Probability Model



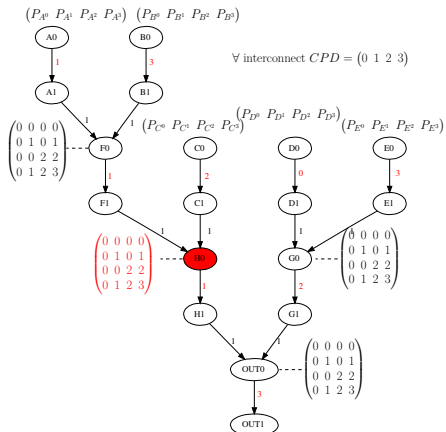
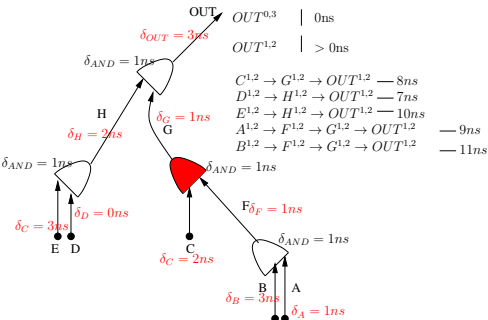
The Local Probability Models are attached to each gate output.

# Bayesian Networks: Local Probability Model



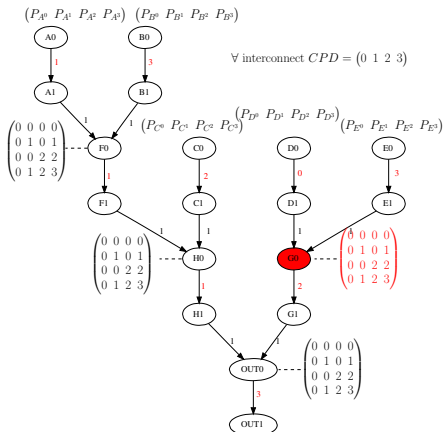
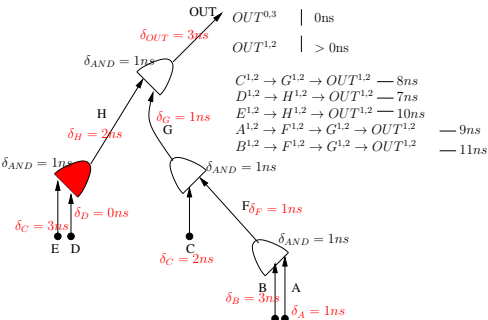
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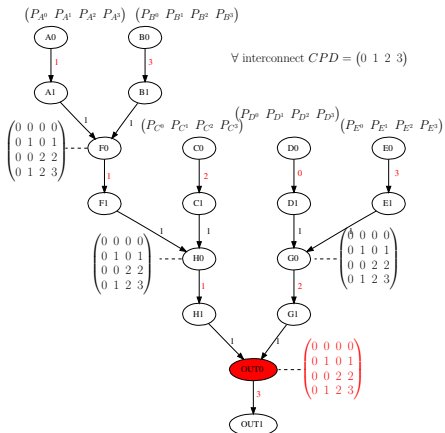
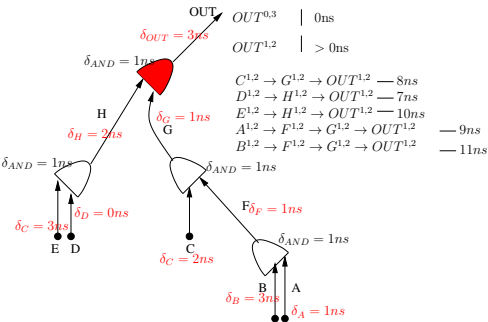
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Using MATLAB BNT Toolbox  
the BN can be queried for

- ▶ Joint Distribution:

e.g  $P(A0^1, A1^1, F0^1, F1^1, H0^1, H1^1, OUT0^1, OUT^1)$

- ▶ Marginal Distribution:

e.g  $P(OUT1^{0,3})$

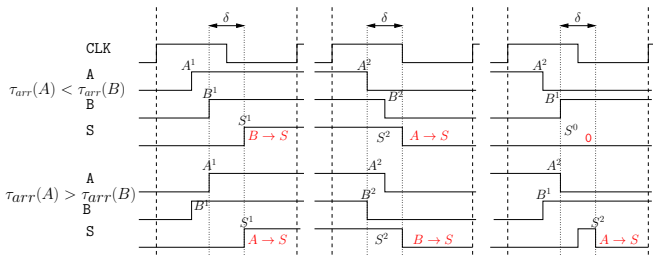
- ▶ Exact Algorithms

- ▶ Variable Elimination
- ▶ Junction Tree
- ▶ Quickscore
- ▶ Pearl (for Polytree)

- ▶ Approximation Algorithms

- ▶ Belief Propagation
- ▶ Gibbs Sampling
- ▶ Likelihood Weighting
- ▶ Pearl (DAG)

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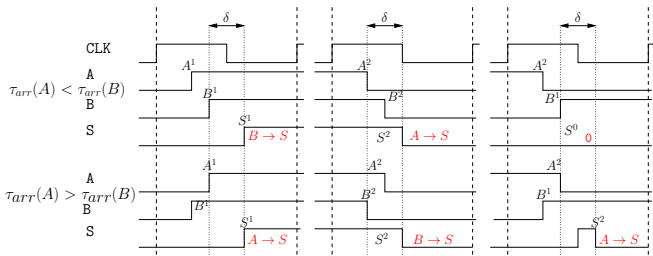


$A \rightarrow S$

$$P(\tau_{arr}(S) = \tau_{arr}(A) + \delta_{AND} | A, B, \tau_{arr}(A), \tau_{arr}(B))$$

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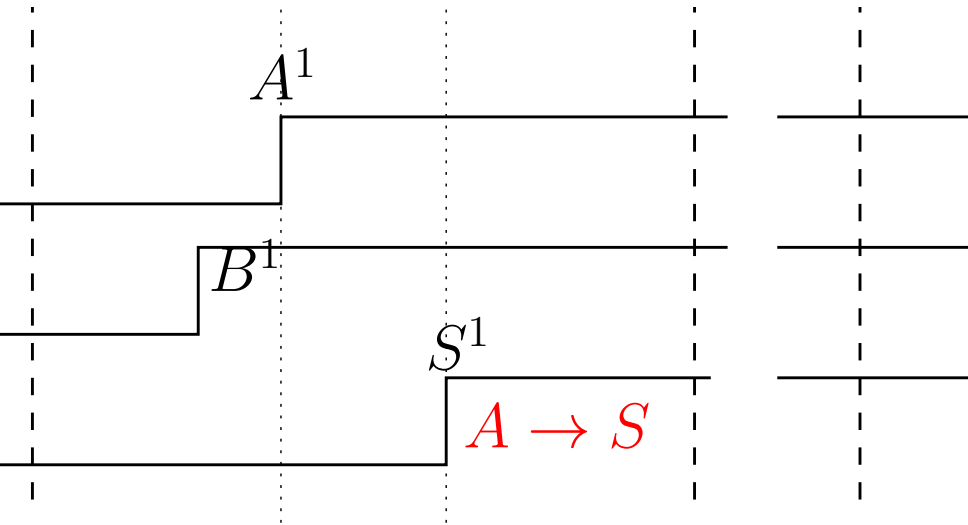


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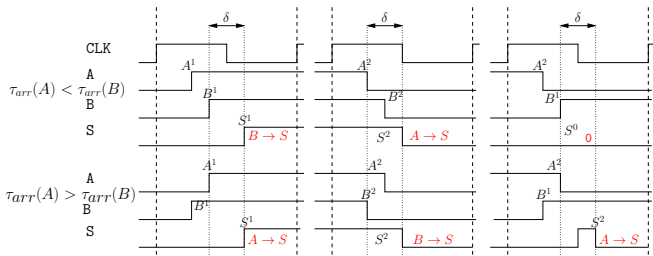
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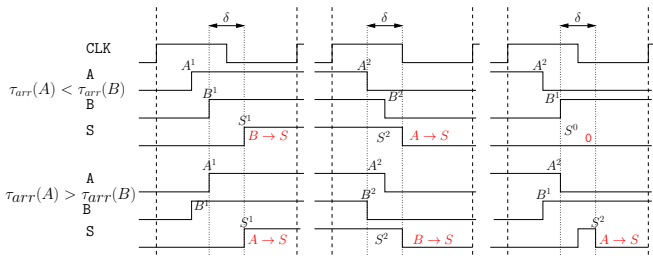


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# Bayesian Networks: Local Probability Model

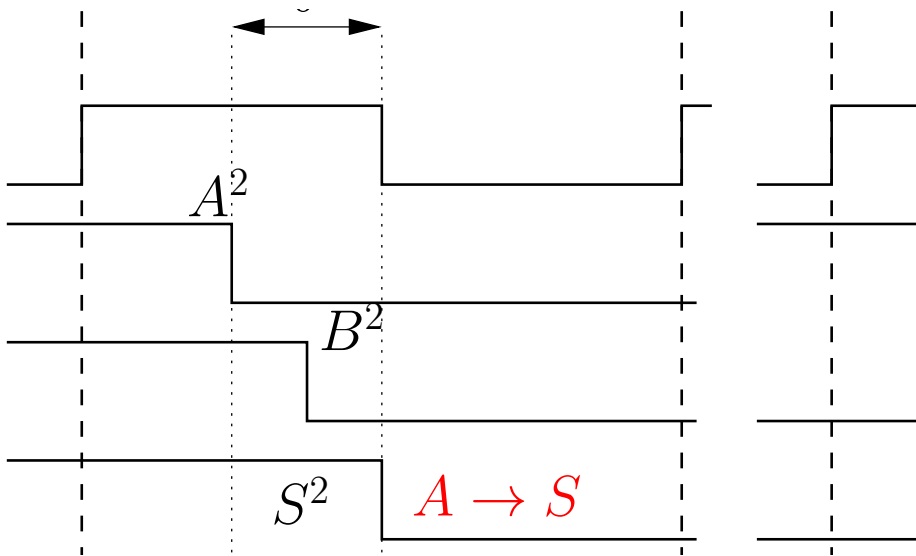


$A \rightarrow S$

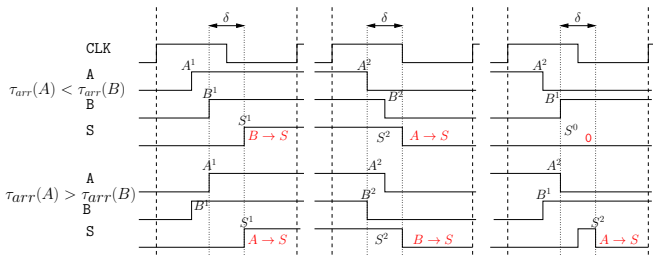
$$P(\tau_{arr}(S) = \tau_{arr}(A) + \delta_{AND} | A, B, \tau_{arr}(A), \tau_{arr}(B))$$

$a \backslash b$	$b^0$	$b^1$	$b^2$	$b^3$
$a^0$	0	0	0	0
$a^1$	0	$P(\tau_{arr}(B) < \tau_{arr}(A))$	0	1
$a^2$	0	$P(\tau_{arr}(B) < \tau_{arr}(A))$	$P(\tau_{arr}(B) \geq \tau_{arr}(A))$	1
$a^3$	0	0	0	0

# Bayesian Networks: Local Probability Model



# Bayesian Networks: Local Probability Model



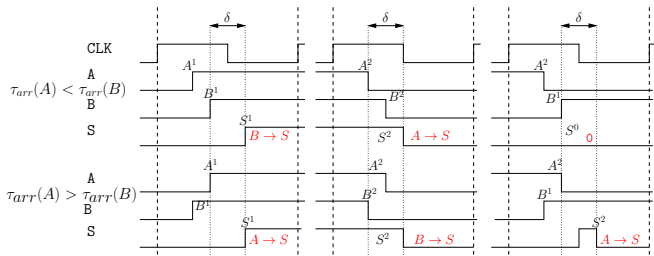
$A \rightarrow S$

$$P(\tau_{arr}(S) = \tau_{arr}(A) + \delta_{AND} | A, B, \tau_{arr}(A), \tau_{arr}(B))$$

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# Bayesian Networks: Local Probability Model

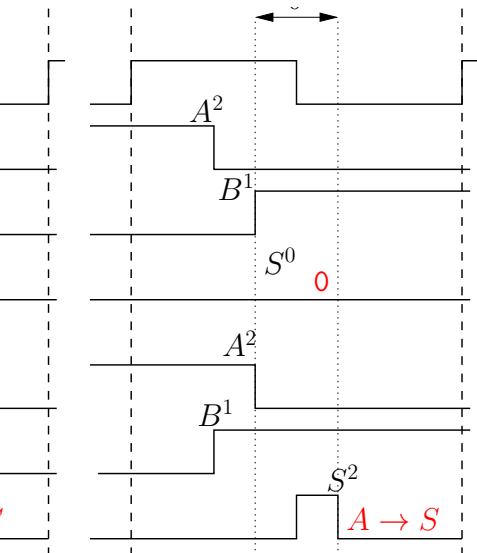


$A \rightarrow S$

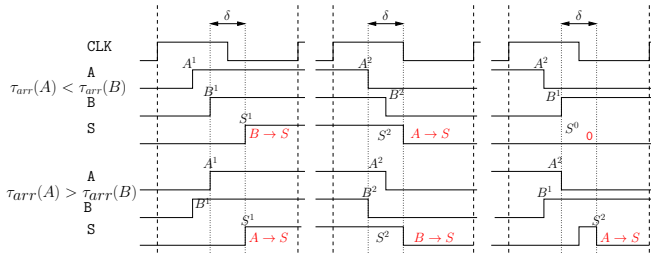
$$P(\tau_{arr}(S) = \tau_{arr}(A) + \delta_{AND} | A, B, \tau_{arr}(A), \tau_{arr}(B))$$

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# Bayesian Networks: Local Probability Model



# Bayesian Networks: Local Probability Model



$A \rightarrow S$

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$a^3$	0	0	0	0

# Algorithms: BN Construction

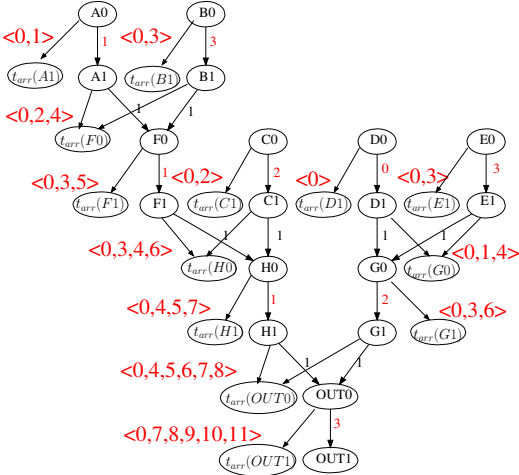
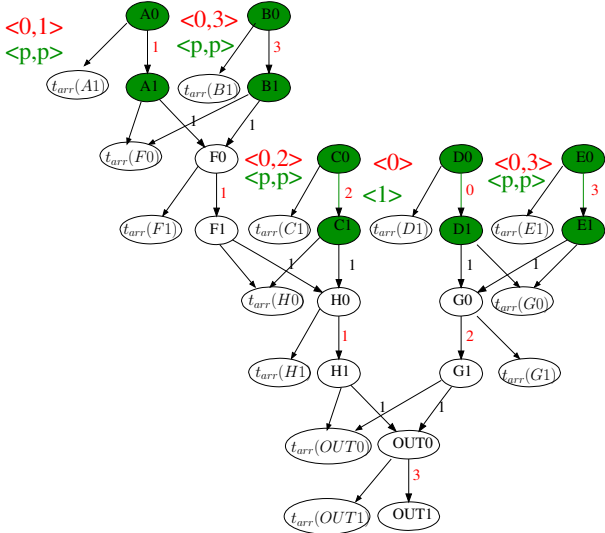
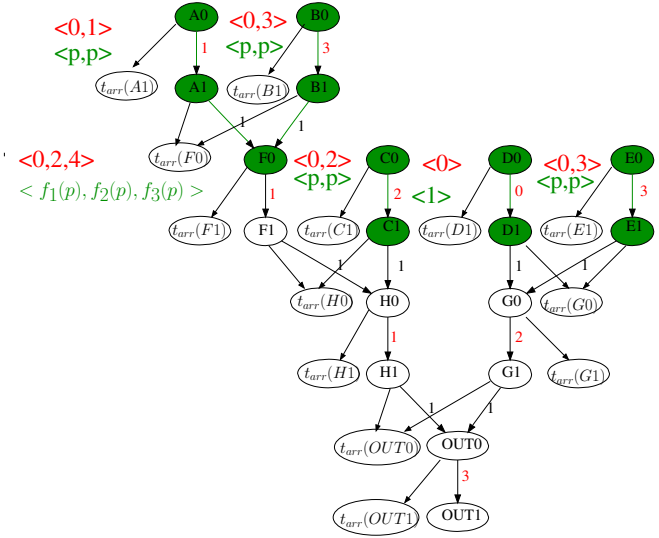


Figure 5: The same BN of figure 23 augmented with  $\tau_{arr}$  nodes. The event space  $\Omega$  for each RV  $\tau_{arr}$  is shown in red.

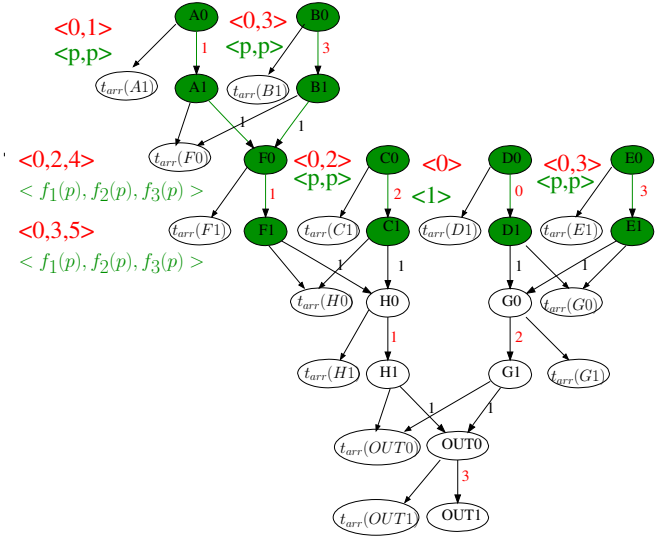
# Algorithms: BN Inference



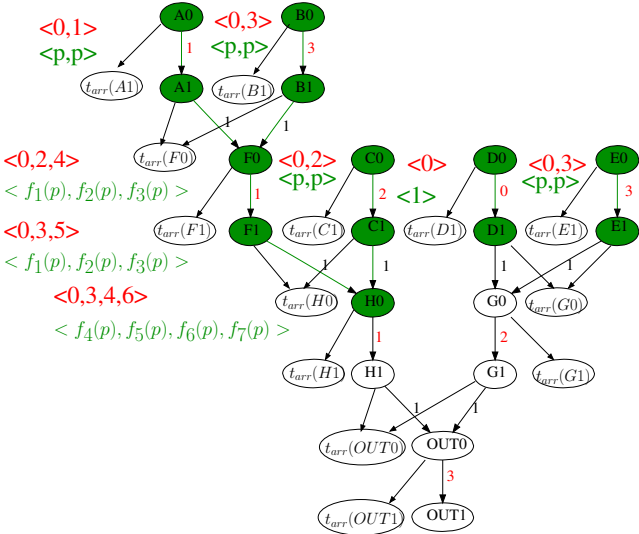
# Algorithms: BN Inference



# Algorithms: BN Inference

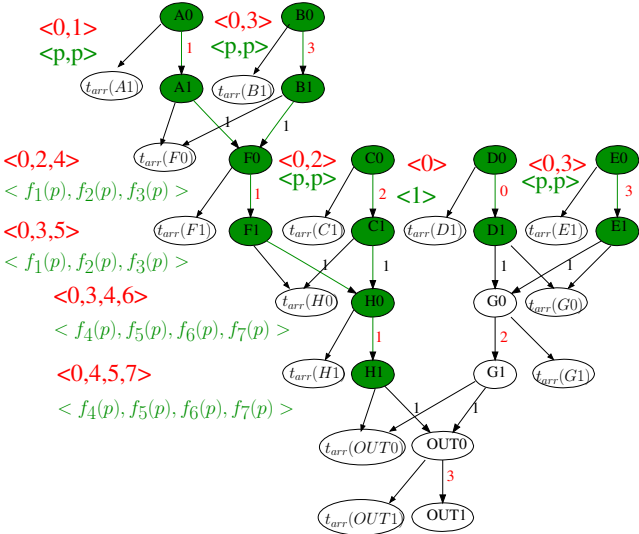


# Algorithms: BN Inference

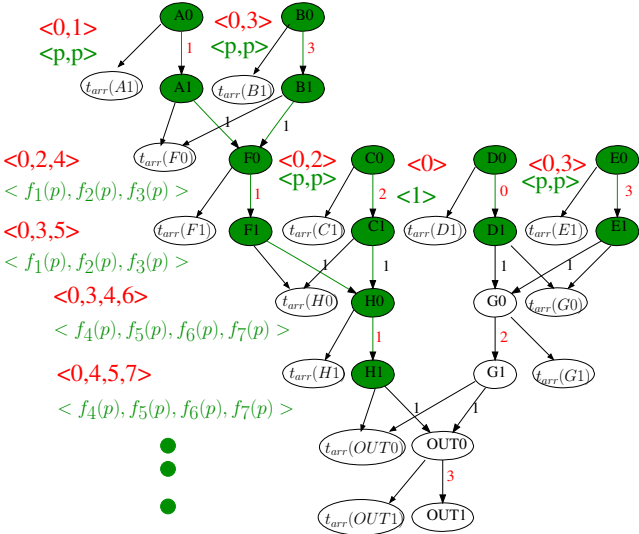




# Algorithms: BN Inference



# Algorithms: BN Inference



## Summary of Assumptions

- ▶ We assume that only one event occurs on any input to a gate in the netlist, within a single clock period. For outputs, if there are more than one events, we consider the latest event only.

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- ▶ We assume that only one event occurs on any input to a gate in the netlist, within a single clock period. For outputs, if there are more than one events, we consider the latest event only.
- ▶ We made an assumption that for any signal  $A$ ,  $P(\tau_{arr}(A^i)) = \text{mean}(\tau_{arr}(A))$  that is we ignore the individual arrival times of each event, replace it by the average.
- ▶ In actual operation there is an **Aliasing Behaviour**, that is the errors from one clock period are spilled into the next one. We don't take into account this effect.

## Simulation Results

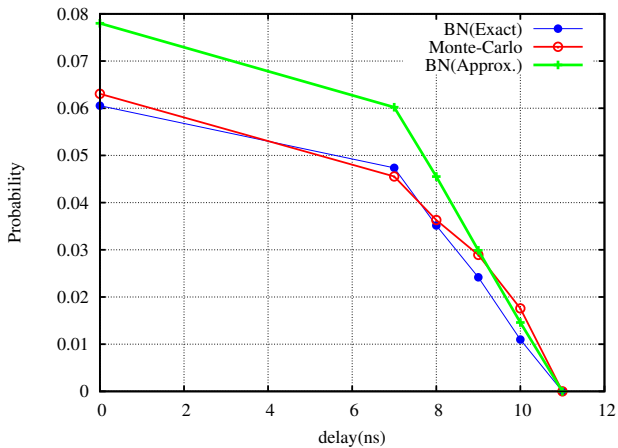
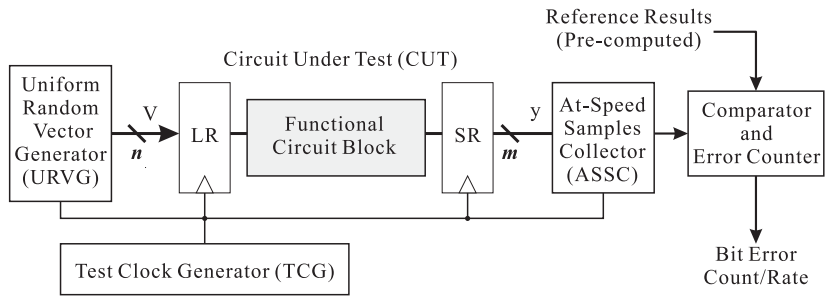
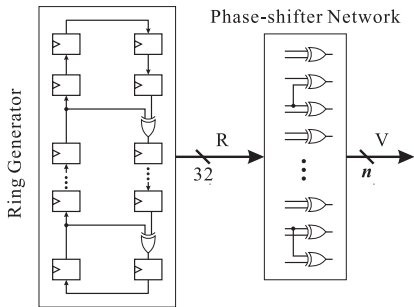


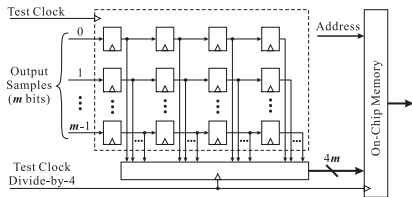
Figure 6: Comparison of MC simulations, and BN inference for example circuit

# FPGA Implementation: Cyclone III





**Figure 7:** Circuit diagram of the Uniform Random Vector Generator (URVG).



**Figure 8:** Circuit diagram of the At-Speed Samples Collector (ASSC).



# 4X4 Multiplier

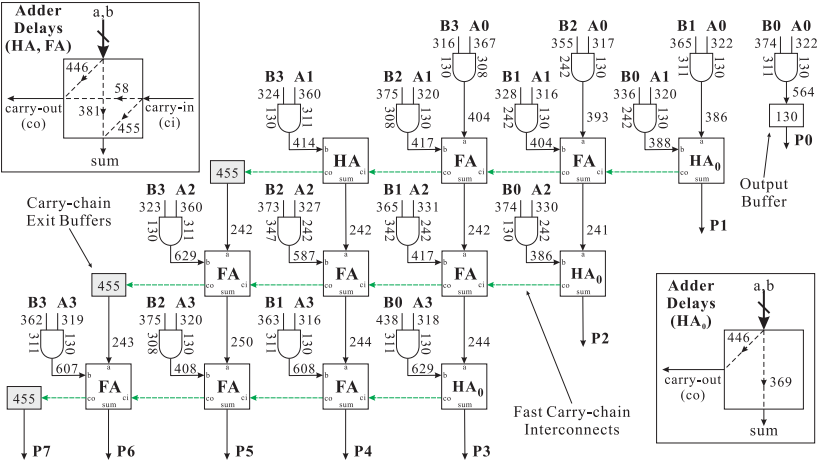
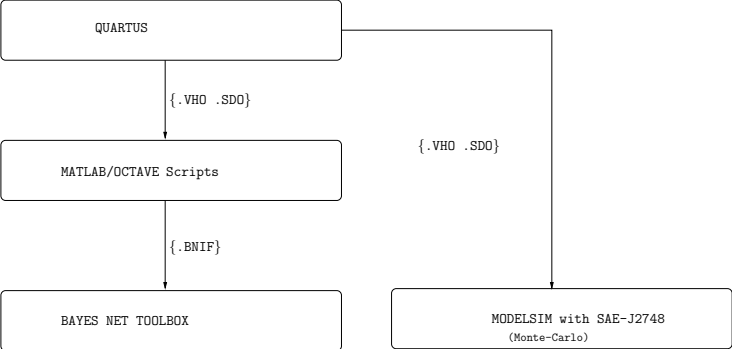
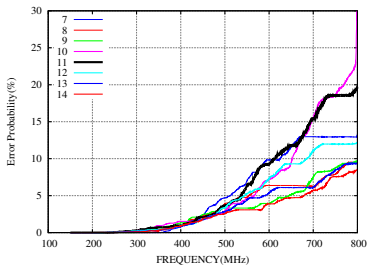


Figure 9: The adder based 4x4 multiplier circuit tested on the Cyclone III.

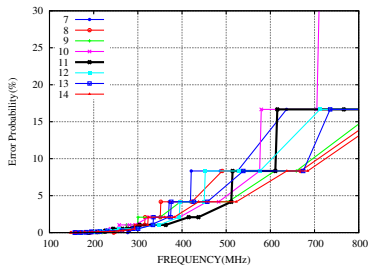
# FPGA Implementation: Flow



# Results and Comparison: 15 bit RCA 8 MSBs

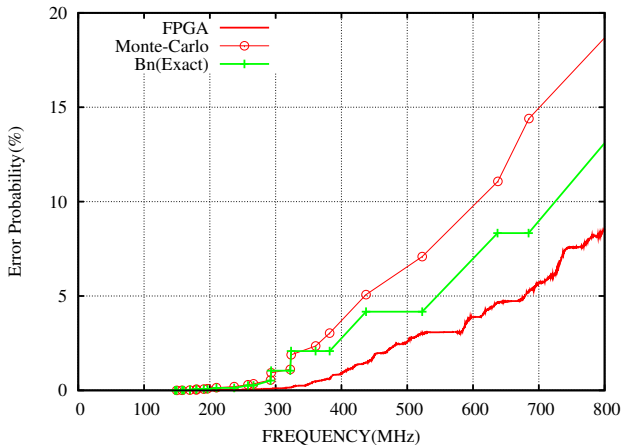


(a) 8 MSBs (CYCLONE III FPGA).



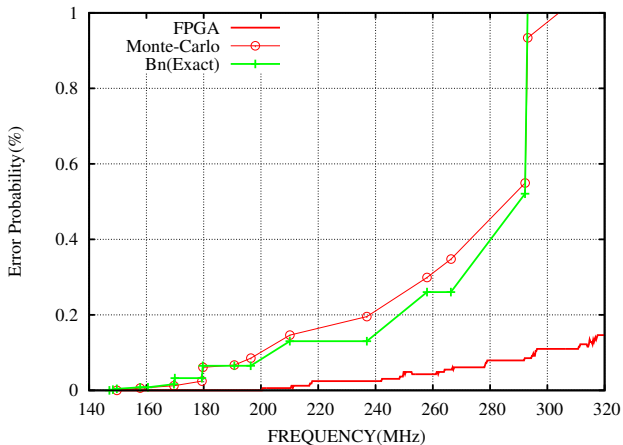
(b) 8 MSBs (BN inference).

## Results and Comparison: 15 bit RCA MSB



(c) MSB(14):comparison with BN and Monte-Carlo simulation.

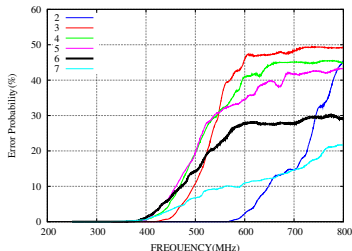
## Results and Comparison: 15 bit RCA MSB(Zoomed)



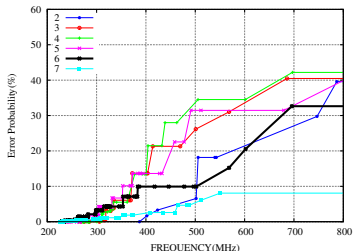
(d) MSB(14) Zoomed to (140-300) MHz Range, 140 MHz is the predicted  $f_{max}$  from STA

# Results and Comparison: 4x4 Array Multiplier 6 MSBs

Delay Assumption 1: Carry always arrives late !



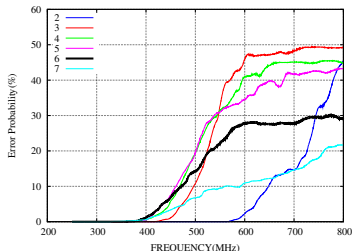
(e) 6 MSBs (CYCLONE III FPGA).



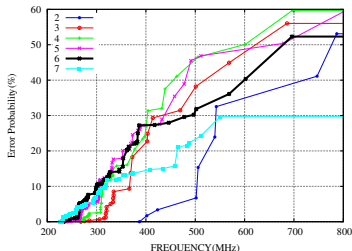
(f) 6 MSBs (Bn Inference).

## Results and Comparison: 4x4 Array Multiplier 6 MSBs

Delay Assumption 2:  $P(\tau_{arr}(C_{in}) \geq \tau_{arr}(A)) = P(\tau_{arr}(A) \geq \tau_{arr}(C_{in})) = 0.5$ .

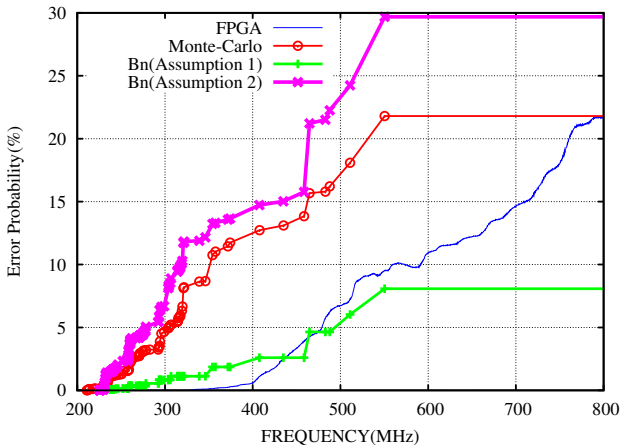


(g) 6 MSBs (CYCLONE III FPGA).



(h) 6 MSBs (Bn Inference).

## Results and Comparison: 4x4 Array Multiplier MSB



(i) Failure rates for the MSB(7) and comparison with BN and Monte-Carlo simulation. 210MHz is the predicted  $f_{max}$  from STA.



- ▶ We modeled combinatorial datapaths with Bayesian Network, in order to infer failure probabilities given a certain clock frequency.
- ▶ Comparison of error profiles of different implementations is possible with this method.
- ▶ Useful for design/prediction of achievable throughput (timing speculation), and achievable accuracy (Probabilistic Computing).

### TODO (Chronological):

- ▶ Define a metric for goodness-of-fit.
- ▶ Analysis of Run-Time.
- ▶ Development of a generalised tool: BEST (BN based Error Speculation for Timing.)
- ▶ Including functional errors into the model.



.  
Bayes net toolbox.

<http://code.google.com/p/bnt/>.



M. Dietrich, U. Eichler, and J. Haase.

Digital statistical analysis using vhdl: impact of variations on timing and power using gate-level monte carlo simulation.

*In Proceedings of the Conference on Design, Automation and Test in Europe, DATE '10*, pages 1007–1010, 3001 Leuven, Belgium, Belgium, 2010. European Design and Automation Association.



D. Koller and N. Friedman.

*Probabilistic Graphical Models - Principles and Techniques*.  
MIT Press, 2009.

Bon Apetit !!