TELECOM ParisTech

Une école de l'IMT

Multi-level embedded system design

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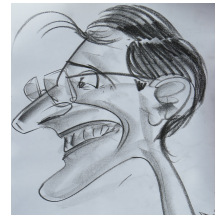

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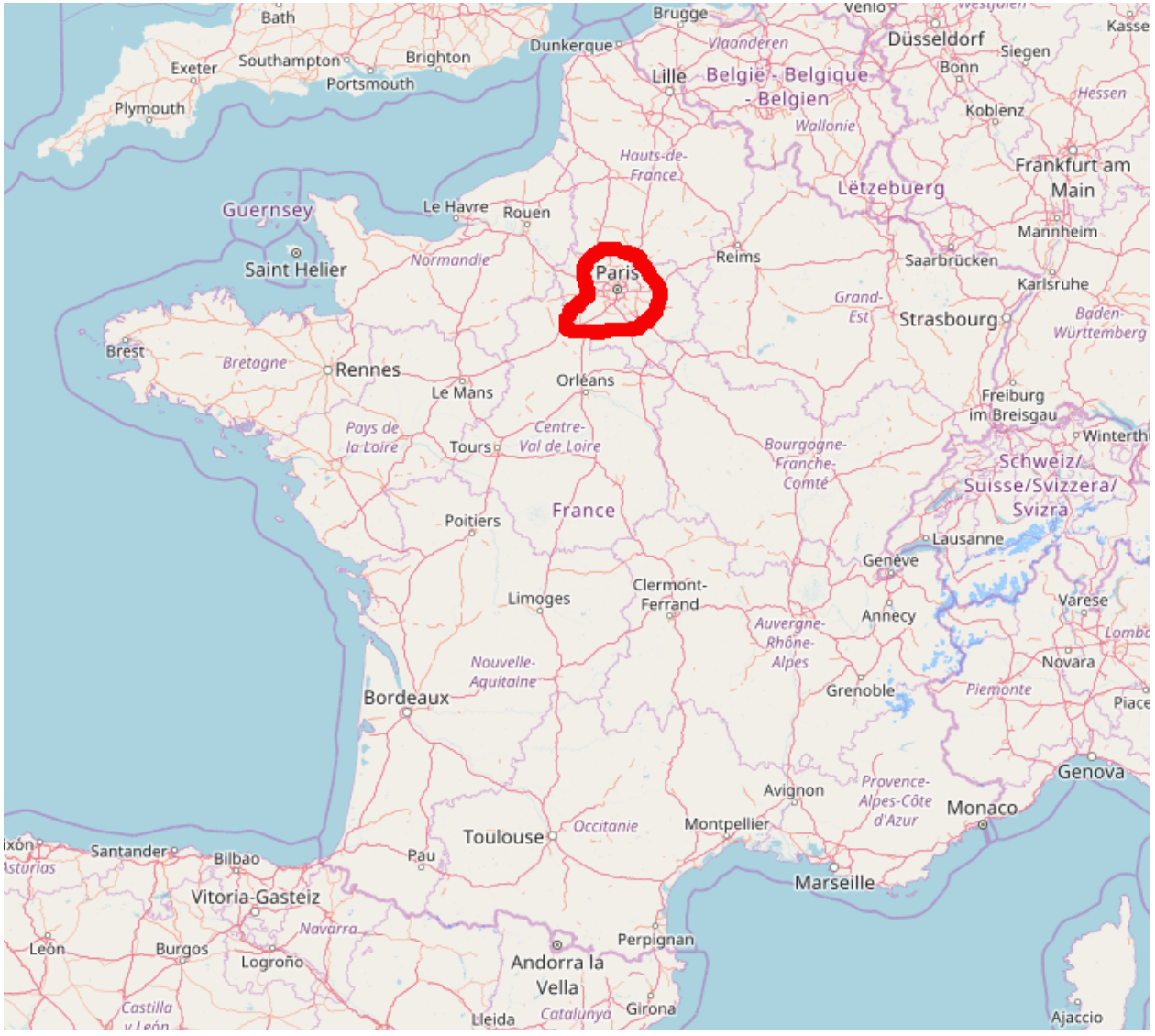
Best Paper Award at Modelsward'2017

Members

- 5 Full-time researchers (by arrival order): Renaud Pacalet, Sophie Coudert, Ludovic Apvrille, Rabéa Ameur-boulifa, Tullio Tanzi
- 1 half-time research engineer: Dominique Blouin
- 7 Ph.D. students (by arrival order): Florian Lugou, Letitia Li, Maciej Bielski, Vincent Hui, Lilia Bellabed, Giovanni Camurati, Matteo Bertolino.

TPT ...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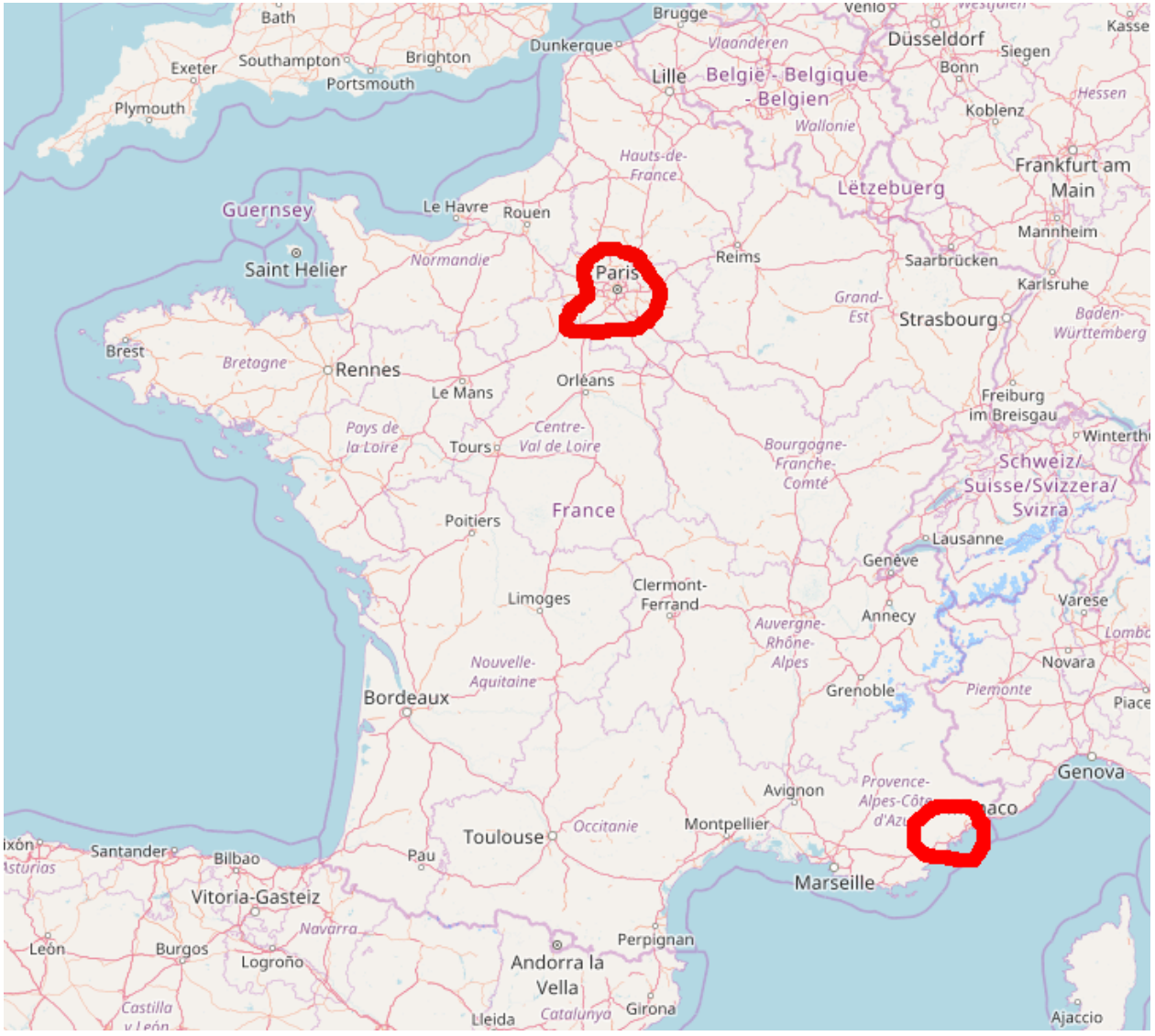
TPT !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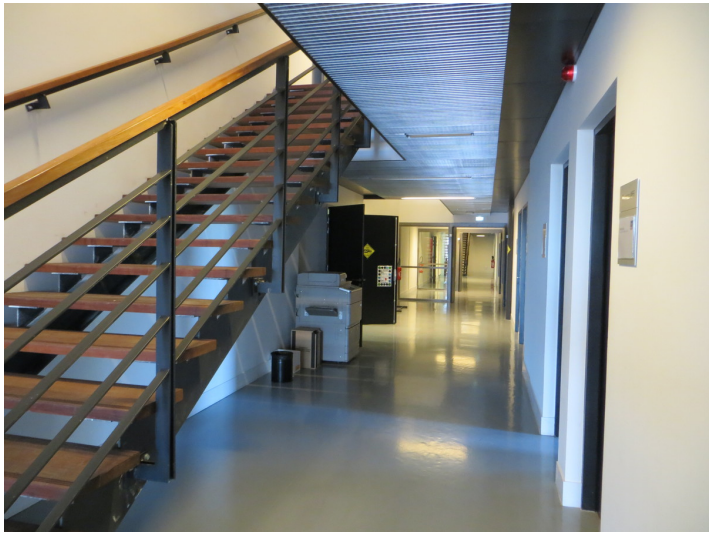
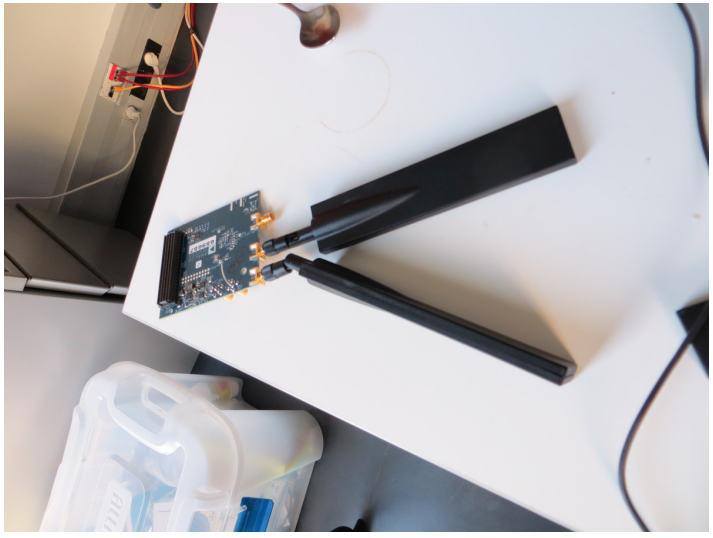
Our Building

Our Building (Cont.)

Our Building (Cont.)



Our Building (Cont.)



Research Work: Overview

Modeling and Verification for Safe and Secure Embedded Systems

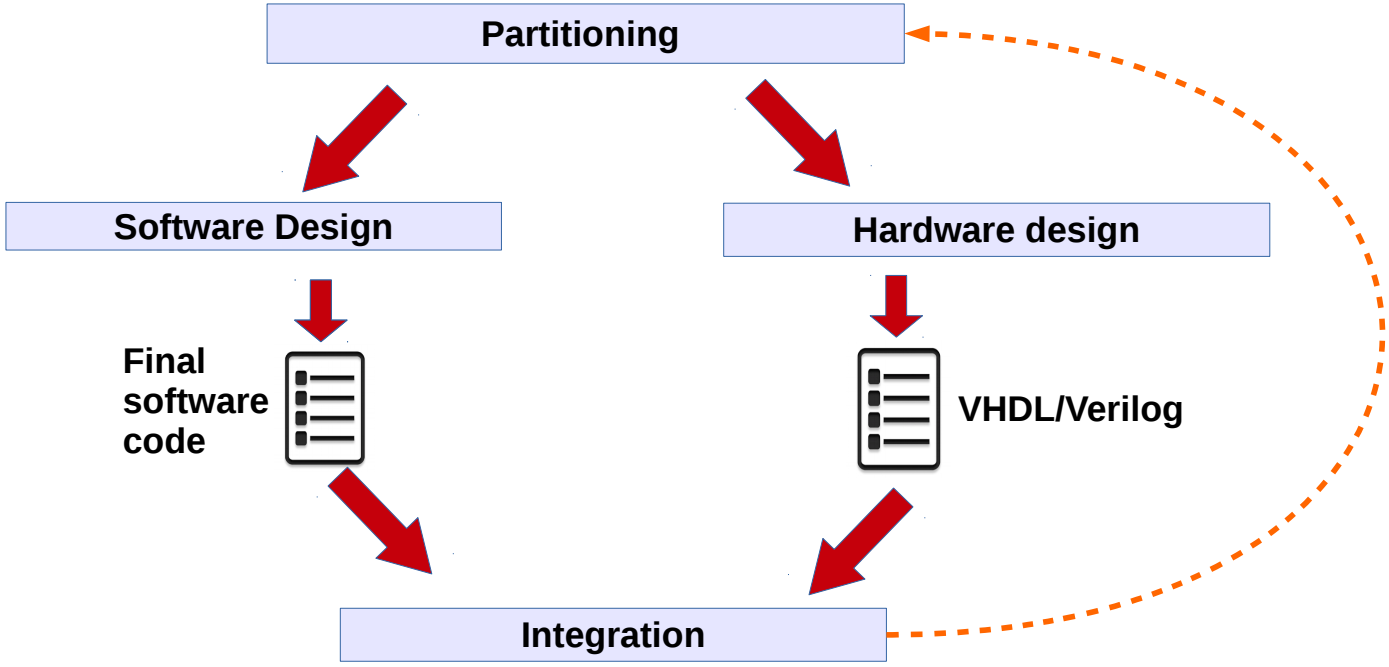
Application domains

IoT, Transports (automotive, drones), telecommunication systems (5G, Software-Defined Radio)

Contracts&projects

Local (Labex, FUI, ...), national (Nokia lab, ...), international (H2020 "AQUAS", ...)

Designing Embedded Systems



Other contributions: Usually focused on one modeling aspect: difficult to iterate between partitioning and design

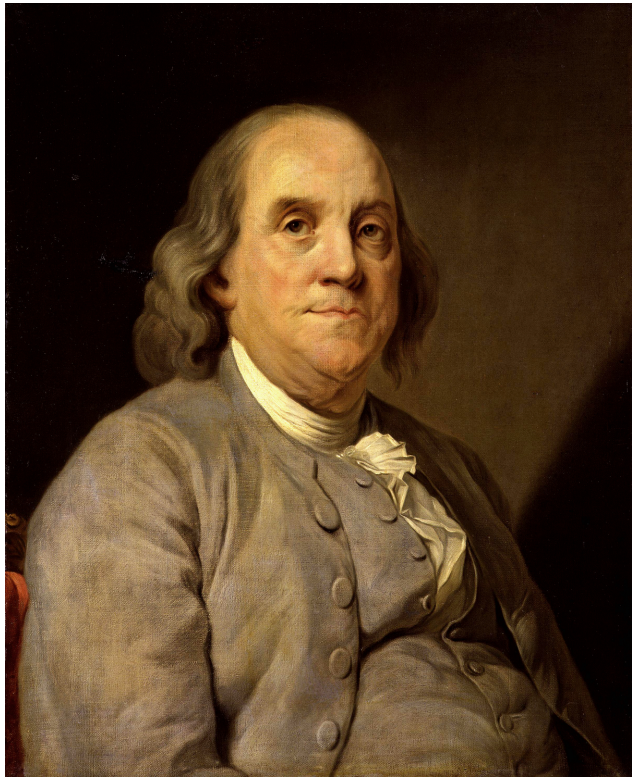
Our Proposal

A model-based approach with a close interaction between partitioning and software design

Modeling is not Really a New Technique...

...and it is not limited to Software!

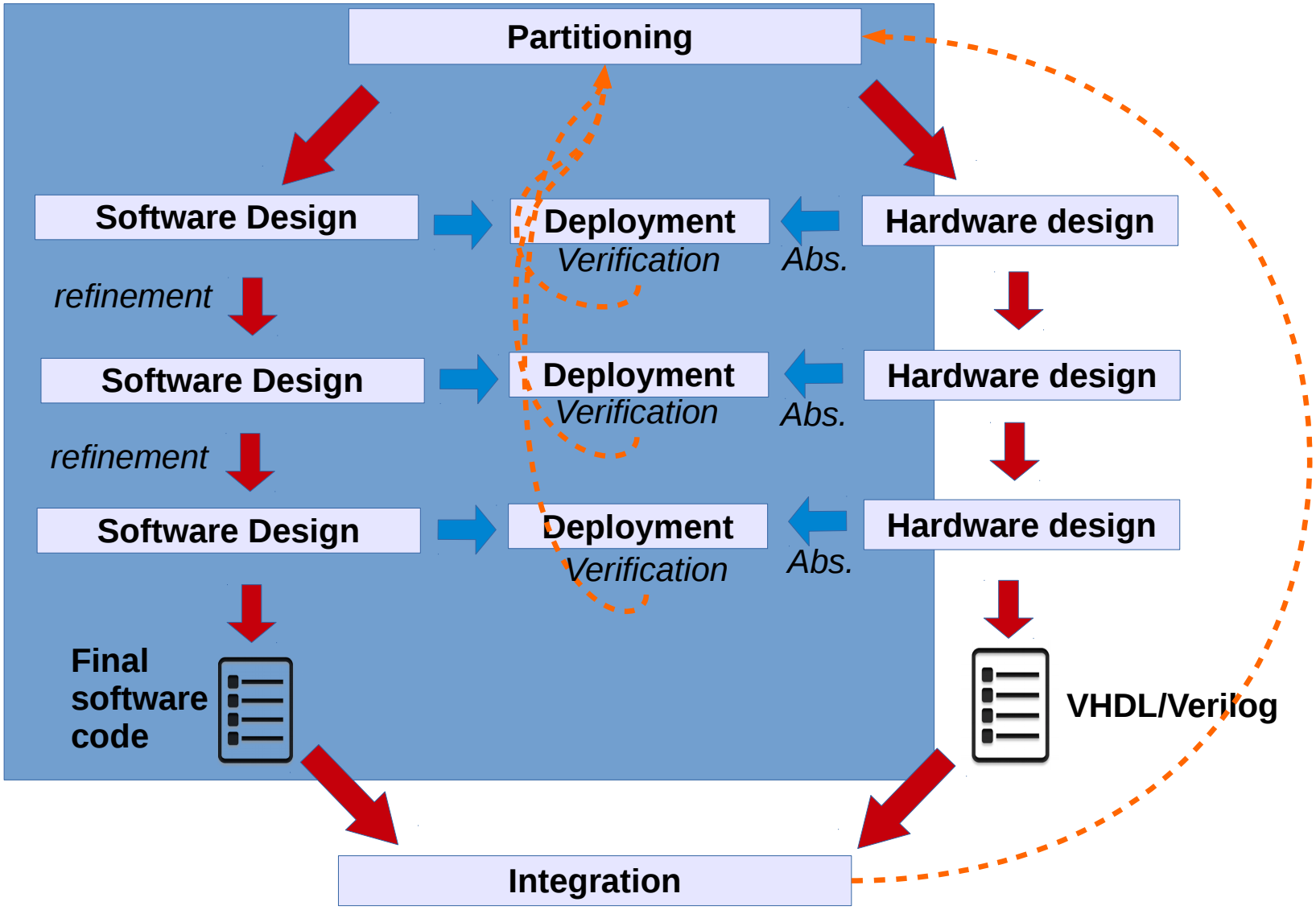
Modeling is not Really a New Technique...



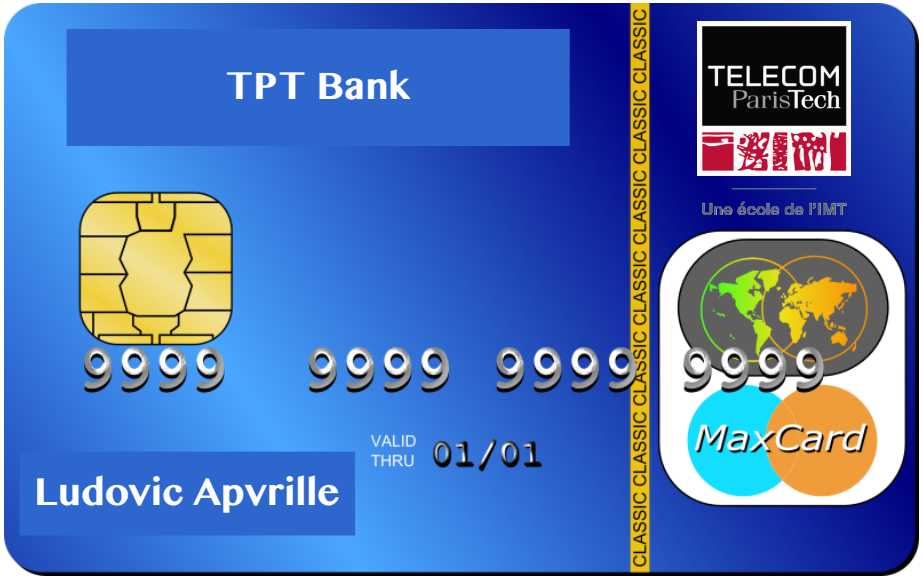
Painting by Duplessis.
Source: Wikipedia

"If you fail to plan,
you are planning to fail!"

Method

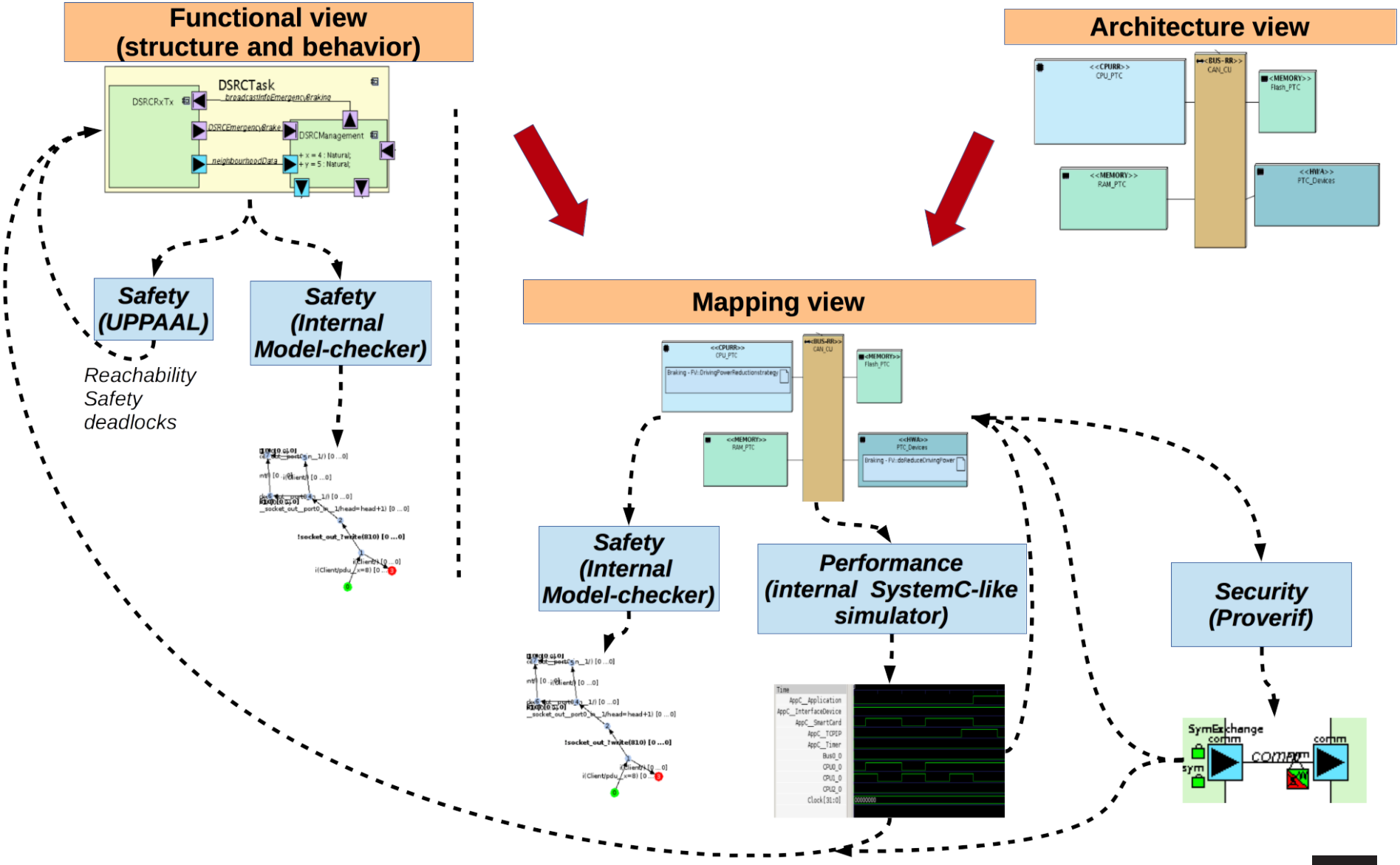

Partitioning
Software Design
Deployment
Verification
Abs.
Hardware design
refinement
Software Design
Deployment
Verification
Abs.
Hardware design
refinement
Software Design
Deployment
Verification
Abs.
Hardware design
Final software code
VHDL/Verilog
Integration

Case Study: Smart Card

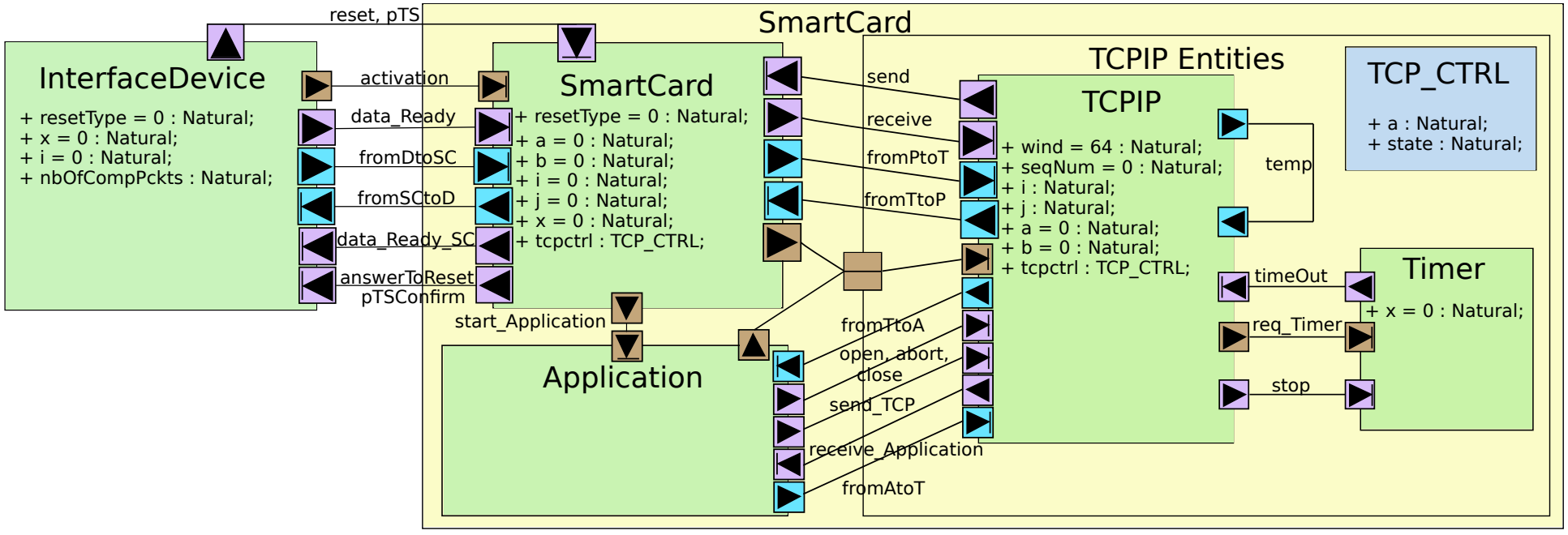


- Read or write transactions
- Hardware accelerators and processors

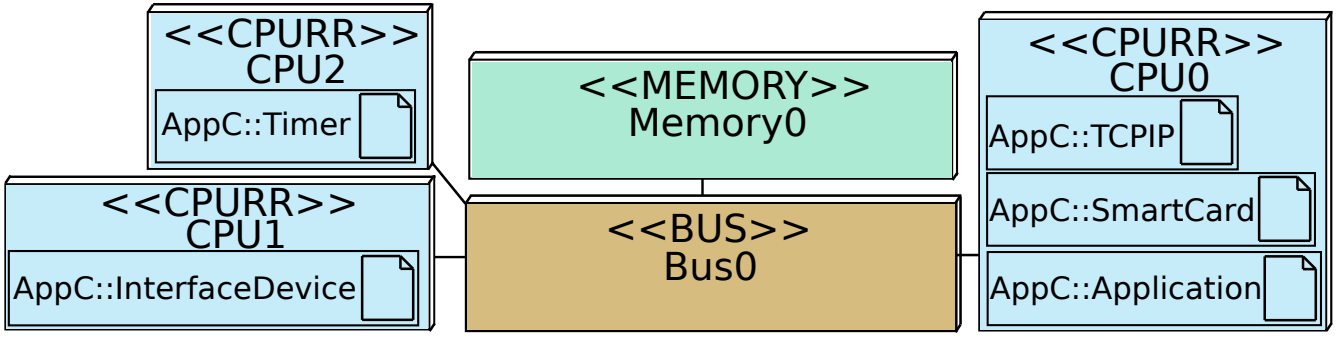
Partitioning Method

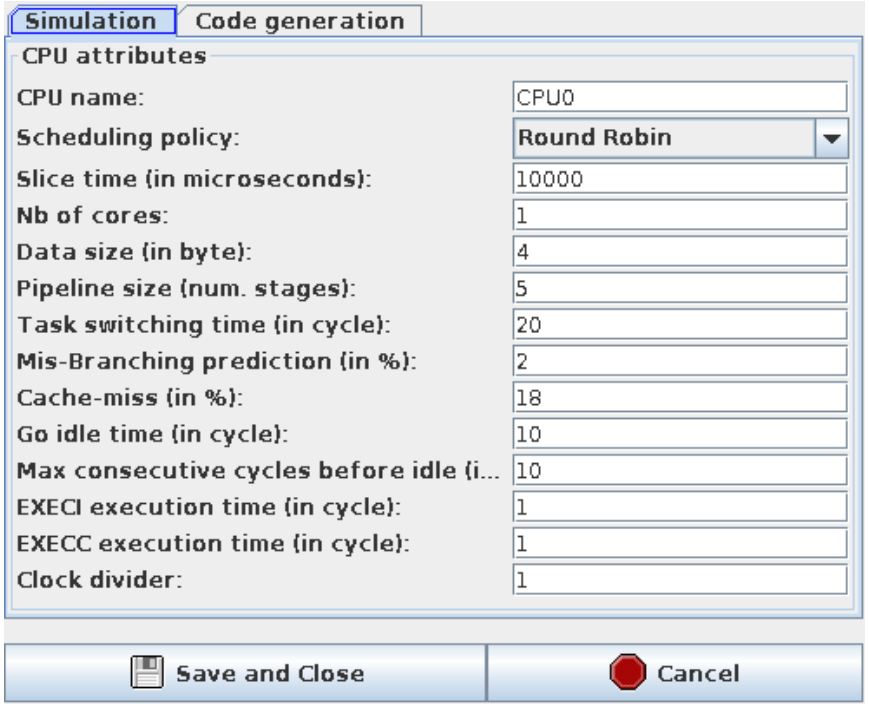


Functional View

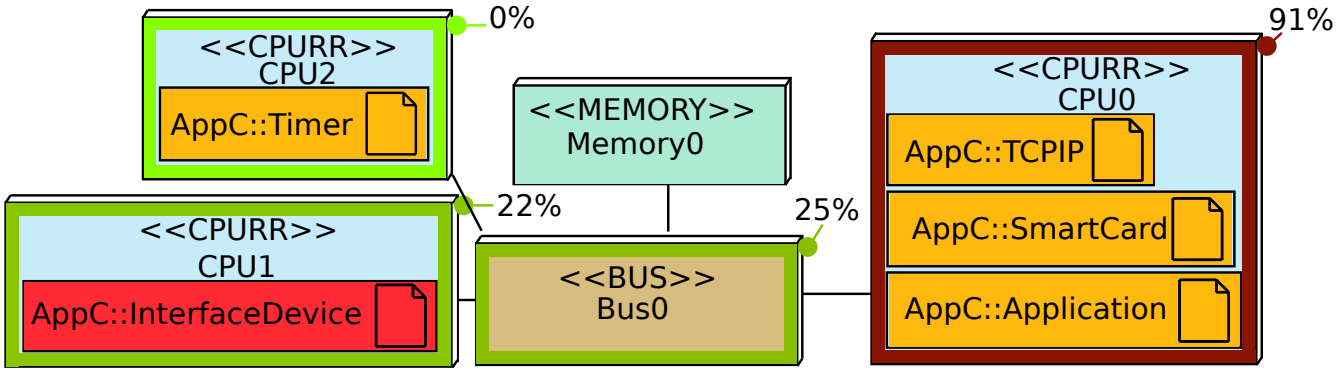


Mapping View

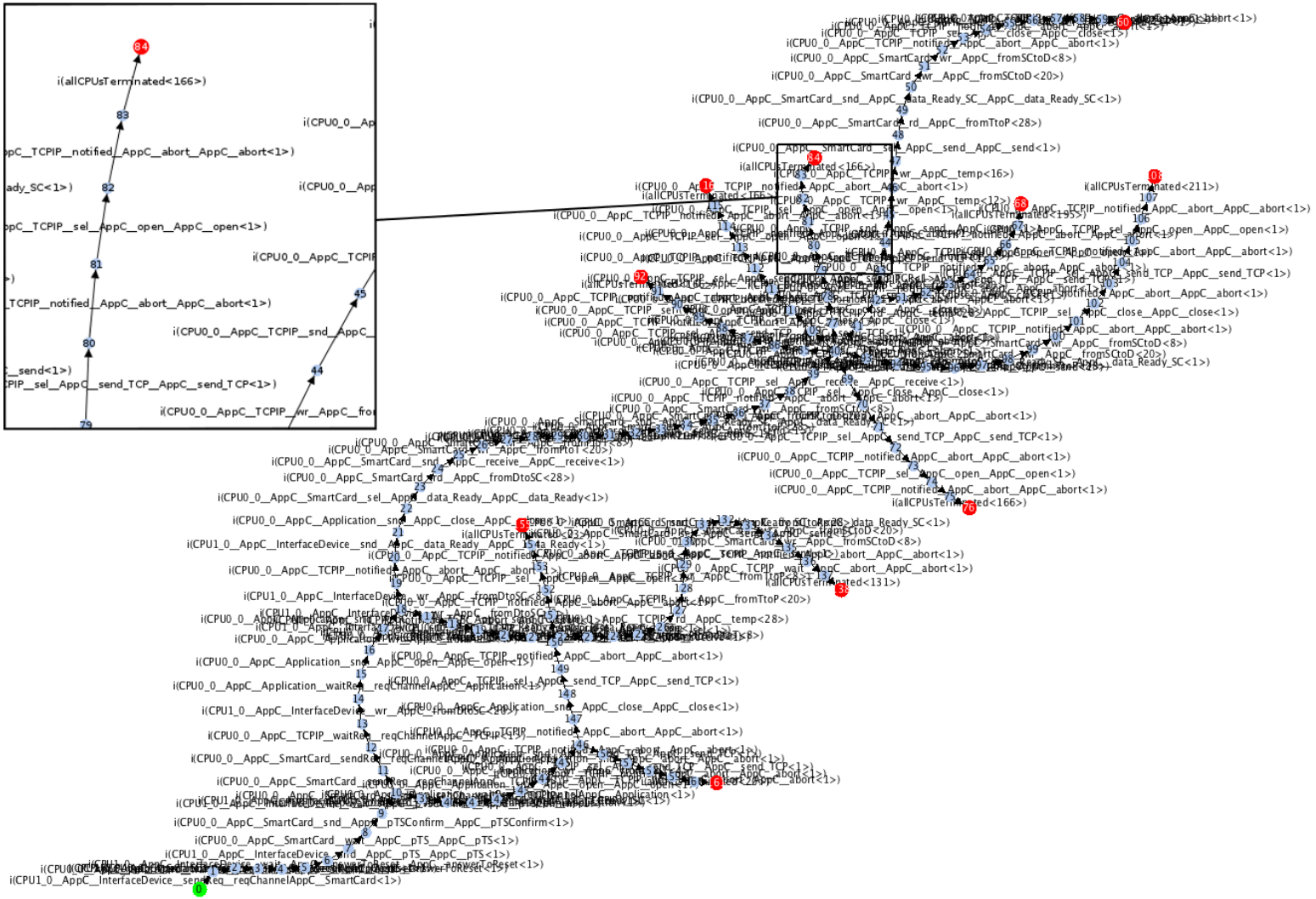




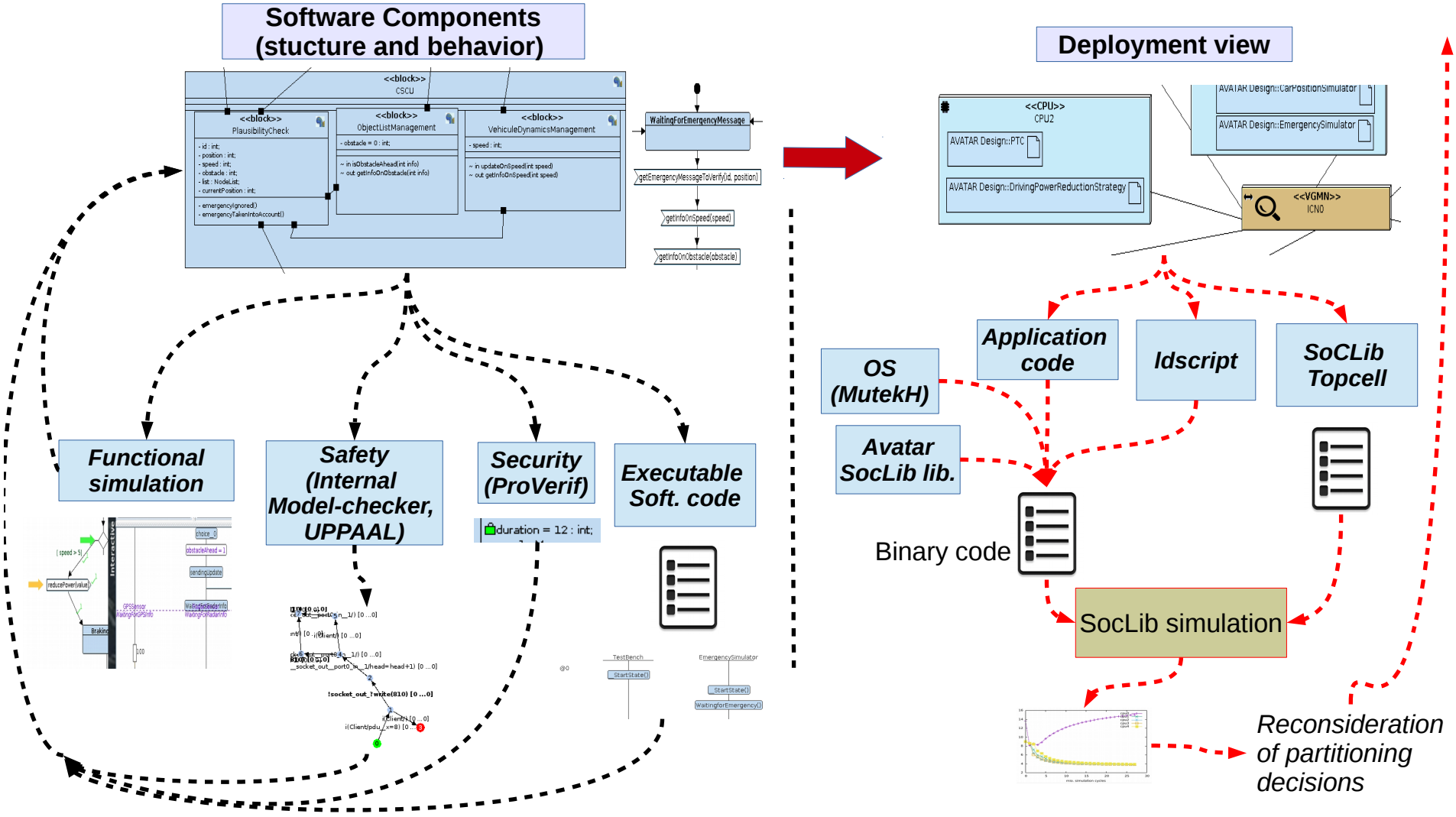
Mapping View (After Simulation)



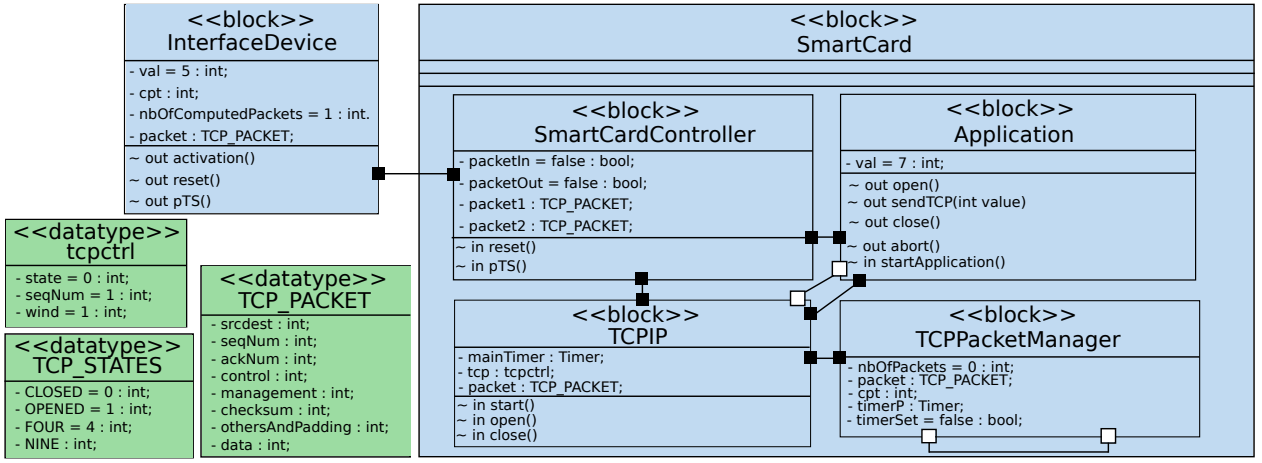
Mapping View (RG)

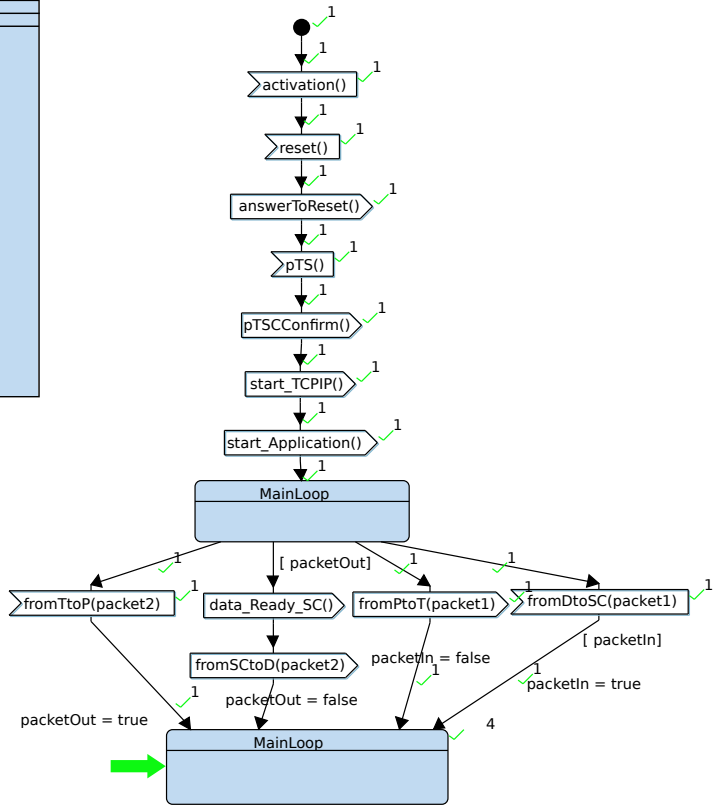


Software Design Method

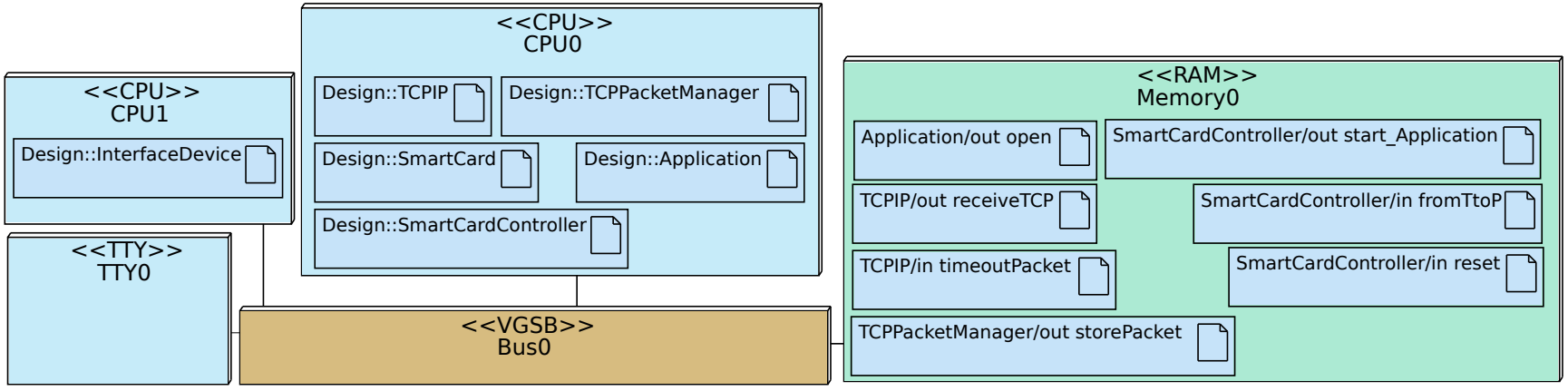


Software Components

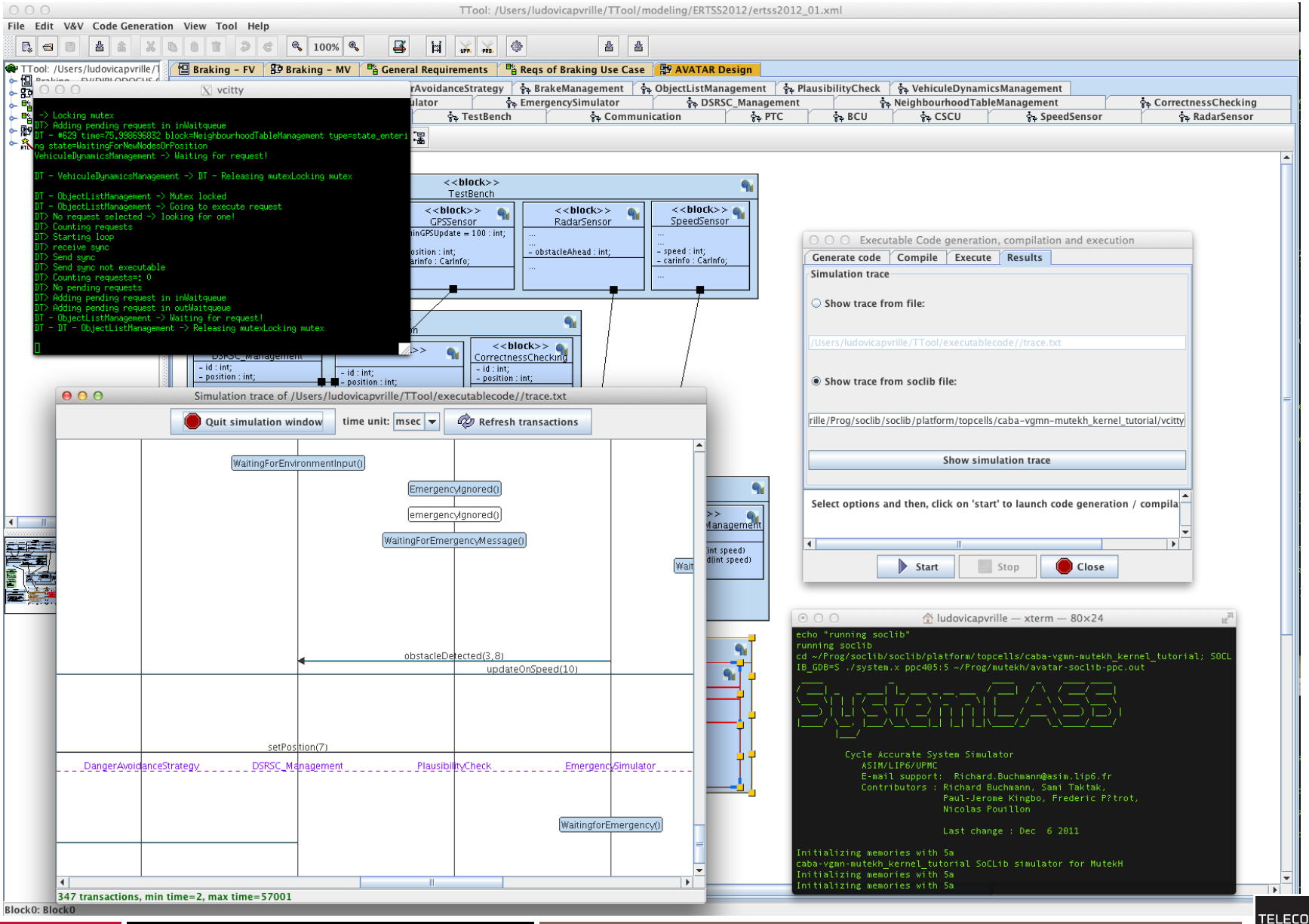




Deployment View



SoCLib "CABA" Simulation

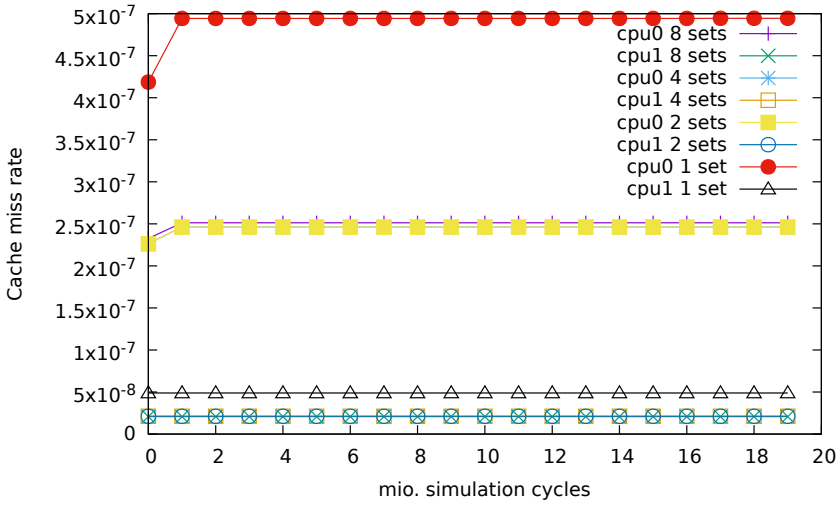


Typical Performance Information

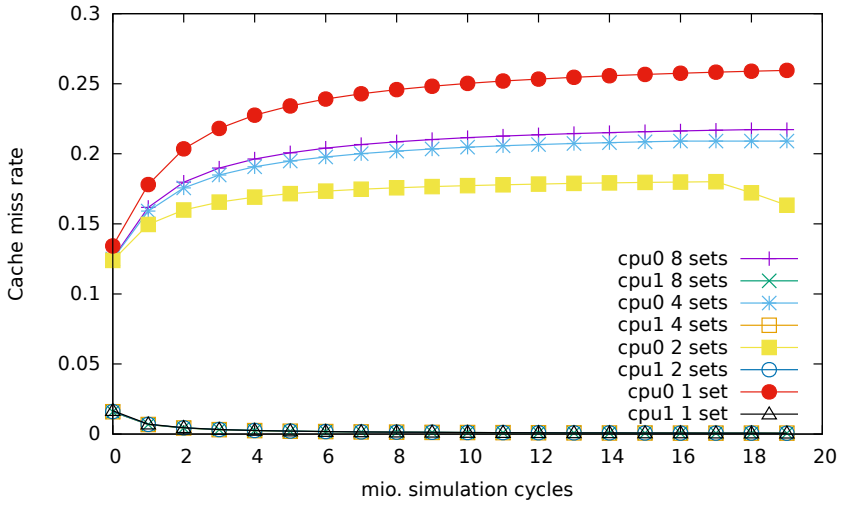
- Overhead due to context switching (Cycles per Instruction)
- Memory access latency
  - Data and instruction cache miss
- Bus contention

Performance Information: Cache Miss

Data-cache miss



Instruction cache miss



(Configuration: 2 processors, 1 to 4 cache sets)

Conclusion and Future Work

Contributions

- Multi-level design of embedded systems
- Push-button approach for simulation and formal verification

What's next?

- Design Space Exploration, with automatically suggested modifications
- More detailed performance profiles (buffer fill state etc.)

Thank You!

References

TTool: ttool.telecom-paristech.fr

SoCLib: www.soclib.fr

Personal website:
http://perso.telecom-paristech.fr/~apvrille