

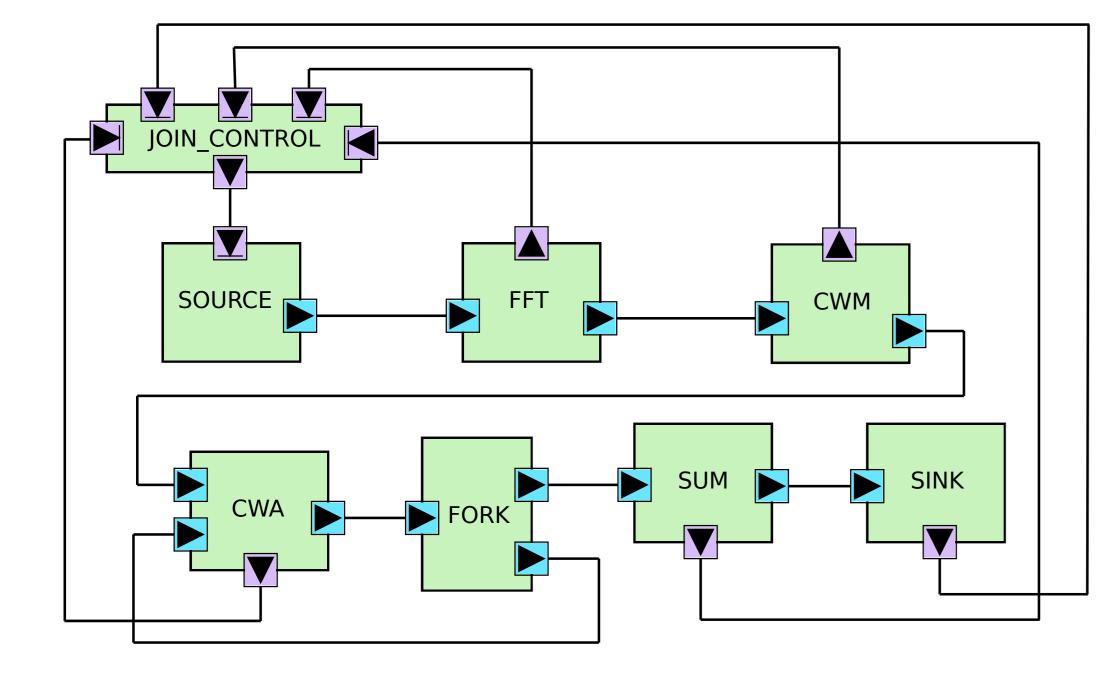
Hw/Sw Co-Design of Data-Dominated Systems-on-Chip - The Ψ-chart Approach in TTool/DIPLODOCUS -

Supported by the French FUI project **NETCOM** under grant agreement n. F1405046 U

Andrea ENRICI, Adrien CANUEL, Ludovic APVRILLE, Daniel CAMARA, Renaud PACALET Institut Mines-Telecom, Telecom ParisTech, CNRS/LTCI - Sophia Antipolis, France

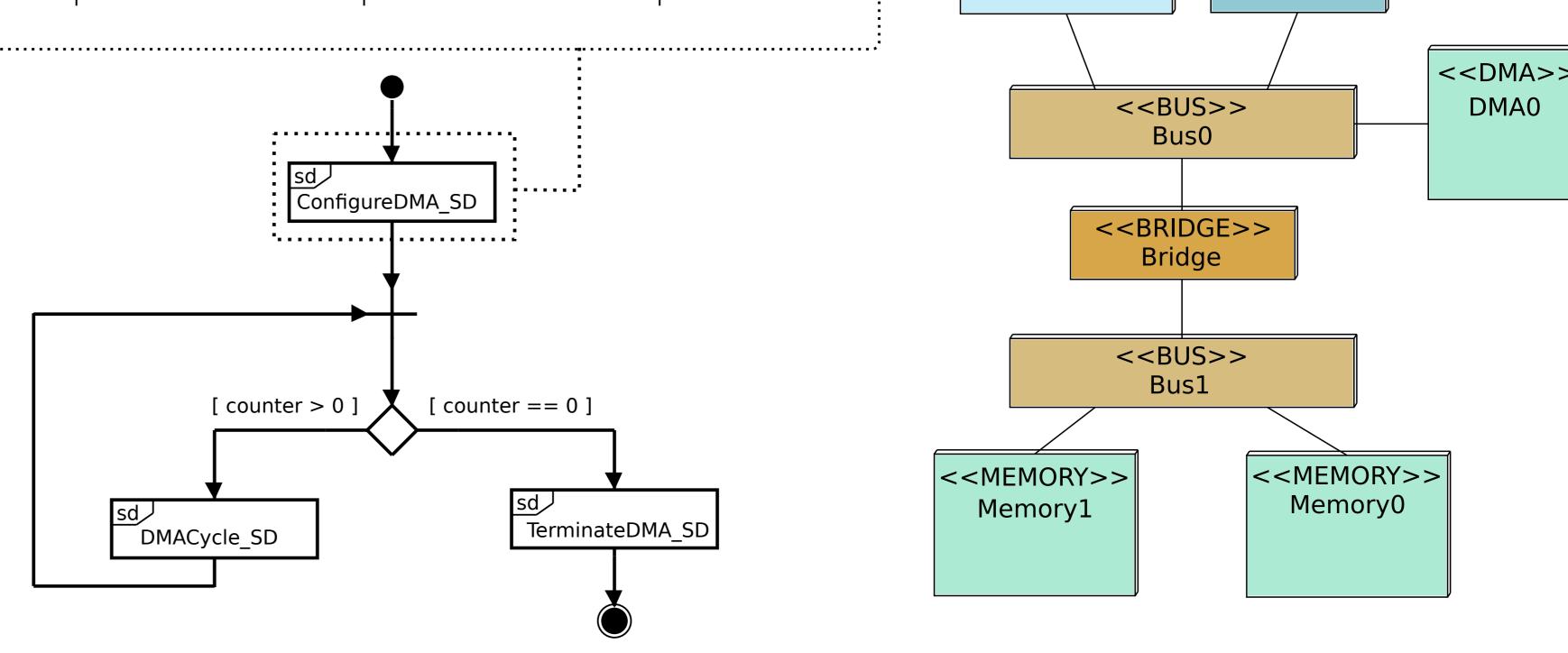
System Level Modeling with the Ψ -chart: Application, Communications, Architecture and Mapping

CPU_Controller TransferInstance_1 DMA_Controller							
TransferRequest	(bytesToTransfer, source	Address, destinationAdd	ress, ID1)				
TransferRe	> equest(bytesToTransfer,	sourceAddress, destinati	onAddress, ID1)		< <cpu>> CPU0</cpu>	< <dsp>> DSP0</dsp>	
		counter =	bytesToTransfer				



Application (what): Dataflow graph with data and functional abstractions, where algorithms are described using abstract cost operators



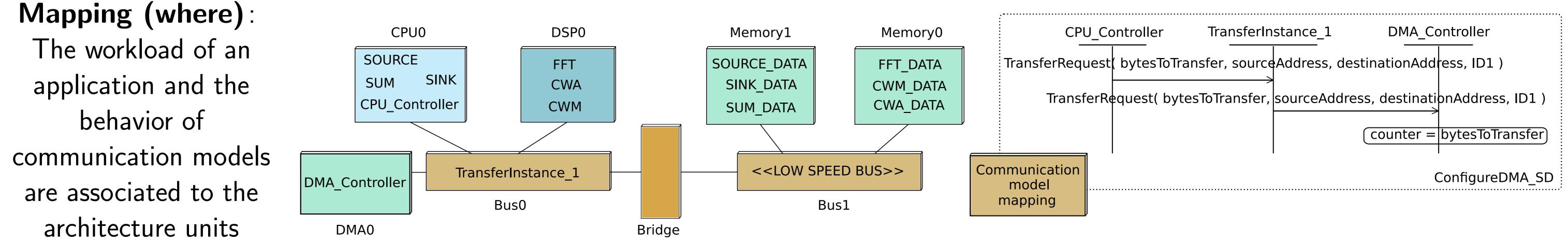


Communications (how):

Behavioral model of generic communication protocols that are described independently of the application and architecture models

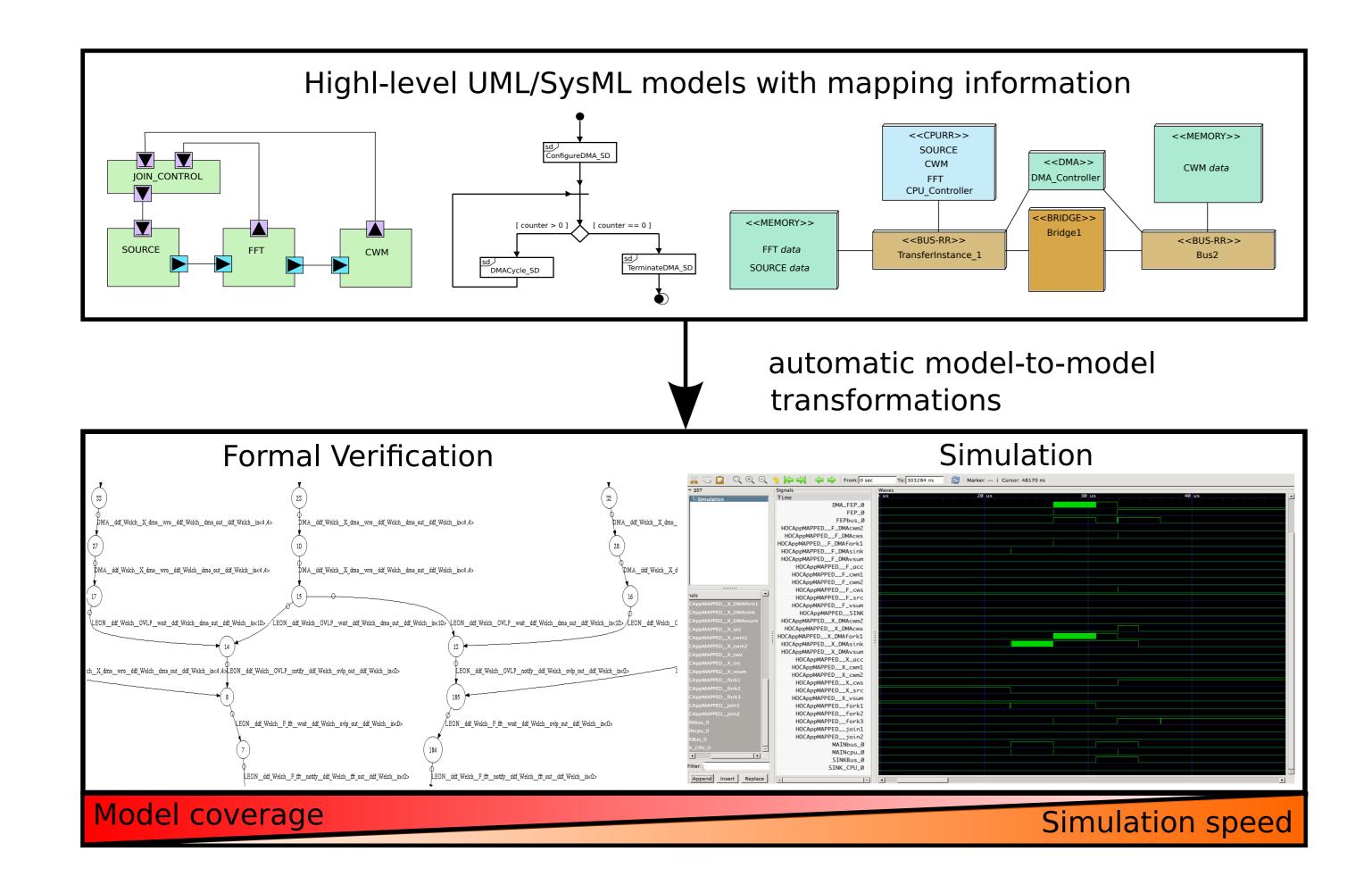
Architecture (who):

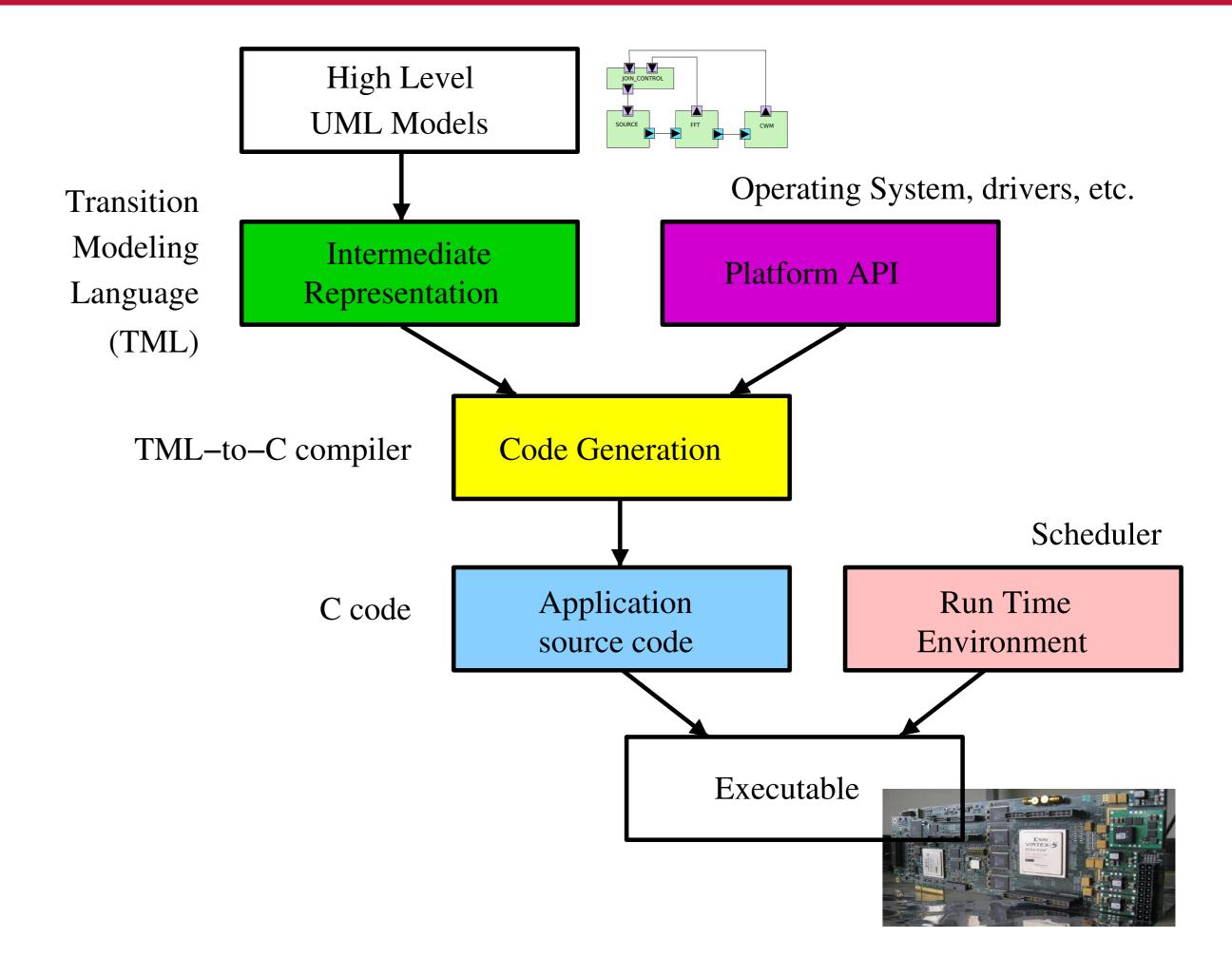
Set of interconnected generic hardware nodes, decorated with parameters, e.g., bus width, arbitration policy



Design Space Exploration: Simulation and Formal Verification at the push of a button

Automatic Generation of Executable Code from High Level Models





Model-checking of system properties (e.g., safety, schedulability, performance) with LOTOS and UPPAAL **Functional simulation** interactively, with graphical interface and debug facilities (e.g., breakpoints, simulation traces)

An **executable implementation** of the application is automatically generated for rapid prototyping on the real hardware: only memory allocation and data-blocks addresses must be manually encoded